Single Coupled-Inductor Dual Output Soft-Switching DC-DC Converters with Improved Cross-Regulation and Reduced Components

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***Abstract*—Single inductor dual output (SIDO) dc-dc converters are attractive in diverse applications such as renewable energy systems and electric vehicles, due to its favorable advantages of reduced magnetic core and high power density. However, in conventional SIDO converters, severe cross-regulation problem is caused by the multiplex of inductor current, resulting in deteriorated dynamic performance. In order to alleviate the cross-regulation problem, a new family of dual output dc-dc converters is proposed in this paper, which employs a coupled-inductor to substitute the inductor in SIDO converters. The proposed converters can achieve improved dynamic performance while keeping the advantage of reduced magnetic core. Moreover, the number of semiconductor devices is reduced in comparison with conventional SIDO converters, and soft-switching operation of switches is also achieved. Therefore, lower cost and higher power density are obtained. In the paper, topology derivation of proposed converters from conventional SIDO converters are firstly demonstrated in detail. After that, the operation principle, steady-state characteristics and small-signal model are provided. Finally, design example and experiment results are given to validate the merits of the proposed topology.**

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I. INTRODUCTION

Nowadays, multiple-output dc-dc converters are extensively applied in many fields such as renewable energy systems [1-3], electric vehicles [4, 5] and consumer electronics [6-9]. Although conventional *N* separate dc-dc converters can easily generate *N* outputs, the number of components increases *N* times, which causes high cost and large size of system. In order to achieve high power density and low cost, single inductor multi-output (SIMO) dc-dc converters have been proposed in [10-26].

In SIMO converters, only one inductor is needed, which remarkably reduces the number of magnetic components. Therefore, its system volume can be significantly reduced and high power density is achieved. Due to its attractive advantage, numerous researches have been conducted. In [11], an SIMO boost converter that can supports series regulated outputs for low- and high-power applications is proposed. A novel SIMO buck-boost converter is presented in [12], which achieves both step-up and step-down conversions and is a suitable topology to eliminate voltage imbalance of DC link in diode-clamped multi-level inverters. In [13], operation principle, control design as well as challenges of SIMO dc-dc converters based on buck, boost and buck-boost converters, are introduced and evaluated. And a new family of SIMO dc-dc converters with reduced semiconductor devices is proposed in [14]. In [15], a SIMO topology which can support independent buck, boost, and inverted outputs simultaneously is put forward. SIMO topology also can be applied in multiple port dc-dc converters [16, 17] to realize power regulation in input port and voltage regulation in output port.

However, SIMO converters suffer from an inherent drawback. Multiplexing inductor current leads to serious cross regulation problem between different outputs when SIMO converters work in continuous conduction mode (CCM), resulting in terrible dynamic behavior and system instability. A variety of researches have been conducted to solve this problem. There are two common solutions, including different operating mode and improved control methods.

In [18] and [19], SIMO converters operate in discontinuous conduction mode (DCM) and thus effectively alleviates cross-regulation. Nevertheless, DCM limits the output power of SIMO converters owing to large current ripple existing in heavy load, which also gives rise to high current stress and severe EMI problem. To reduce the peak inductor current, a freewheel period is added to ensure converters working in pseudo continuous conduction mode (PCCM) [20] through an additional freewheel switch. Although PCCM makes up the drawback of DCM, costs and conduction losses are increased due to the auxiliary switch.

To eliminate cross regulation problem in CCM, a variety of control schemes are proposed in [21-26]. A digital control approach is presented in [21], where common-mode and differential-mode output voltages are regulated respectively. And a variable gain compensation is used in differential-mode loop for cross regulation elimination. In addition to voltage loop, a current loop is added in [22] to accelerate outputs recovery from load changes. In [23], inner current loop and the outer voltage loop with an interleaving scheme are designed to obtain good dynamical behavior. A novel modeling method is derived in [24], and cross-regulation transfer function is calculated and compensated with the help of the model. In [25], a predictive digital current control is proposed where

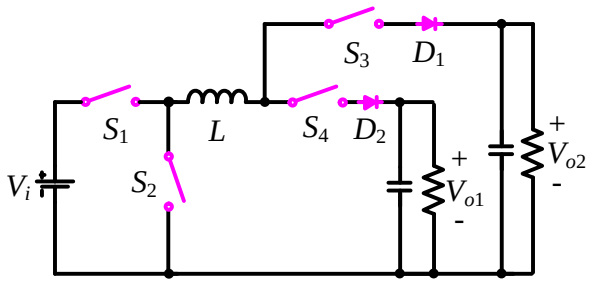
duty cycles for the next switching cycle are calculated by load current. A power-weighed CCM controller and a floating capacitor-based output filter are designed in [26] to suppress cross regulation and maintain power quality. Although these approaches effectively improve the performance of SIMO converters, the control complexity is greatly increased because of sophisticated algorithms.

In order to obtain novel converters that have high power density, low cost and simple control strategy, a new family of single coupled-inductor dual output (SCIDO) soft-switching(SS) dc-dc converters is proposed in this paper. The proposed converters not only keep the advantage of single inductor dual output (SIDO) converters that only one magnetic core is needed, but also achieve improved cross regulation with simple control strategy. Besides, compared with conventional SIDO converters, the number of switches or diodes are reduced in the proposed converters, and thus the overall cost is further reduced. Moreover, zero-voltage switching(ZVS) or zero-current switching(ZCS) operation of switches are achieved and the reverse-recovery problem of switch is eliminated, which contributes to reduced switching losses.

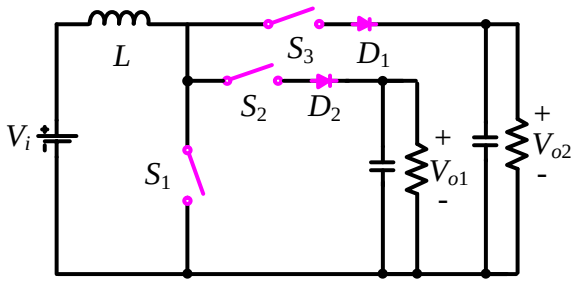
The rest of this paper is organized as follows. The topology derivation from conventional SIDO converters to the proposed SCIDO converters is introduced in Section II. Section III presents the operation principle of proposed converters. Circuit characteristics are detailed discussed in Section IV. The design example and experiment result are given in Section V. Finally, a conclusion is drawn in Section VI.

II. Topology Derivation

Fig. 1 shows the conventional SIDO converters based on buck, boost and buck-boost converters [13, 14], in which energy is delivered to each output in different interval by controlling switches S_3~S_4 of converter in Fig. 1(a) and S_2~S_3 of converter in Fig. 1(b)~ (c). Since only one inductor is utilized, the overall system volume and cost are effectively reduced. However, due to the multiplex of inductor current, load variation of one output will influence another output voltage in the CCM, resulting in severe cross-regulation problem. Moreover, the switches in SIDO converters are hard-switching and as a consequence, switching losses are high. In order to achieve improved cross-regulation as well as lower switching losses, a novel family of SCIDO converters is proposed in this paper, which is simply derived from SIMO converters but with more favorable performance characteristics.



(a)



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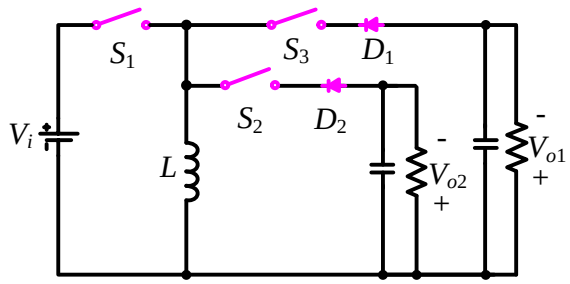


(c)

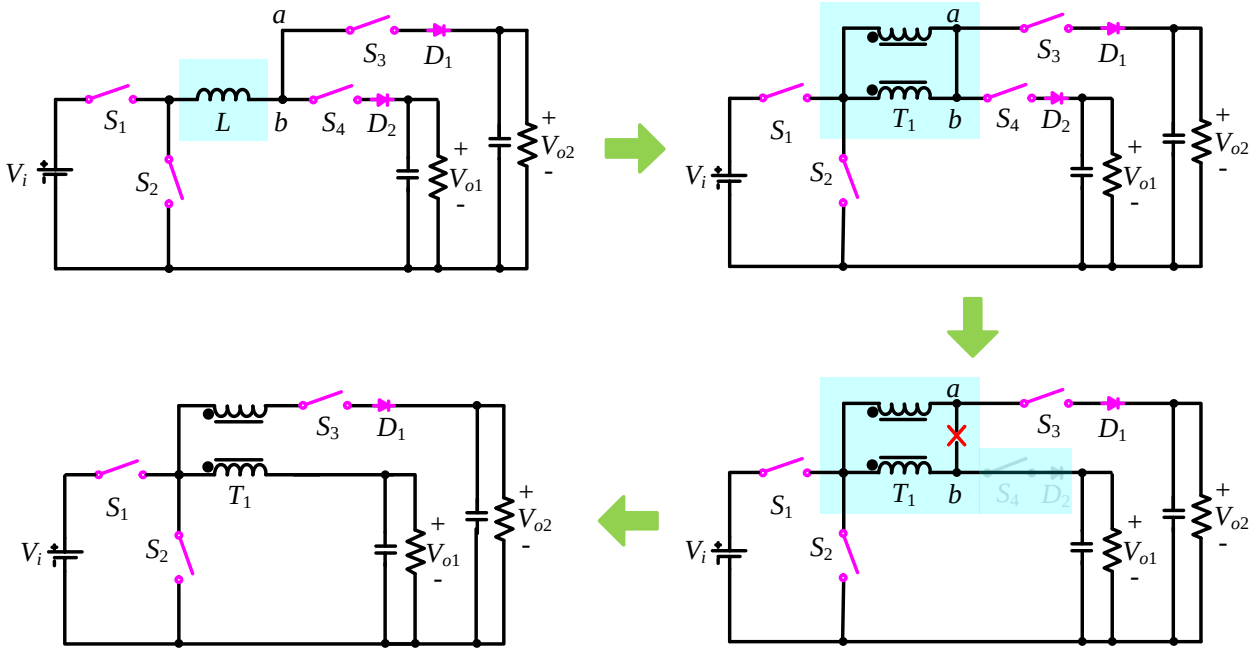
Fig. 1 SIDO converters based on different converters: (a) buck, (b) boost and (c) buck-boost converter

In order to obtain a comprehensive understanding, detailed topology derivation of proposed SCIDO SS converter based on buck converter is illustrated as an example, which is derived from the SIDO converter in Fig. 1(a). Firstly, the inductor L can be made equivalent to a coupled inductor with turns ratio 1:1, as shown in Fig. 2(a). Then disconnect the connection (a, b) of coupled inductor right side to eliminate cross-regulation problem caused by multiplex of inductor current. Actually, the turns ratio of coupled inductor can be designed arbitrarily to achieve flexible relationship between two output voltages V_{o1} and V_{o2}. After disconnection, the switch S_4 and diode D_2 are not required anymore and thus, can be eliminated. Likewise, the proposed SCIDO converters based on boost and buck-boost converter are also simply derived in Fig. 2(b) and Fig. 2(c). Compared with conventional SIDO converters, the proposed converters are more preferred due to the following advantages:

(1) Two outputs are independently controlled and thus no cross-regulation problem exists,

(2) All switches are ZVS or ZCS,

(3) Number of semiconductor device is reduced.



(a)

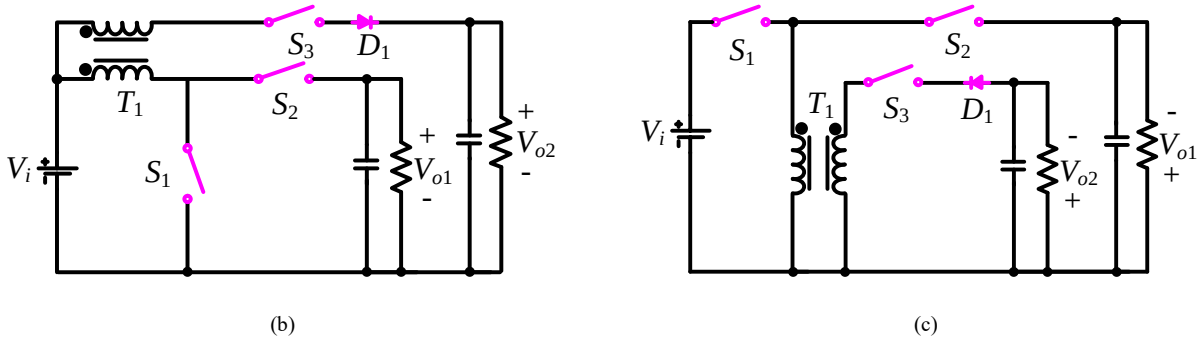


Fig. 2. Proposed dual-output dc-dc converters based on different converters: (a) buck, (b) boost and (c) buck-boost converter

III. Operation Principle

Since the operation principle of proposed converters in Fig. 2 are similar, SCIDO converter based on buck converter is chosen as an example to analyze, and its equivalent circuit is illustrated in Fig. 3(a). The coupled inductor T_1 is equivalent to a leakage inductor L_r, magnetizing inductor L_m, as well as an ideal transformer whose turns ratio is N_p:N_s(=1:n).

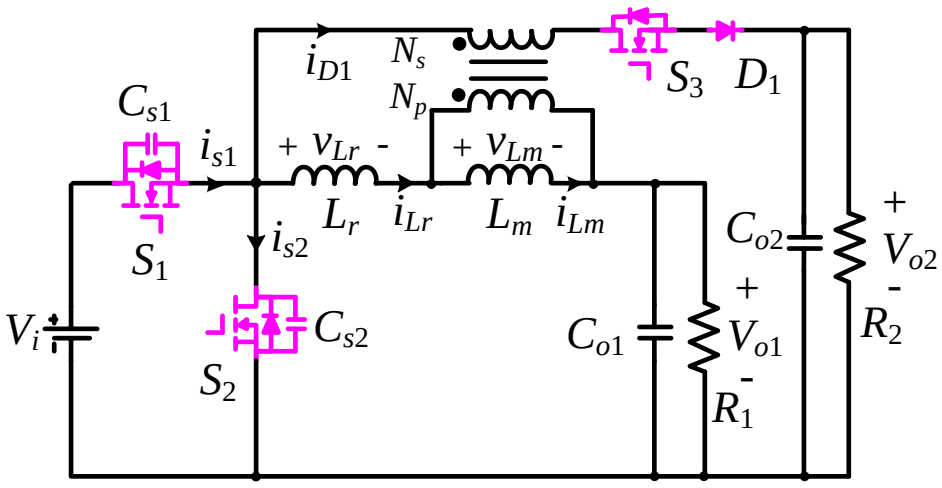
In order to simplify the analysis, the following assumptions are made:

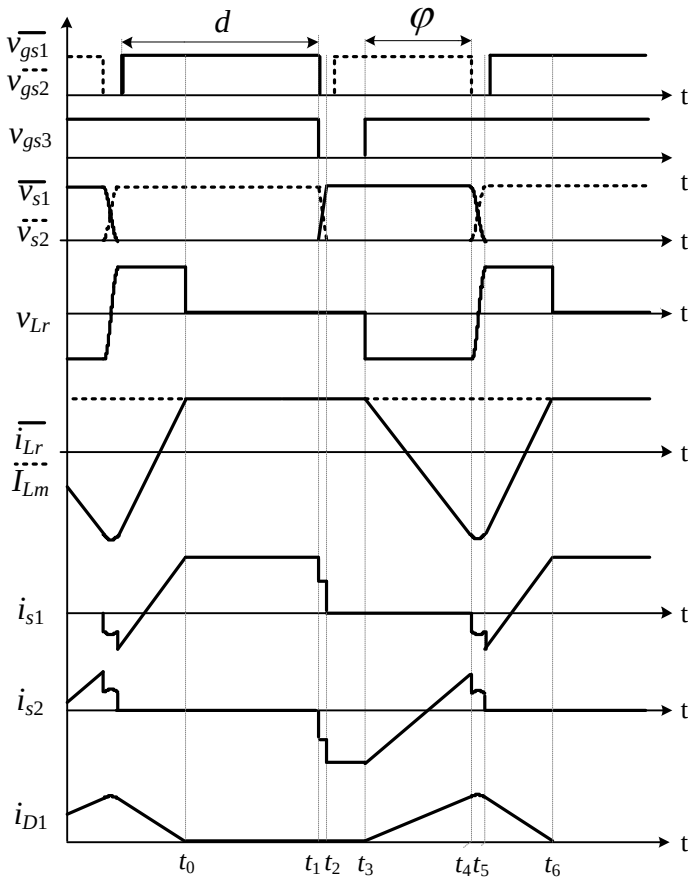
(1) Compared with the leakage inductance L_r, the magnetizing inductance L_m is much larger and thus magnetizing current i_{Lm} is approximately constant.

(2) All components in circuit are ideal except for the parasitic capacitor C_{s1} and C_{s2} of switches S_1 and S_2.

(3) The parasitic capacitances C_{s1} and C_{s2} are constant and their sum is represented by C_s.

The key operating waveform is shown in Fig. 3(b). In Fig. 3(b), v_{gs1}, v_{gs2}, v_{gs3} are the driving signals of S_1, S_2 and S_3, respectively. Switches S_1 and S_2 are operated complementarily, and the duty cycle of S_1 is d. S_3 is turned on $\varphi\times360°$ in advance before turn-off of S_2, and the duty-cycle of S_3 is $d+\varphi$. The operation in a switching period T can be divided into six different modes, and equivalent circuits of each mode are shown in Fig. 3(c).





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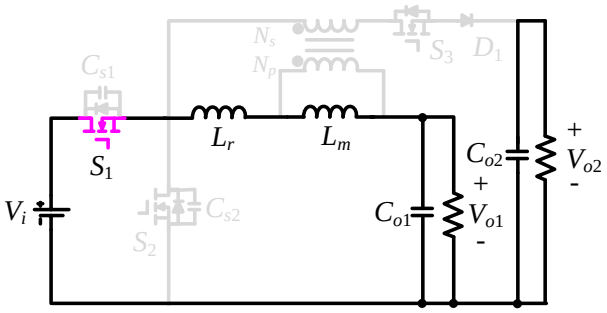
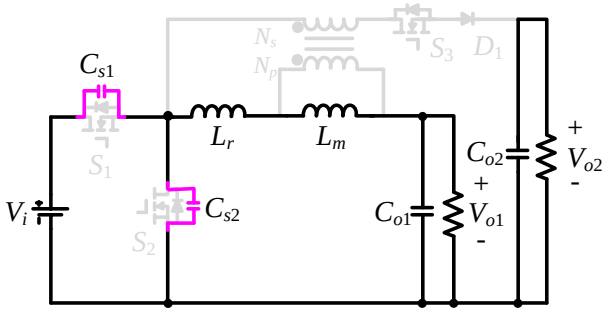
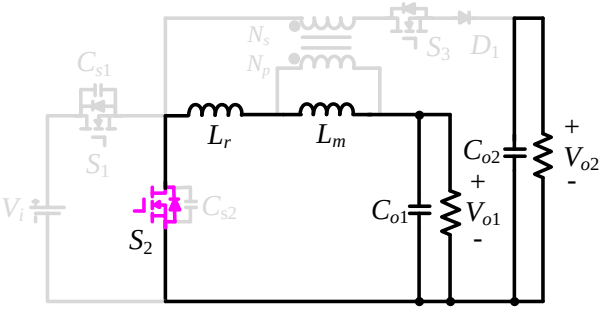


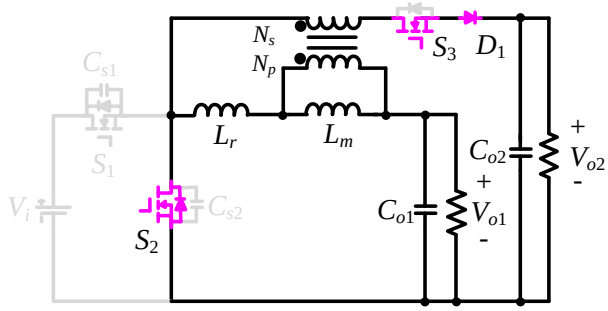
Mode 1[t_0-t_1]



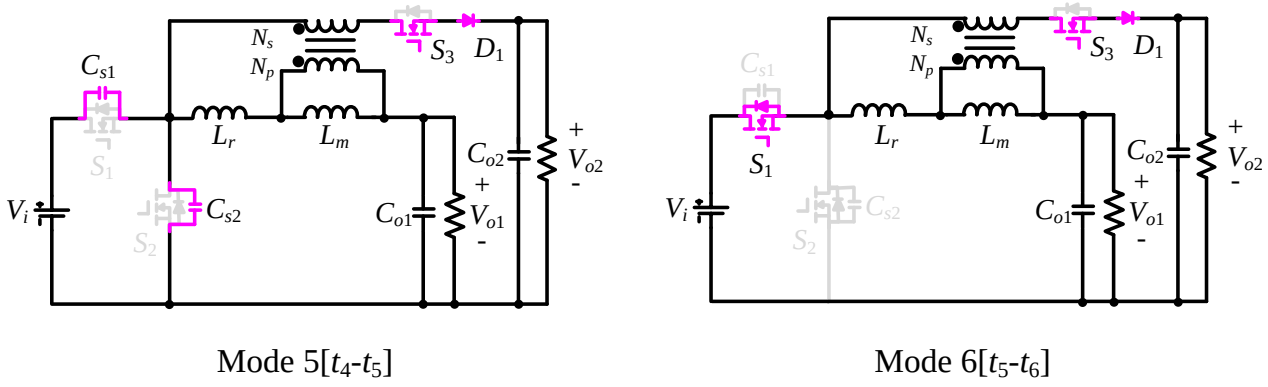
Mode 2[t_1-t_2]



Mode 3[t_2-t_3]



Mode 4[t_3-t_4]



(c)

Fig. 3 Equivalent circuits and key operating waveforms of proposed SCIDO converter based on buck converter: (a) equivalent circuit, (b) key operating waveforms and (c) equivalent circuits in different modes

Mode 1[t_0-t_1]: Prior to t_0, S_1 and S_3 are on, and D_1 is forward biased. The leakage inductor current i_{Lr} increases linearly while the diode current i_{D1} decreases. As soon as i_{D1} decays to zero, Mode 1 begins. V_i-V_{o1} is applied to the leakage inductor L_r and the magnetizing inductor L_m. Since L_m is large enough, the magnetizing current i_{Lm} can be regarded as constant I_{Lm}. In addition, S_3 is turned off at t_1, which realizes ZCS operation.

$$i_{s1}(t) = i_{Lr}(t) = i_{Lm}(t) = I_{Lm} \tag{1}$$

Mode 2[t_1-t_2]: S_1 is also turned off at t_1. The magnetizing current i_{Lm} starts to charge the parasitic capacitor C_{s1} and discharge C_{s2}. Then the drain-to-source voltage v_{s1} rises while v_{s2} falls, as shown in (2) and (3).

$$v_{s1}(t) = \frac{I_{Lm}}{C_s}(t - t_1) \tag{2}$$

$$v_{s2}(t) = V_i - \frac{I_{Lm}}{C_s}(t - t_1) \tag{3}$$

Mode 3[t_2-t_3]: The voltage v_{s2} decreases to zero at t_2. As a result, the body diode of S_2 begins to conduct. Hence, ZVS turn-on of S_2 is achieved. In this mode, the leakage inductor L_r and the magnetizing inductor L_m are discharged by -V_{o1}.

$$i_{s2}(t) = -i_{Lr}(t) = -i_{Lm}(t) = -I_{Lm} \tag{4}$$

Mode 4[t_3-t_4]: S_3 is turned on at t_3 and the magnetizing inductor voltage v_{Lm} is clamped at -V_{o2}/n. Then, the leakage inductor voltage v_{Lr} is obtained in (5) and the leakage inductor current i_{Lr} can be derived in (6). From Fig. 3(b), the relationship among diode current i_{D1}, magnetizing current I_{Lm} and leakage inductor current i_{Lr} is given in (7). With i_{Lr} in (6) and i_{D1} in (7), the drain-source current i_{s2} can be calculated in (8). To eliminate the reverse-recovery problem of body diode, i_{s2} should become positive before S_2 is turned off. Therefore, i_{s2} must increase during this mode, which means v_{Lr} must be negative as shown in (5).

$$v_{Lr} = \frac{V_{o2} - nV_{o1}}{n} < 0 \tag{5}$$

$$i_{Lr}(t) = i_{Lr}(t_3) + \frac{V_{o2} - nV_{o1}}{nL_r}(t - t_3) = I_{Lm} + \frac{V_{o2} - nV_{o1}}{nL_r}(t - t_3) \tag{6}$$

$$i_{D1}(t) = \frac{1}{n}(I_{Lm} - i_{Lr}(t)) \tag{7}$$

$$i_{s2}(t) = -i_{Lr}(t) - i_{D1}(t) = -I_{Lm} - \frac{(n-1)(V_{o2} - nV_{o1})}{n^2 L_r}(t - t_3) \tag{8}$$

Mode 5[t_4-t_5]: S_2 is turned off at t_4. The leakage inductor L_r resonates with the parasitic capacitor C_{s1} and C_{s2}, as shown in (9).

$$\begin{cases} L_r \dfrac{di_{Lr}(t)}{dt} = v_{s2}(t) - \dfrac{1}{n}[v_{s2}(t) - V_{o2}] - V_{o1} \\ C_s \dfrac{dv_{s2}(t)}{dt} = -i_{D1}(t) - i_{Lr}(t) \end{cases} \tag{9}$$

Mode 6[t_5-t_6]: v_{s2} resonates to V_i at t_5, and v_{s1} drops to zero. Then the body diode of S_1 starts to conduct, and thus S_1 realizes ZVS turn-on. In this mode, the voltage of leakage inductor v_{Lr} is obtained in (10). Based on flux balance of the leakage L_r, the average value of v_{Lr} in a switching period is zero. Since v_{Lr} is negative in t_3-t_4, (10) must be positive during this mode, and thus the leakage inductor current i_{Lr} raises linearly. From (7), the diode current i_{D1} ramps down at the same time. At t_6, the leakage inductor current i_{Lr} reaches I_{Lm} while the diode current i_{D1} decays to zero.

$$v_{Lr} = \frac{(n-1)V_i - nV_{o1} + V_{o2}}{n} > 0 \tag{10}$$

$$i_{Lr}(t) = i_{Lr}(t_5) + \frac{(n-1)V_i - nV_{o1} + V_{o2}}{nL_r}(t - t_5) \tag{11}$$

IV. Circuit Analysis

A. *Maximum Diode Current and Reset Time*

Since the switching process in the interval t_4-t_5 is short and negligible in steady analysis, it can be considered that the diode current i_{D1} increases in the interval t_3-t_4 and decrease in the interval t_5-t_6. Define the reset time of diode current (t_6-t_5) as λT. From Fig. 3(b), the maximum diode current $i_{D1,\max}$ is derived in (12) and λT is calculated in (13).

$$\begin{aligned} i_{D1,\max} &= \frac{i_{Lr}(t_3) - i_{Lr}(t_4)}{n} \approx \frac{nV_{o1} - V_{o2}}{n^2 L_r}\varphi T \\ &= \frac{i_{Lr}(t_6) - i_{Lr}(t_5)}{n} \approx \frac{(n-1)V_i - nV_{o1} + V_{o2}}{n^2 L_r}\lambda T \end{aligned} \tag{12}$$

$$\lambda T = \frac{nV_{o1} - V_{o2}}{(n-1)V_i - nV_{o1} + V_{o2}}\varphi T \tag{13}$$

B. *Voltage Transfer Ratio*

According to the flux balance principle, the average voltage of leakage inductor L_r and magnetizing inductor L_m in a switching period is zero. Hence, V_{o1} is equal to the average drain-to-source voltage of S_2, which is denoted as $V_{s2,\text{ ave.}}$. From Fig. 3(b), $V_{s2,\text{ave}}$ is equivalent to dV_i. Therefore, the voltage transfer ratio of first output is depicted in (14), which is the same as conventional buck converter.

$$\frac{V_{o1}}{V_i}=\frac{V_{s2,ave}}{V_i}=d \tag{14}$$

Likewise, according to the current-second balance principle of output capacitor C_{o2}, (15) is obtained, in which I_{o2} is the load current of second output. Substituting (6), (7), (11) into (15), voltage transfer ratio of second output can be derived, as shown in (16).

$$\int_{t_3}^{t_4}[i_{D1}(t)-I_{o2}]dt+\int_{t_5}^{t_6}[i_{D1}(t)-I_{o2}]dt-I_{o2}(t_3-t_0)=0 \tag{15}$$

$$\frac{V_{o2}}{V_i}=\frac{-b-\sqrt{b^2-4ac}}{2a} \tag{16}$$

where $a=2n^2L_r$, $b=\varphi^2R_2T(n-1)+2n^2L_r(n-nd-1)$, $c=-\varphi^2R_2Tn(n-1)d$.

With the system parameters T=10μs, n=3, L_r=4.45μH and R_2= 120Ω, Fig. 4(a) shows the relationship between voltage transfer ratio and d~φ from (14) and (16). From Fig. 4, DC gain V_{o1}/V_i is only affected by duty cycle d, and V_{o2}/V_i is influenced by both φ and d. Therefore, duty cycle d is employed to control V_{o1} while φ is utilized to regulate V_{o2}, which can realize independent regulation for V_{o1} and V_{o2}. Besides, V_{o2}/V_i can be bigger or smaller than 1, which means second output is able to operate in both step-up and step-down occasions.

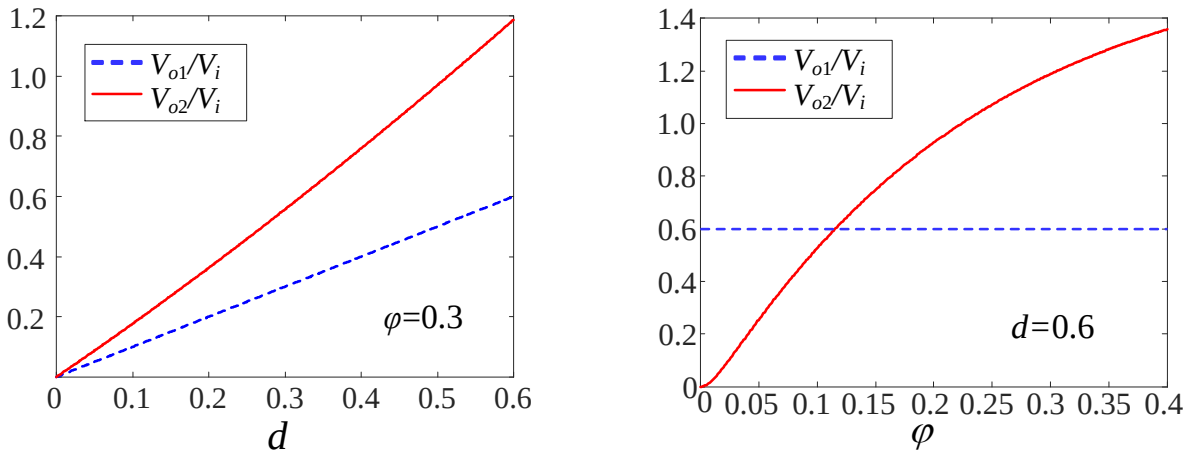


Fig. 4 Relationship between different parameters and voltage transfer ratio: (a) d and (b) φ

C. *Voltage and Current Stress of Power Device*

The turn-off voltage of S_1 and S_2 is clamped by input voltage V_i, which is identical to the conventional buck converter. The diode D_1 is reverse biased in the interval t_0-t_1, and its turn-off voltage is shown in (17). Likewise, the turn-off voltage across switch S_3 in the interval t_2-t_3 is given by (18).

$$V_{D1,\max}=\frac{L_m}{L_r+L_m}n(V_i-V_{o1})-V_i+V_{o2}\approx(n-1)V_i-nV_{o1}+V_{o2} \tag{17}$$

$$V_{s3,\max}=\frac{L_m}{L_r+L_m}nV_{o1}-V_{o2}\approx nV_{o1}-V_{o2} \tag{18}$$

The current stress of S_1 and S_2 can be derived from Fig. 3(b), as shown in (19) and (20). And $i_{s1}(t_5)$, $i_{s2}(t_4)$ are given in (21),

where $i_{Lr}(t_4)$ is shown in (22) from (4) and (6). Also, the average diode current I_{D1} is obtained in (23).

$$I_{s1,\mathrm{rms}} = \sqrt{\frac{\lambda}{3}(i_{s1}^2(t_5) + i_{s1}(t_5)I_{Lm} + I_{Lm}^2) + (d-\lambda)I_{Lm}^2} \tag{19}$$

$$I_{s2,\mathrm{rms}} = \sqrt{\frac{\varphi}{3}(i_{s2}^2(t_4) - i_{s2}(t_4)I_{Lm} + I_{Lm}^2) + (1-d-\varphi)I_{Lm}^2} \tag{20}$$

$$i_{s1}(t_5) \approx -i_{s2}(t_4) = \frac{n-1}{n} i_{Lr}(t_4) + \frac{1}{n} I_{Lm} \tag{21}$$

$$i_{Lr}(t_4) = I_{Lm} - \frac{nV_{o1} - V_{o2}}{nL_r}\varphi T \tag{22}$$

$$I_{D1} = \frac{1}{2}(\varphi+\lambda) i_{D1,\max} = \frac{\varphi^2 T}{2n^2 L_r} \frac{(n-1)V_i}{(n-1)V_i - nV_{o1} + V_{o2}} (nV_{o1} - V_{o2}) \tag{23}$$

D. Turns Ratio n

From above analysis, (5) and (10) must be satisfied to guarantee normal operation of the proposed converter. So the constraint of turns ratio n is derived from (5) and (10), as shown in (24).

$$n > \max\left(\frac{V_{o2}}{V_{o1}}, \frac{V_i - V_{o2}}{V_i - V_{o1}}\right) \tag{24}$$

E. Average Magnetizing Current I_{Lm} and Magnetizing Inductance L_m

The average leakage inductor current I_{Lr} is given in (25), where I_{o1} is the average output current of first output. From (25), the average magnetizing current I_{Lm} is also illustrated in (26).

$$I_{Lr} = I_{o1} = \frac{V_{o1}}{R_1} \tag{25}$$

$$I_{Lm} = I_{Lr} + nI_{D1} = I_{o1} + nI_{D1} \tag{26}$$

Based on the operation principle, the positive voltage is employed in the magnetizing inductor L_m in the interval t_0-t_1 and t_5-t_6. So the required magnetizing inductance L_m to achieve magnetizing current ripple ΔI_{Lm} is shown in (27)

$$L_m = \frac{[(1-d-\varphi)V_{o1} + \lambda\frac{V_{o2}}{n}]T}{\Delta I_{Lm}} \tag{27}$$

F. ZVS Condition and Reverse-Recovery Elimination

The parasitic capacitor C_{s2} is discharged by magnetizing current I_{Lm} in the interval t_1-t_2 as illustrated in Fig. 3(b). The energy required for ZVS operation is enough due to large magnetizing inductance L_m. Thus, the ZVS condition of S_2 is easy to achieve.

The parasitic capacitor C_{s1} is discharged during the resonant process t_4-t_5, as shown in (9). With the initial conditions $i_{Lr}(t_4) = I_{Lm} - (nV_{o1} - V_{o2})\varphi T / nL_r$ and $v_{s2}(t_4) = 0$, the solution of voltage $v_{s2}(t)$ is derived in (28). To achieve ZVS turn-on of S_2, v_{s2} should increase to V_i and thus v_{s1} can decrease to 0. Define the maximum of v_{s2} as $v_{s2,\max}$. Therefore, $v_{s2,\max}$ should be bigger than V_i, and thus (29) should be satisfied.

$$v_{s2}(t) = -V_c \cos\omega(t-t_4) - \sqrt{\frac{L_r}{C_s}}\left(\frac{1}{n-1} I_{Lm} + i_{Lr}(t_4)\right)\sin\omega(t-t_4) + V_c \tag{28}$$

$$v_{s2,\max} > V_i \quad \Leftrightarrow \quad Z_1 = L_r\left(\frac{1}{n-1} I_{Lm} + i_{Lr}(t_4)\right)^2 - C_s[(V_i - V_c)^2 - V_c^2] > 0 \tag{29}$$

where $\omega = \left(\frac{n-1}{n}\right)\frac{1}{\sqrt{L_r C_s}}$, $V_c = \frac{nV_{o1} - V_{o2}}{n-1}$

From operation principle, in order to eliminate the reverse-recovery problem, i_{s2} should turn to positive before S_2 is turned off at t_4, as shown in (30).

$$i_{s2}(t_4) = -\frac{1}{n} I_{Lm} - \frac{n-1}{n} i_{Lr}(t_4) > 0 \tag{30}$$

G. Small Signal Model

According to operation principle of the proposed converter, the average state space equation can be derived, as shown in (31). Besides, the average input current $\langle i_{in}(t)\rangle_T$ and average leakage inductor current $\langle i_{Lr}(t)\rangle_T$ are obtained in (32) and (33).

$$\begin{cases} L_r \dfrac{d\langle i_{Lr}(t)\rangle_T}{dt} + L_m \dfrac{d\langle i_{Lm}(t)\rangle_T}{dt} = d(t)\langle v_i(t)\rangle_T - \langle v_{o1}(t)\rangle_T \\ C_{o1} \dfrac{d\langle v_{o1}(t)\rangle_T}{dt} = \langle i_{Lr}(t)\rangle_T - \dfrac{\langle v_{o1}(t)\rangle_T}{R_1} \\ C_{o2} \dfrac{d\langle v_{o2}(t)\rangle_T}{dt} = \dfrac{\langle i_{Lm}(t)\rangle_T - \langle i_{Lr}(t)\rangle_T}{n} - \dfrac{\langle v_{o2}(t)\rangle_T}{R_2} \end{cases} \tag{31}$$

$$\langle i_{in}(t)\rangle = f_1(i_{Lm}, d, v_i, v_{o1}, v_{o2}) = \langle i_{Lm}(t)\rangle d(t) - \frac{[n\langle v_{o1}(t)\rangle_T - \langle v_{o2}(t)\rangle_T]^2}{2n^2 L_r[(n-1)\langle v_i(t)\rangle_T - n\langle v_{o1}(t)\rangle_T + \langle v_{o2}(t)\rangle_T]}\varphi^2(t)T \tag{32}$$

$$\langle i_{Lr}(t)\rangle = f_2(i_{Lm}, v_{o1}, v_{o2}, \varphi) = \langle i_{Lm}(t)\rangle - \frac{[n\langle v_{o1}(t)\rangle - \langle v_{o2}(t)\rangle](n-1)\langle v_i(t)\rangle}{2nL_r[(n-1)\langle v_i(t)\rangle - n\langle v_{o1}(t)\rangle + \langle v_{o2}(t)\rangle]}\varphi^2(t)T \tag{33}$$

In order to obtain small signal model of proposed converter, small perturbations are added in the quiescent operation point. From (31), (34) is obtained. Also, $\hat{i}_{in}(t)$ and $\hat{i}_{Lr}(t)$ can be represented by $\hat{v}_i(t)$, $\hat{v}_{o1}(t)$, $\hat{v}_{o2}(t)$, $\hat{\varphi}(t)$ through (32) and (33), which are depicted in (35) and (36). Parameters g_1, h_1, j_1, r_1, g_2, h_2, j_2, r_2, are given in (37) and (38).

$$\begin{cases} L_r \dfrac{d\hat{i}_{Lr}(t)}{dt} + L_m \dfrac{d\hat{i}_{Lm}(t)}{dt} = D\hat{v}_i(t) + V_i\hat{d}(t) - \hat{v}_{o1} \\ C_{o1} \dfrac{d\hat{v}_{o1}(t)}{dt} = \hat{i}_{Lr}(t) - \dfrac{\hat{v}_{o1}(t)}{R_1} \\ C_{o2} \dfrac{d\hat{v}_{o2}(t)}{dt} = \dfrac{\hat{i}_{Lm}(t) - \hat{i}_{Lr}(t)}{n} - \dfrac{\hat{v}_{o2}(t)}{R_2} \end{cases} \tag{34}$$

$$\hat{i}_{in}(t) = D\hat{i}_{Lm}(t) + I_{Lm}\hat{d}(t) + g_1\hat{\varphi}(t) + h_1\hat{v}_i(t) + j_1\hat{v}_{o1}(t) + r_1\hat{v}_{o2}(t) \tag{35}$$

$$\hat{i}_{Lr}(t) = \hat{i}_{Lm}(t) + g_2\hat{\varphi}(t) + h_2\hat{v}_i(t) + j_2\hat{v}_{o1}(t) + r_2\hat{v}_{o2}(t) \tag{36}$$

$$\begin{cases} g_1 = \dfrac{df_1}{d\varphi}\Big|_{\varphi=\psi} = -\dfrac{2(nV_{o1}-V_{o2})^2}{nA}\psi T \\ h_1 = \dfrac{df_1}{dv_i}\Big|_{v_i=V_i} = \dfrac{2(n-1)L_r(nV_{o1}-V_{o2})^2}{A^2}\psi^2 T \\ j_1 = \dfrac{df_1}{dv_{o1}}\Big|_{v_{o1}=V_{o1}} = -\dfrac{2(nV_{o1}-V_{o2})A+2nL_r(nV_{o1}-V_{o2})^2}{A^2}\psi^2 T \\ r_1 = \dfrac{df_1}{dv_{o2}}\Big|_{v_{o2}=V_{o2}} = \dfrac{2(nV_{o1}-V_{o2})A+2nL_r(nV_{o1}-V_{o2})^2}{nA^2}\psi^2 T \end{cases} \tag{37}$$

$$\begin{cases} g_2 = \dfrac{df_2}{d\varphi}\Big|_{\varphi=\psi} = -2\dfrac{B}{A}\psi T \\ h_2 = \dfrac{df_2}{dv_i}\Big|_{v_i=V_i} = -\dfrac{(nV_{o1}-V_{o2})(n-1)A-2nL_r(n-1)B}{A^2} \\ j_2 = \dfrac{df_2}{dv_{o1}}\Big|_{v_{o1}=V_{o1}} = -\dfrac{n(n-1)V_iA+2n^2L_rB}{A^2}\psi^2 T \\ r_2 = \dfrac{df_2}{dv_{o2}}\Big|_{v_{o2}=V_{o2}} = \dfrac{(n-1)V_iA+2nL_rB}{A^2}\psi^2 T \end{cases} \tag{38}$$

where $A = 2nL_r[(n-1)V_i - nV_{o1} + V_{o2}]$, $B = (nV_{o1} - V_{o2})(n-1)V_i$

From (35), (36) and (34), the small signal model of the proposed converter can be derived, which is shown in Fig. 6(a). And M_1 and M_2 are given in (39).

$$\begin{cases} M_1 = I_{Lm}\hat{d} + g_1\hat{\varphi} + j_1\hat{v}_{o1} + r_1\hat{v}_{o2} \\ M_2 = -\dfrac{1}{n}(g_2\hat{\varphi} + h_2\hat{v}_i + j_2\hat{v}_{o1} + r_2\hat{v}_{o2}) \end{cases} \tag{39}$$

V. Design Example and Experimental Results

In this section, a prototype circuit with system parameters in Table I is designed in this section according to the above analysis, and its experiment results are also demonstrated to validate the advantages.

Table I System parameters of prototype circuit

Input Voltage	V_i=100V
Output Voltages	V_{o1}=60V, V_{o2}=120V
Duty Cycle of S_1	d=0.6
Output Resistor	R_1=30Ω, R_2=120Ω
Output Current	$I_{o1,max}$=2A, $I_{o2,max}$=1A

A. Circuits Parameter Design

From Fig. 3(b), the maximum of φ and λ are limited by d to guarantee normal operation, as shown in (40).

$$\begin{cases} \varphi_{\max} < 1-d \\ \lambda_{\max} < d \end{cases} \tag{40}$$

From (16), φ is derived in (41). Also, λ can be calculated by (41) and (13), as shown in (42). According to (41) and (42), φ and λ increase with the increment of I_{o2}, and thus they achieve maximum value $\varphi_{\max}$ and $\lambda_{\max}$ when I_{o2} reaches its maximum value at full load condition. And $\varphi_{\max}$, $\lambda_{\max}$ are shown in Fig. 5(a). From Fig. 5(a), $\varphi_{\max}$ is always smaller than 0.4 and thus $\varphi_{\max}$<1-d can be always realized.

$$\varphi = \sqrt{\frac{2n^2 L_r[(n-1)V_i - nV_{o1} + V_{o2}]}{(n-1)(nV_{o1} - V_{o2})TV_i}}\, I_{o2} \tag{41}$$

$$\lambda = \sqrt{\frac{2n^2 L_r (nV_{o1} - V_{o2})}{(n-1)[(n-1)V_i - nV_{o1} + V_{o2}]TV_i}}\, I_{o2} \tag{42}$$

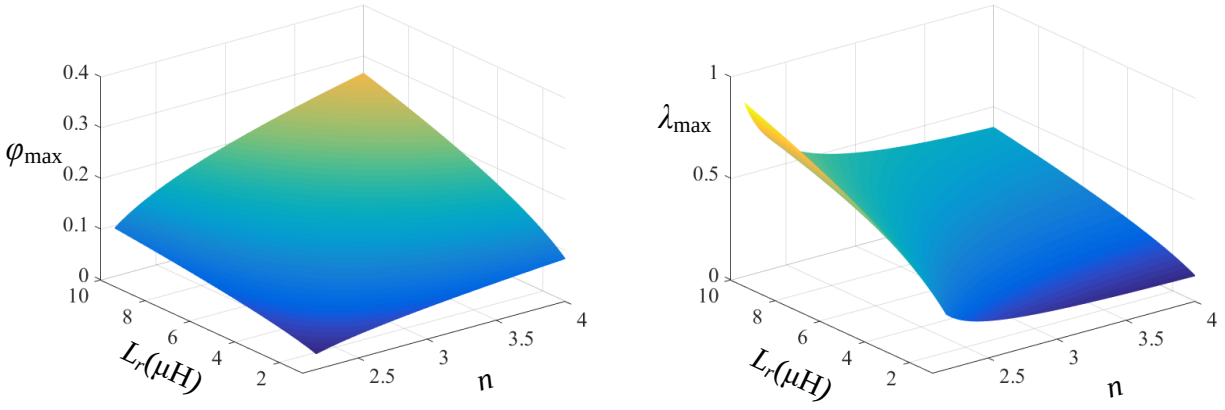
Meanwhile, the value of n and L_r also need to guarantee (29) and (30) to achieve the ZVS and eliminate reverse-recovery problem. By substituting (21), (23) and (26), (29) and (30) respectively turn into (43) and (44). Under 10%-100% load condition, the minimum of Z_1 and $i_{s2}(t_4)$ are defined as $Z_{1,\min}$ and $i_{s2t4,\min}$. Fig. 5(b) depicts the $Z_{1,\min}$ and $i_{s2t4,\min}$ under different n and L_r. From Fig. 5(b), $Z_{1,\min}$ is always larger than zero and thus ZVS can be always achieved.

$$Z_1 = L_r[m_2(\varphi - m_1)^2 + \frac{n}{n-1} I_{o1} - m_3]^2 - C_s[(V_i - V_c)^2 - V_c^2] > 0 \tag{43}$$

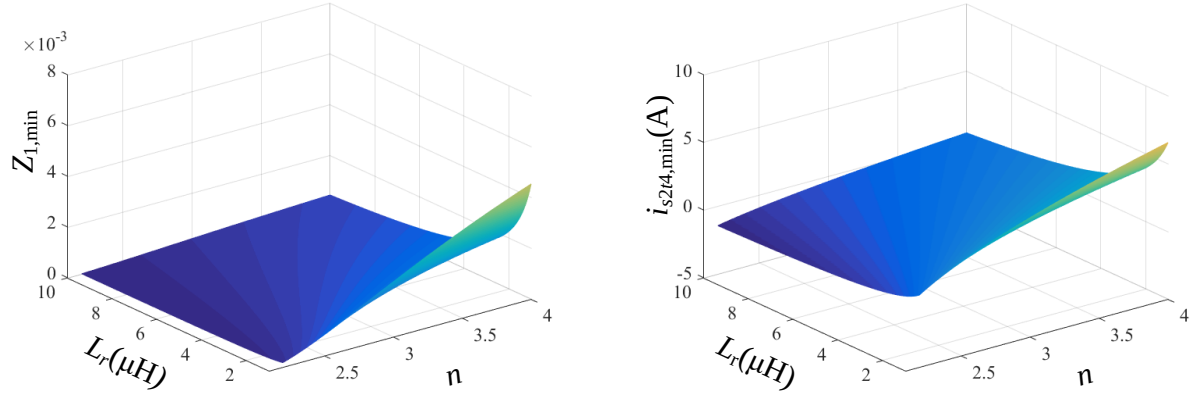
$$i_{s2}(t_4) = -(n-1)m_2(\varphi - \frac{m_1}{n})^2 + (n-1)m_3 - I_{o1} > 0 \tag{44}$$

where $m_1 = \dfrac{(n-1)V_i - nV_{o1} + V_{o2}}{nV_i}$, $m_2 = \dfrac{V_i(nV_{o1} - V_{o2})T}{2L_r[(n-1)V_i - nV_{o1} + V_{o2}]}$, $m_3 = \dfrac{[(n-1)V_i - nV_{o1} + V_{o2}](nV_{o1} - V_{o2})T}{2L_r n^2 V_i}$.

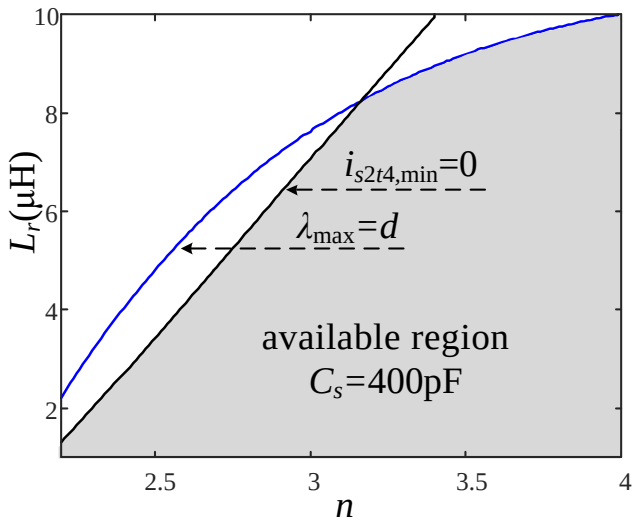
According to above analysis, the available region of n and L_r for achieving ZVS operation, eliminating the reverse-recovery problem and operating normally is illustrated in Fig. 5(c). Combining with the comprehensive consideration of voltage and current stress, n=3 and L_r=4.45μH which are in the available region, are chosen in the practical design. Choose ΔI_{Lm}=10%I_{Lm}, then L_m should be larger than 200μH from (27). In order to implement the coupled inductor, ferrite EE42 magnetic core is used. The turns of primary windings and secondary windings are 19 and 57, respectively. According to the analysis in section IV, voltage and current stress of semiconductor devices can be easily obtained that MOSFET IRFB4620 are chosen as S_1-S_3, while diode 8ETH03 is chosen as D_1. Meanwhile, output capacitators C_{o1} and C_{o2} are 330μF. The circuit parameters of experimental prototype are also summarized in Table II.



(a)



(b)



(c)

Fig. 5 The relationship among φ_{max}, λ_{max}, $Z_{1,min}$, $i_{s2t4,min}$, available region and n, L_r: (a) φ_{max} and λ_{max}, (b) $Z_{1,min}$ and $i_{s2t4,min}$, (c) available region

Table II Circuit parameters of experimental prototype

Input Voltage	V_i=100V
Output Voltages	V_{o1}=60V, V_{o2}=120V
Output Resistor	R_1=30Ω, R_2=120Ω
Output Capacitor	C_{o1}=C_{o2}=330μF
Turns ratio	N_p/N_s=1: n=1:3
The leakage inductor and magnetize inductor	L_r=4.45μH, L_m=210μH

B. Controller Design

As is discussed in circuit analysis, there are two control variables for two output voltages regulation that d is used to control V_{o1} and φ is chosen to regulate V_{o2}. From the small-signal model in Fig. 6(a), the control-to-output transfer function G_{v11} between $\hat{d}$ and $\hat{v}_{o1}$, G_{v22} between $\hat{\varphi}$ and $\hat{v}_{o2}$ are respectively derived in (45) and (46). With the parameters in Table II, bode plots of G_{v11} and G_{v22} are illustrated in Fig. 6(c) and Fig. 6(d). From Fig. 6(c) and Fig. 6(d), G_{v11} is unstable since the phase margin is zero and both output voltages suffer from steady-state errors. Therefore, compensators are required in the control-system to improve stability as well as static and dynamitic behavior of converter, as shown in Fig. 6(b).

$$G_{v11}=\frac{\hat{v}_{o1}(s)}{\hat{d}(s)}=\frac{B_1 s+B_0}{s^3+A_2 s^2+A_1 s+A_0} \tag{45}$$

$$G_{v22}=\frac{\hat{v}_{o2}(s)}{\hat{\varphi}(s)}=\frac{C_2 s^2+C_1 s+C_0}{s^3+A_2 s^2+A_1 s+A_0} \tag{46}$$

where $B_0=\frac{V_i}{(L_r+L_m)C_{o1}C_{o2}}(\frac{r_2}{n}+\frac{1}{R_2})$, $B_1=\frac{V_i}{(L_r+L_m)C_{o1}}$, $A_0=\frac{(r_2R_2+n)}{n(L_r+L_m)C_{o1}C_{o2}R_2}$, $A_2=\frac{r_2R_2+n}{nC_{o2}R_2}-\frac{j_2L_m}{(L_r+L_m)C_{o1}}+\frac{1}{R_1C_{o1}}$

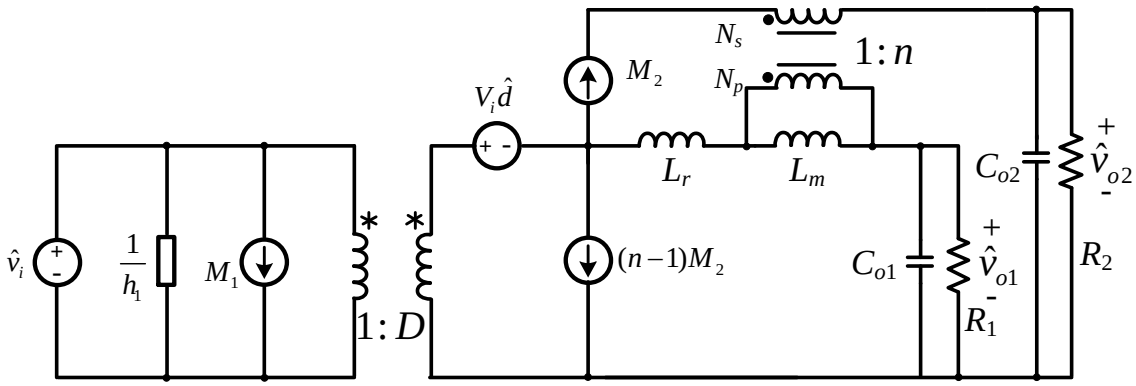
$A_1=-\frac{(j_2L_mR_1-L_m-L_r)(r_2R_2+n)}{n(L_r+L_m)C_{o1}C_{o2}R_1R_2}+\frac{1}{(L_m+L_r)C_{o1}}+\frac{j_2r_2L_m}{n(L_r+L_m)C_{o1}C_{o2}}$, $C_2=\frac{-g_2}{nC_{o2}}$, $C_1=\frac{-g_2}{nC_{o1}C_{o2}R_1}$, $C_0=\frac{-g_2}{n(L_m+L_r)C_{o1}C_{o2}}$

In order to increase the phase margin, a lead-lag compensation G_{c1} is added in the close-loop of $\hat{v}_{o1}$, as shown in (47). Meanwhile, simple proportion-integrator (PI) compensator G_{c2} in (48) is applied in close-loop system of $\hat{v}_{o2}$ to eliminate static error. Define the compensated open-loop transfer functions $G_{c1}\times G_{v11}$, $G_{c2}\times G_{v22}$ as G_{op1} and G_{op2}, respectively. Bode plots of compensators and compensated open-loop transfer functions with the parameters in Table II, are also depicted in Fig. 6(c) and Fig. 6(d). From Fig. 6(c) and Fig. 6(d), the phase margin of G_{op1} and G_{op2} are 31° and 55°, which means system achieve good stability and dynamic performance with the help of well-designed compensators. Besides, cross-regulation problem is effectively alleviated due to the independent control of $\hat{v}_{o1}$ and $\hat{v}_{o2}$. The above analysis is also validated in the following experiment results.

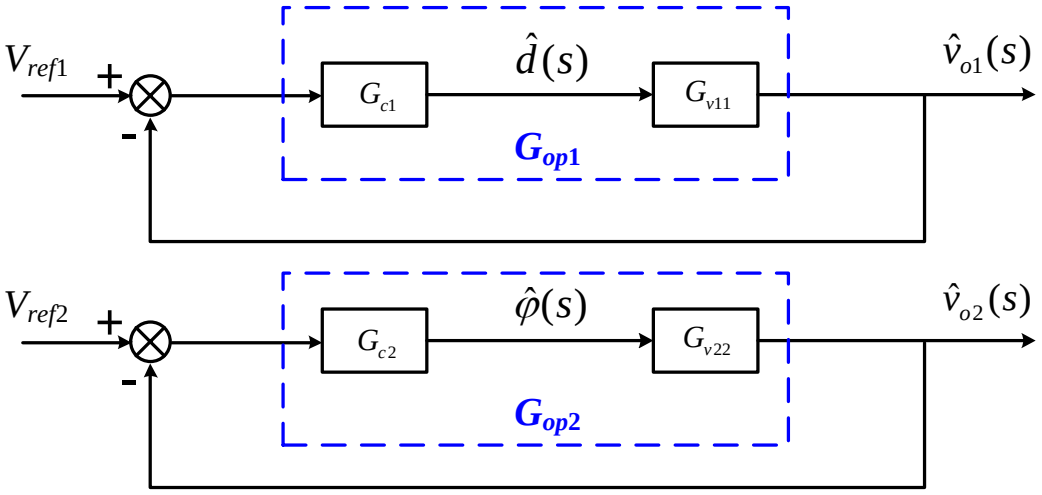
$$G_{c1} = \frac{K_{c1}(s/2\pi f_z + 1)(s/2\pi f_z + 1)}{s(s/2\pi f_p + 1)(s/2\pi f_p + 1)} \tag{47}$$

$$G_{c2} = 0.2 + \frac{10}{s} \tag{48}$$

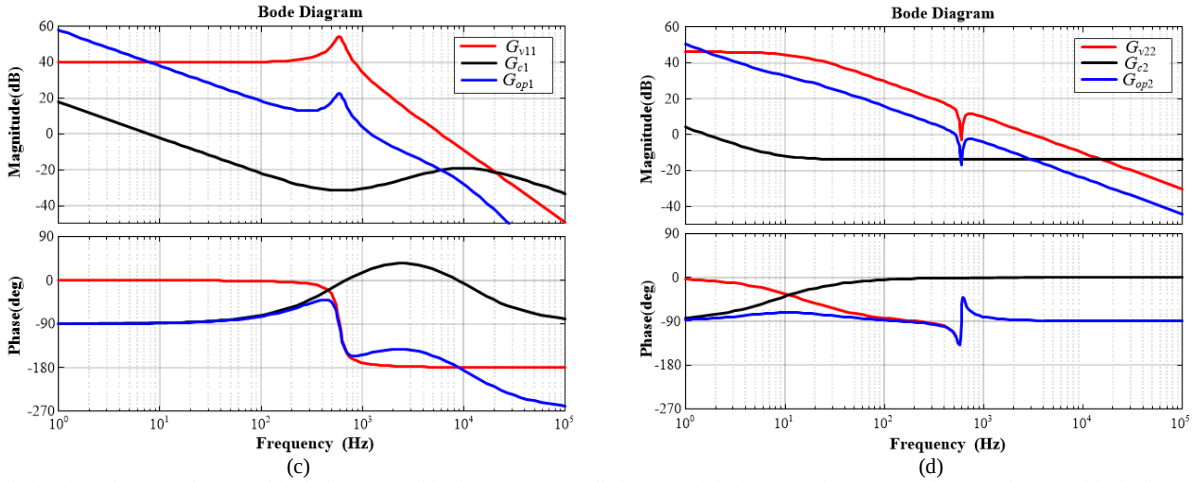
where $K_{c1} = 50$, $f_z = 600$, $f_p = 10000$.



(a)



(b)

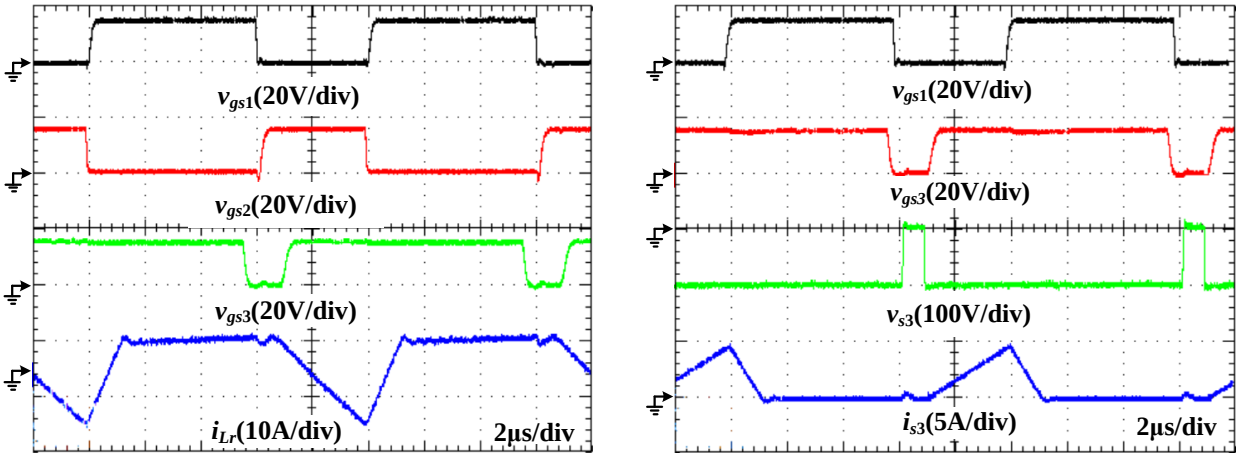


(c) (d)

Fig. 6 Small signal mode, control system block diagram and bode plots: (a) small signal model of proposed converter, (b) control system block diagram, (c) G_{v11}, G_{c1}, G_{op1} and (d) G_{v22}, G_{c2}, G_{op2}

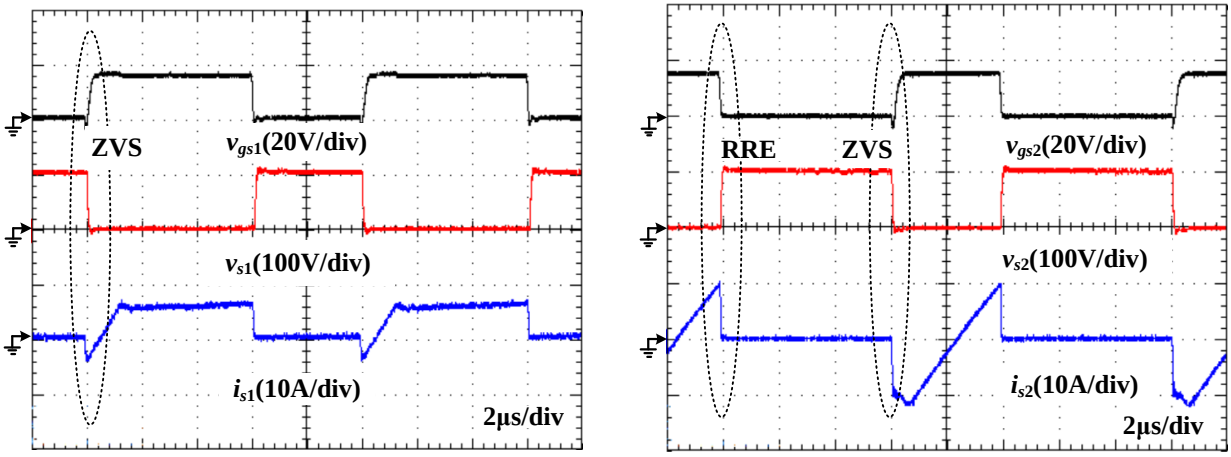
C. Experiment Results

The key operating waveforms at full load are depicted in Fig. 7, including drive signal $v_{gs1,2,3}$, the leakage inductor current i_{Lr}, the drain-to-source voltage v_{s3} and current i_{s3}. From Fig. 7(b), ZCS of S_3 is achieved because S_3 is turned off after i_{s3} decays to zero. Fig. 8 also shows drive signal, drain-to-source voltage and current of S_1 and S_2 under different load conditions. From Fig. 8, the ZVS operation of S_1 and S_2 as well as the reverse-recovery elimination (RRE) of S_2, are realized under 10%~100% load condition, which is in good agreement with analysis. Therefore, switching losses are greatly reduced over a wide range of load. And it also can be observed from Fig. 8 that the most difficult load condition to achieve ZVS operation of S_1 as well as RRE of S_2 is 100% load of first output and 10% load of second output.



(a) (b)

Fig. 7 Key operating waveforms: (a) $v_{gs1,2,3}$ and i_{Lr}, (b) v_{gs1}, v_{gs3}, v_{s3} and i_{s3}



(a)

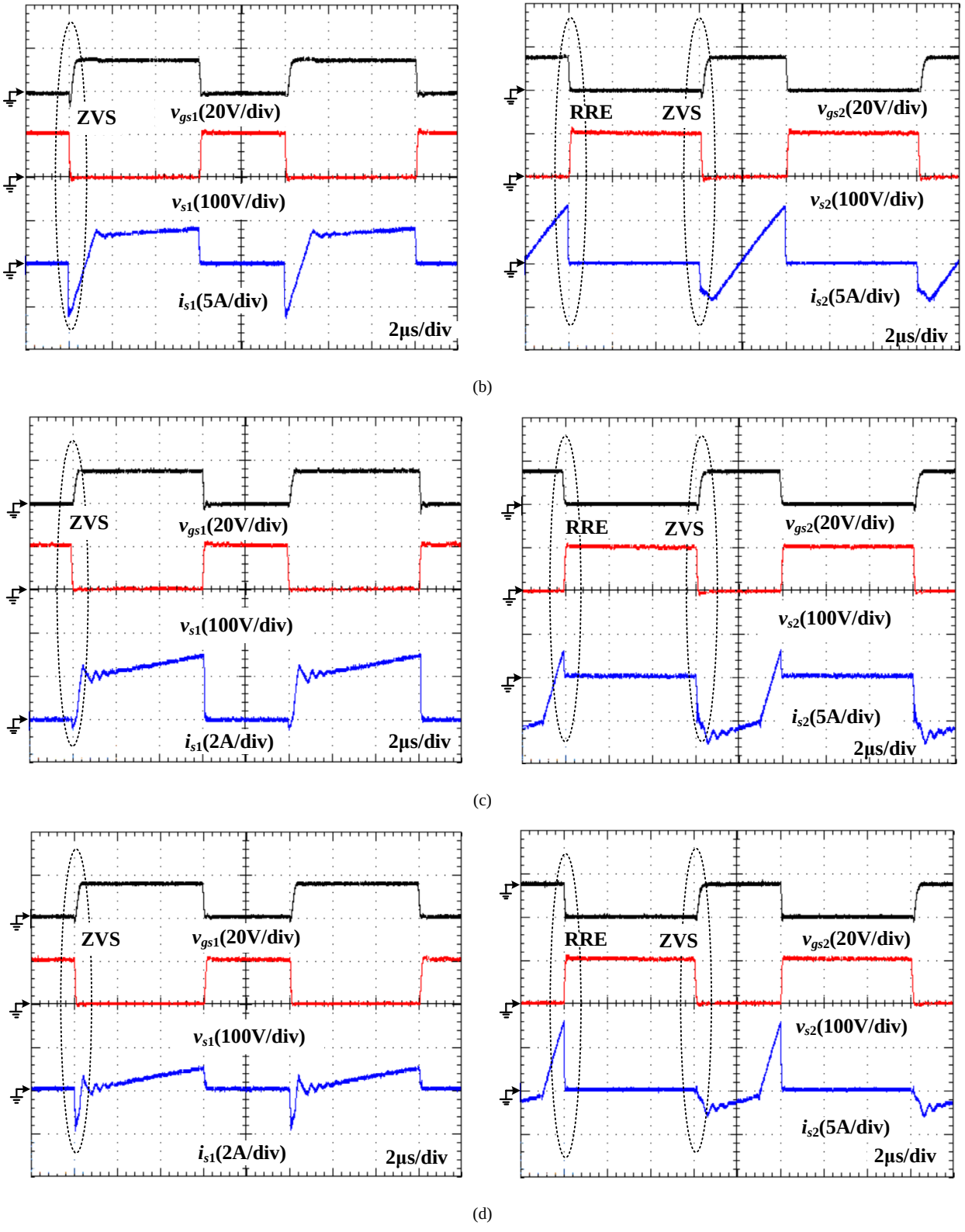
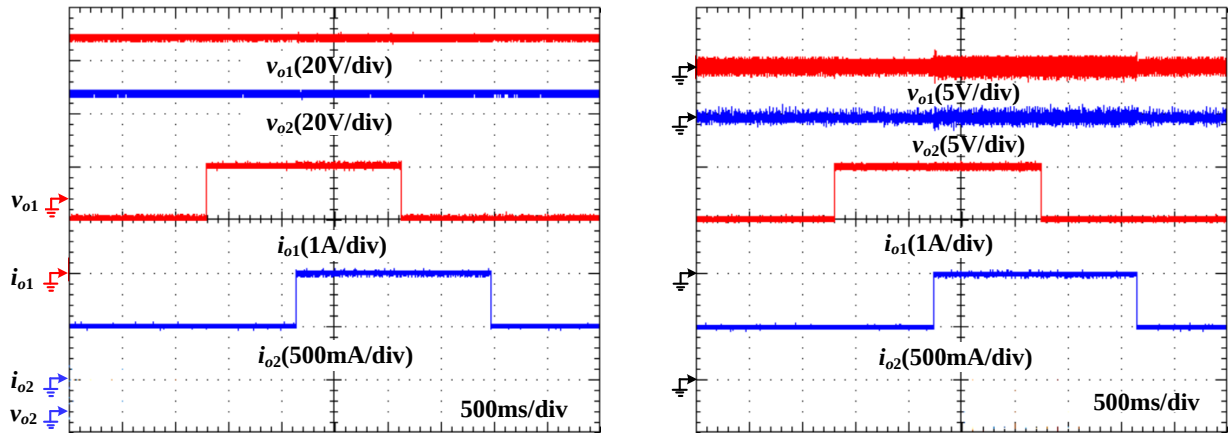


Fig. 8 ZVS operation of S_1 and S_2 under different load conditions (i_{o1}, i_{o2}): (a) (100% $I_{o1,max}$,100%$I_{o2,max}$), (b) (10% $I_{o1,max}$,100%$I_{o2,max}$), (c) (100% $I_{o1,max}$,10%$I_{o2,max}$) and (d) (10% $I_{o1,max}$,10%$I_{o2,max}$)

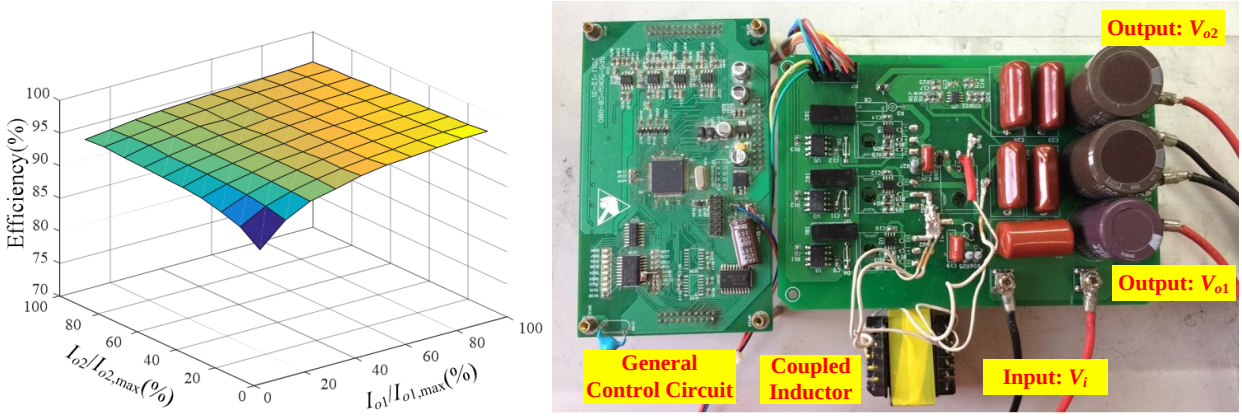
The transient response with load variation is given in Fig. 9(a) and Fig. 9(b). Output voltage $v_{o1,2}$ and current $i_{o1,2}$ in DC coupling is illustrated in Fig. 9(a). In order to observe detailed transient response of output voltages, $v_{o1,2}$ in AC coupling is shown in Fig. 9(b). From Fig. 9, the variations of output current i_{o1} and i_{o2} almost have no influence on output voltage v_{o1} and v_{o2}, and thus the

overall system achieves good dynamic responsibility and improved cross-regulation. Besides, measured efficiency over whole load range is shown in Fig. 10(a), which reaches the maximum 97.1% at 100% load of first output and 10% load of second output. And the efficiency under 100% load condition of both outputs is 95.3%. In addition, Fig. 10(b) depicts the photograph of proposed circuit.



(a) (b)

Fig. 9 Transient response with load variation (a) DC coupling and (b) v_{o1},v_{o2} in AC coupling



(a) (b)

Fig. 10 Efficiency and porotype:(a) results of efficiency measurement and (b) photograph of porotype circuit

VI. CONCLUSION

In this paper, a family of single coupled-inductor dual output soft-switching dc-dc converters was proposed, which is derived from the conventional SIDO converters. The proposed converters attain the following favorable advantages: (1) improved cross-regulation and dynamic performance, (2) reduced number of magnetic core and semiconductor device, (3) soft-switching operation. Therefore, lower cost and higher efficiency are obtained when compared with conventional SIDO converters. As an example, the proposed dual output converter based on buck converter is introduced in detail, including its operation principle and circuit analysis. Finally, a 60V/2A and 120/1A dual-output prototype converter was built to verify the effectiveness of proposed topology, which achieves both good dynamic characteristic and high power density.

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