On-silicon Supercapacitors with Enhanced Storage Performance

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The expanding development of portable electronic devices and ubiquitous sensing systems has created a strong demand for efficient miniaturized energy storage units, with planar geometries and capable of being integrated on a silicon platform. Generally, the performance of thin-film storage devices, including using graphene, is dramatically limited by their low surface area for ion-exchange. We had recently shown that a higher number of graphene layers does not translate into higher storage performance. Here we show a way to overcome this limitation and achieve a maximum accessible area for ion exchange. A repeated graphitization strategy using a nickel catalyst on epitaxial silicon carbide films on silicon yields few-layers graphenic nanocarbon electrodes with prominent edge defects, facilitating the intercalation between multiple graphenic sheets while maintaining overall a high electrode conductivity.

Keywords: Energy storage, Supercapacitors, Graphene, Silicon, Thin-film, Miniaturization

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1. Introduction

Efficient on-chip energy storage is nowadays the roadblock towards an ultimate miniaturization of complex microsystems [1, 2] necessary to extend the connectivity and autonomy of smart consumer portable devices, as well as to enable minimally-invasive wearable and endoscopic sensing for healthcare.[3, 4] At this stage, it is difficult to foresee an efficient solution, as advancement in energy storage technology is mostly based on large-scale fabrication and not compatible with planar geometries of on-silicon integration.[5]

Li-ion bulk and thin-film battery technologies have dominated the recent landscape of energy storage,[6, 7] however major drawbacks are in their high specific weight and their safety due to the high reactivity of lithium,[8] as well as the scarcity of the alkali metal in stark contrast to its growing demand.[9] On-wafer supercapacitors, fabricated directly on silicon wafer, would offer the most promising perspective for miniaturization and integration with current silicon technologies,[10] but they have limitations in terms of specific energy densities.[11, 12]

Similar to conventional energy storage devices, on-silicon supercapacitors require high-performance active materials. The most prominent type are carbon materials in a powder form, e.g. activated carbon and porous nanocarbon, [4] offering high specific surface areas with good cyclability though only moderate conductivities, and no faradic reactions.[13, 14] However, making carbon powders compatible with the planar geometry and fabricate on-chip energy storage is a complex process.[15] Active materials in a thin film form are a more appropriate alternative, as they can more easily be integrated onto substrates to fabricate planar devices.[1, 16] However, thin-film materials are typically far less efficient than powders, as ion-exchange can exclusively reach the small fraction of the active material that is exposed at its planar surface.[11] This limitation was exclusively overcome by the recent work of El-Kady et al, who demonstrated that light-scribed graphene thin-film electrodes with the highly accessible surface area on polymer substrates could improve the ion exchange rate and manifold energy density

compared to that of lithium thin film battery.[1, 17, 18] Nevertheless, this approach has challenges in terms of large-scale fabrication and reliability. It requires a complex handling of graphene oxide, which needs to be reduced with a laser source to produce serially each micro-capacitor, plus the use of materials like MnO_2 with potential faradic reactions and reduced reliability.[17] In order to enable a seamless integration with semiconductor technologies, a wafer-level fabrication using materials and processes compatible with silicon technologies would be highly desirable.

In a recent work, we presented a first attempt at SiC-derived graphene for application in on-silicon supercapacitors, showing a modest capacitance of up to 65 F g^{-1}.[19] This was obtained through a nickel-assisted graphitization process, yielding graphene onto a silicon carbide (SiC) surface. This technique has also been exploited to fabricate all-solid-state supercapacitors on silicon.[20] However, we pointed out that the synthesis of a thicker graphene was not translating into a higher capacitance, typical limitation of planar approaches. Realizing a highly porous underlying frame could potentially be a more effective alternative for harvesting ionic conductivity and electronic transport kinetics over a larger surface area.[21] However, SiC thin films are chemically resilient and mechanically robust,[22] making the creation of pores particularly challenging.

In this study, we enhance dramatically the accessible surface area of thin graphenic nanocarbon on SiC by using nickel diffusion, silicidation, and nickel-assisted graphitization to progressively intrude the SiC layer and simultaneously obtain highly conductive graphenic electrodes onto a porous frame. We demonstrate supercapacitors with energy densities of up to 0.15 Wh cm^{-3}. We also illustrate the essential role of tailoring the graphene thickness and defectivity to the underlying SiC roughness to obtain a consistent conductive path over the total surface, and at the same time, sufficient edges and discontinuities to enable ion diffusion in between graphenic sheets.

The process here described is fabricated on silicon using exclusively processes, materials and equipment routinely used in the semiconductor industry. This also implies that wafer-scale lithography can be used to define thousands of micro devices in a single step, making the upscaling to large wafer sizes straightforward as we have indicated in our earlier work.[23]

2. Experimental

An epitaxial 3C-SiC layer (500 nm) with an unintentional n-type doping of 10^{16}–10^{17} cm^{-3} was initially grown on a Si (100) wafer.[24] A thin nickel film (~2 nm) was sputtered onto this 3C-SiC/Si wafer by using a DC Ar^{+} ion sputterer (deposition current of 100 mA and a base pressure of 8×10^{-2} mbar) and transferred into a tube furnace. The coated 3C-SiC/Si wafer was annealed for 2 h under vacuum with a temperature ramping rate of ~25 °C min^{-1} at 1000-1200 °C. The graphitized samples were allowed to cool down to room temperature and immersed in Freckle solution (70:10:5:5:10 – 85% H_3PO_4: Glacial acetic acid: 70% HNO_3: 50% HBF_4: H_2O) overnight to eliminate nickel silicides and unreacted nickel.[23] The obtained samples were denoted as Phase 1 product and the entire synthesis processes were then repeated once and twice to yield Phase 2 and Phase 3 products.

Raman Spectroscopy of all samples was recorded on a Renishaw spectrometer with a laser excitation at 514 nm on five different spots of the surface. XPS was performed in an ultrahigh vacuum system to acquire the chemical compositions by utilizing a non-monochromatic Mg Kα (1253.6 eV) X-ray source (DAR 400, Omicron Nanotechnology), 300W incident angle at 65° to the sample surface, with a 125 mm hemispherical electron energy analyser (Sphera II, 7 channels detector, Omicron Nanotechnology). Photoelectron data were captured at a take-off angle of 90° and the high-resolution scans were carried out at 20 eV pass energy with 0.2 eV steps and 0.2 s dwell time. The surface morphology of all samples was revealed by SEM on a JEOL JSM6510-LV facility. Cross-sectional features of the sample F1200-3 were investigated by using TEM with a FIB lift-out technique. The sample was shielded with a 5 keV e-beam

deposited platinum cap to retain the initial surface integrity prior to ion milling. The preparation of samples was then performed by FIB milling with a Ga ion beam at 30 keV to a thickness of ~1 µm followed by polishing using an Ar^+ ion beam at 500 eV to polish off the Ga ion damage and to obtain electron transparency for high-resolution imaging. Then the sample was placed into an FEI Titan Cs-corrected TEM instrument operated at 80 keV. To obtain the surface texture on all samples, AFM scans were conducted by using an NT-MDT Integra spectra system.

Two identical samples (1×2 cm^2) were assembled face-to-face with a reference Saturated Calomel Electrode (SCE) in a three-electrode configuration. One sample was selected as the working electrode, and the other as the counter electrode. A glass microfiber membrane was used as the separator (GF/B, Whatman) to prevent short circuit. All electrochemical measurements were conducted on an Electrochemistry Workstation (CHI660E) in the presence of a 3 M KCl aqueous electrolyte. The CV tests were carried out in a voltage range of -0.2 to 0.8 V (against SCE) from 10-100 mV s^{-1}. Galvanostatic charge-discharge (GC) performance was evaluated at current densities of 3-10 µA cm^{-2}. The cyclic stability of sample F1200-3 was examined at the current density of 10 µA cm^{-2} for 10,000 cycles. EIS was performed at a frequency range of 100 kHz to 100 mHz with an amplitude of 10 mV.

3. Results and Discussion

A schematic diagram of our repeated graphitization strategy is represented in **Figure 1(a)**, which depicts the mechanism of controlled structuring of SiC and simultaneous growth of graphitic carbon. The 3C-SiC/Si wafer acts as template and source of carbon for graphitization. First, 2 nm of nickel is sputtered on the epitaxial 3C-SiC layer on Si wafer. The nickel metal reacts during annealing with SiC to form metal silicides, releasing free atomic carbon which produces a graphitic carbon network at the metal-SiC interface. The nickel silicide and residual

metal are then etched away by using a Freckle solution, leaving the graphitic carbon network on a highly rugged SiC surface.[25] The obtained samples are indicated as Phase 1 product. The entire synthesis process is then repeated to obtain Phase 2 and Phase 3 products. Graphenic nanocarbon is therefore grown onto a progressively roughened and porous SiC surface. We name the produced samples according to their graphitization temperature and phases as F1000-3 (1000 °C, Phase 3), F1100-3 (1100 °C, Phase 3), F1200-1 (1200 °C, Phase 1), F1200-2 (1200 °C, Phase 2), and F1200-3 (1200 °C, Phase 3), respectively. These nanocarbon samples are later assembled in a symmetric double-layer supercapacitor cell, as shown in **Figure 1(b)**. Raman spectra of all samples are shown in **Figure 2(a)**. The three prominent peaks in the Raman spectra represent the D band (~1350 cm^{-1}), G band (~1580 cm^{-1}) and 2D band (~2700 cm^{-1}), which are indicative of defects, in-plane vibration of sp^2 carbon atoms, and second harmonic of D band, respectively, confirming the presence of graphenic nanocarbon in all our samples.[26-28] It is worth noting that the G band exhibits two shoulder peaks. One, around 1621 cm^{-1} is commonly known as the D´ band. Both the D and D´ peaks are indicative of structural disorder in the sp^2 network of carbon,[29] and they appear more intense for the samples processed at higher temperatures. The second, around 1526 cm^{-1}, is not generally promptly observed and has been reported as related to graphenic fragments vibration.[30] This second peak likely indicates the appearance of more prominent discontinuities in the graphenic layers as samples are produced at high temperatures and through an increasing number of cycles. In addition, the intensity ratio of the D band and G band (I_D/I_G), is 0.88, 0.99, 1.46, 1.5 and 1.69 for sample F1000-3, F1100-3, F1200-1, F1200-2 and F1200-3, respectively (**Table 1**). A higher I_D/I_G value indicates a greater amount of defects in the layers,[31] and sample F1200-3 has the highest ratio, which we attribute to the presence of functional groups within the sp^2 carbon network as well as to an extensive presence of graphenic edges/discontinuities, as indicated by the shoulder peak at ~1530 cm^{-3} (**Figure 2(a)**).

The graphitization process leads to very few layer graphenic nanocarbon on the SiC substrate, as suggested by a detailed analysis and fitting of the 2D Raman bands (**Figure S2, Supporting Information**).[32] The FWHM of the 2D band of the F1000-3 and F1200-1 samples is ~55 and 50 cm^{-1}, respectively, while the single Lorentzian peak indicates a prevalence of mono- to bilayer graphenic nanocarbon (**Table 1**). On the other hand, the 2D band of F1100-3 and F1200-2 show an FWHM value of 60 and 61 cm^{-1}, and can be fitted by at least two Lorentzian peaks, indicating rather 3-4 layers of graphenic nanocarbon. Finally, the 2D peak of the F1200-3 sample shows a considerably larger FWHM of 77 cm^{-1}, plus a slightly asymmetric shape due to the incipience of a shoulder towards higher wavenumbers, indicating a thicker graphenic nanocarbon of about 5-6 layers.[33, 34] For an even thicker graphenic carbon, this shoulder would comparatively increase and gradually lead to a blueshift of the 2D band to match that of HOPG.[33, 34] However, the graphenic carbon has small crystallite size as our samples have considerable I_D/I_G values. Tuinstra-Koenig law gives a clear measurement of crystallite size by considering I_D/I_G ratio and excitation laser energy and can be expressed by Equation.[35]

$$L_a = (2.4 \times 10^{-10}) E^4 \left(\frac{I_G}{I_D}\right) \quad (1)$$

Where, L_a is the crystallite size and E is excitation laser energy (in our case, E is 2.41 eV for 514 nm of excitation wavelength). Our all samples (**Table 1**) shows high I_D/I_G, which clearly indicates small crystallite sizes and the calculated values of L_a ranges from 10 to 18 nm.

To examine the sample morphology, we performed cross-sectional Transmission Electron Microscopy as shown in **Figure 2(b)** for sample F1200-3. A platinum capping layer was deposited on the top of the sample as protection upon preparation for TEM. This protective layer filled the valleys of the rugged SiC surface as highlighted with a dashed line. Note that no evident graphenic layer can be distinguished in the TEM image, due to the few-layer nature of graphenic carbon on a highly rough and porous underlying surface.

Top-down Scanning Electron Microscopy images of all samples are shown in **Figure 3**, revealing a significant morphological difference and a progressively increasing roughened surface. While the samples graphitized at 1000 °C (Phase 1 through to Phase 3) exhibit similar surface morphology (**Figure 3(a)**, **(b)**, and **(c)**), the samples graphitized at 1100 °C start showing gradually more surface pores as the graphitization is repeated (**Figure 3(d), (e)** and **(f)**). At 1200 °C (**Figure 3(g)**, **(h)**, and **(i)**), large pores appear, together with the occurrence of progressively more pronounced "cracks". This all suggests a gradually increasing diffusion of nickel and intrusion of nickel silicides in the SiC as the graphitization temperature is increased and the cycles are repeated, also leading to a strongly enhanced surface area for the graphenic nanocarbon coating. This is also confirmed by roughness measurements with atomic force microscopy (AFM), as reported in **Table 1** and **Figure S3**.

The full cyclic voltammetry [6] curves of F1000-3, F1100-3, F1200-1, F1200-2, F1200-3 and the reference 3C-SiC/Si samples are shown in **Figure S4**. All electrodes demonstrate a rectangular shape at scan rates of 10-100 mV s^{-1}, supporting a typical double-layer storage mechanism. In addition, the CV curves maintain their shape at each scan rate, revealing a highly reversible charge/discharge response and excellent rate capability. It is worth noting that all the samples showed minimal distortion with increasing scan rates. This indicates a fast and efficient kinetics of electron transportation in the electrode materials and excellent ion adsorption–desorption process at the electrode/electrolyte interface.[36] The CV curves of F1200-3 cover the largest area, indicating the best capacitive performance, and are compared to the bare SiC reference in **Figure 4(a) and (b)**.

The galvanostatic charge-discharge (GC) curves of F1200-3 and the reference sample are shown in **Figure 4(c) and (d)**. The curves show very regular shapes, indicating an ideal capacitor behavior. F1200-3 demonstrates again the best performance (the longest discharge time) (**Figure S5**), with no significant potential (IR) drop, suggesting high reversibility and

cycling capability.[37] Note that there is a small plateau at the charge curves above 0.7 V, which may relate to the minor electrolysis of water, causing a low Coulombic efficiency. The calculated capacitance of F1200-3 and the reference bare 3C-SiC/Si sample are 176 and 92 μF cm^{-2}, respectively, based on the discharge process at 3 μA cm^{-2}. The galvanostatic capacitance data for all samples are also compared in **Table 1**.

The internal resistance of the best -performing graphene sample and that of the reference bare SiC sample are compared via Electrochemical Impedance Spectroscopy (EIS), in **Figure 4(e)**. In the high-frequency region, the values of the intercept with the real part axis represent the intrinsic ohmic resistance or equivalent series resistance of the electrode and electrolyte.[38] The graphenic electrode shows a considerably lower resistance than the reference. The nearly vertical slopes in the low-frequency region of the Nyquist plot in **Figure 4(e)** indicate an ideal capacitor behavior. The graphenic electrodes also show stability upon long-term cycling, as shown in **Figure 4(f)** (current rate of 10 μA cm^{-2}). Overall, a capacitance retention of 83.2% is obtained for 10,000 continuous charge-discharge cycles. The F1200-3 electrode experiences a sharp decline over the first 1,000 cycles, which we attribute to the mechanical fragility of the highly porous structure, while maintaining excellent cycling stability (retention approaching 93%) throughout the remaining 9,000 cycles.

Table 1 compares the information from Raman spectroscopy, roughness measurements (shown in **Figure S3**), and area capacitance of all graphenic nanocarbon samples and the reference. All graphenic nanocarbon samples have better area capacitance than the reference 3C-Si/Si. Among the five prepared nanocarbon samples, F1200-3 yields consistently the highest area capacitance. F1200-3 also shows the highest roughness (88 nm RMS), which translates into the largest total surface area (**Figure S3**).

However, we show that surface area alone is not sufficient to explain the enhanced capacitance. We specifically evaluate the role of the graphenic nanocarbon in the overall electrochemical

performance, using an oxygen plasma etching (30 min) to remove the carbon layer from F1100-3 and comparing its performance with and without the graphenic overlayer component. Raman spectroscopy on the plasma-etched sample confirms the complete removal of graphenic carbon, as the D, G and 2D peaks of graphene are absent, **Figure 5(a)**. The plasma-etched sample shows low electrochemical performance, very close to that of the reference bare silicon carbide (**Figure 5(b) and (c)**), delivering a similar area capacitance regardless of its substantially higher roughness (by a factor 2-3, **Table 1**). This experiment demonstrates that the roughening of the SiC surface alone is not sufficient to enhance the capacitive performance, as it is the graphenic nanocarbon that makes a crucial contribution to the double layer capacitance.

The graphenic nanocarbon produced via repeated processing at high temperatures leads to an increasing amount of defects, edges, and as a consequence, to the incorporation of more oxygen functional groups (**Figure S1 and Table S1**), preferably at the edge sites as in shown in the schematic in **Figure 6(a)**. The effects of functional groups, such as C=O, C-O, on the electrochemical performance have been reported in the literature for acidic and alkali electrolytes,[39-42] where redox reactions occur and involve the interactions of H^+ or OH^- with functional groups. Since all of the electrochemical tests were performed in a neutral electrolyte (3 M KCl) and no redox peaks were observed on the CV curves, we exclude significant contributions by the oxygen groups to the capacitance.

Comparing the characteristics and capacitance performances of the samples in **Table 1**, we can reach the following conclusion. To reach a maximum available active ion-exchange area and thus a maximum capacitance, an optimal combination of a large surface area covered by a consistently efficient conductive path is necessary. Surface roughening increases the total available area but proves ineffective when it is not continuously covered by a highly conductive graphenic overlayer.

From F1000-3 and F1100-3, **Table 1,** we learn that repeated graphitizations at 1000 and 1100 °C lead to a roughening from ~10 of the bare SiC, to about 20 nm RMS. We see that 1-2 layer graphenic nanocarbon are likely subcritical for obtaining full surface coverage, so the thicker graphenic layer (3-4 layers) of F1100-3 leads to higher coverage and thus capacitance. A dramatic roughening of the SiC film takes place for repeated graphitization at 1200 °C (F1200 -1, -2 and -3, Table 1), reaching almost 90 nm RMS after 3 cycles. The graphenic layer grows thicker as the cycles are repeated, and its defectivity increases, as indicated by an increasing Raman I_D/I_G ratio. The 5-6 graphenic sheets composing the active overlayer in F1200-3, the best–performing sample, are thus highly defective and discontinuous.

So, first of all, we learn that the thicker nature of the graphenic sheets helps towards sufficient coverage by a conductive path of the large surface area of F1200-3. Secondly and equally importantly, this sample can further enhance the amount of active carbon sites that are accessible by the electrolyte ions through its prevalent edges and sheet discontinuities. This concept is illustrated in the schematic in **Figure 6(b)**.

Therefore, we can conclude that obtaining a large porous area consistently covered by several discontinuous graphenic layers help to achieve a maximum nanocarbon active area for ion-exchange and therefore a maximum supercapacitive performance. On the other hand, in the presence of a better quality graphene covering a smooth surface as we discussed earlier,[19] a thicker graphenic layer does not lead to improved capacitance.

Energy (*E)* and power density (*P*) are the key parameters to be considered for practical energy storage applications:

$$E = \frac{1}{2} C(\Delta V)^2 \quad (2)$$

$$P = \frac{E}{\Delta t} \quad (3)$$

Where, E (Wh cm^{-3}), C (F cm^{-3}), ΔV (V), Δt (s), and P (W cm^{-3}) are energy density, specific capacitance, potential window of discharge, discharge time, and power density, respectively. Based on the 5-6 layers carbon estimate, our best performing sample demonstrates a substantially higher energy density (~0.12-0.15 Wh cm^{-3}) than all carbon and laser-scribed graphene supercapacitors,[43-46] while delivering an outstanding power density (7.5-9.0 W cm^{-3}). We have also estimated the energy density and power densities in terms of electrode area. Our best performing sample demonstrates an areal energy density of ~2.5 μWh cm^{-2} and power density of ~ 16-μW cm^{-2}. Note, however, that meaningful areal densities for an actual device will have to be evaluated in an interdigitated 2D or 3D geometry, which will cause the cited areal density figures to increase substantially (see supporting information).

Note that our graphitized 3C-SiC samples can also be implemented for interdigitated structures to achieve wafer-level fabrication of micro-supercapacitors. The interdigitated configuration possesses various advantages, such as on-silicon integration compatibility in a planar geometry, much reduced ion transportation path, elimination of separator, and feasibility to grow in 3D pattern to increase the total electrode area per unit area.[43] Based on our estimation in Figure S6, with the high resolution mask design, we can create ion diffusion paths of as short as 2 μm; with a thick SiC layer of 20 μm,[47] we can achieve at least 11 times greater area capacitance in a 3D interdigitated structure than that in 2D per unit electrode pair, due to the increased electrode area. Hundreds of unit electrode pairs located within the same unit area could contribute to a few orders of magnitude improvement of area capacitance, resulting in a much enhanced energy density. Additionally, by using a non-aqueous solid or gel electrolyte, the Columbic efficiency of the micro-devices can be further improved. Therefore, exploiting structural advantages by microfabrication technology in an interdigitated design could be pivotal to achieve enhanced performance for our on-silicon graphene or graphenic carbon

samples, in terms of both energy and power density, and this will be further investigated in our follow-up work.

4. Conclusion

We demonstrate a highly enhanced supercapacitive performance of thin graphenic nanocarbon, directly synthesized from a SiC film on silicon, leading to energy densities of up to ~0.12-0.15 Wh cm^{-3}, corresponding to areal energy densities of up to ~2.5 µWh cm^{-2} for a simple, unpatterned configuration, while delivering outstanding power densities. We credit this enhanced performance to the achievement of a maximum total ion-exchange surface for the graphenic nanocarbon electrodes through 1) the realisation of a highly porous underlying frame increasing the total electrode surface area, and 2) the prominent presence of edge –type discontinuities in the graphenic sheets, allowing for electrolyte ions to easily and extensively intercalate, and also promptly leave the sheets. This approach greatly extends the limits we encountered with a less defective graphene over a smoother SiC surface, where multiple graphenic layers were not yielding a higher capacitance.[19] Note that the preserving a consistent highly conductive electrode surface while introducing defects in the graphene is paramount. These concepts will offer great opportunities to develop complex micro-supercapacitor shapes using a straightforward patterning approach for miniaturized applications,[23] but may also be of guidance towards enhancing the performance of macroscopic supercapacitors based on bulk graphenic material, with countless potential benefits from electric transport to renewable energies.

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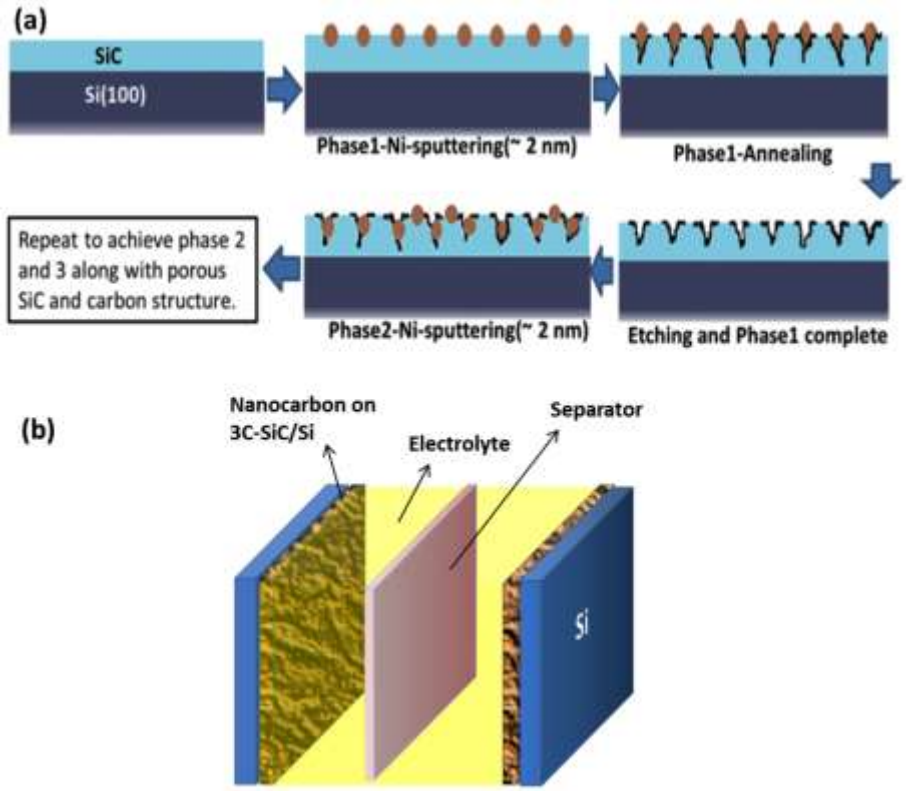

Figure 1. (a) A schematic diagram of the processing strategy to achieve graphenic nanocarbon simultaneously onto a porous underlying frame made of silicon carbide through repeated cycles of sputtering, annealing and etching and (b) diagram of the on-chip double-layer supercapacitor cell structure adopted for this study.

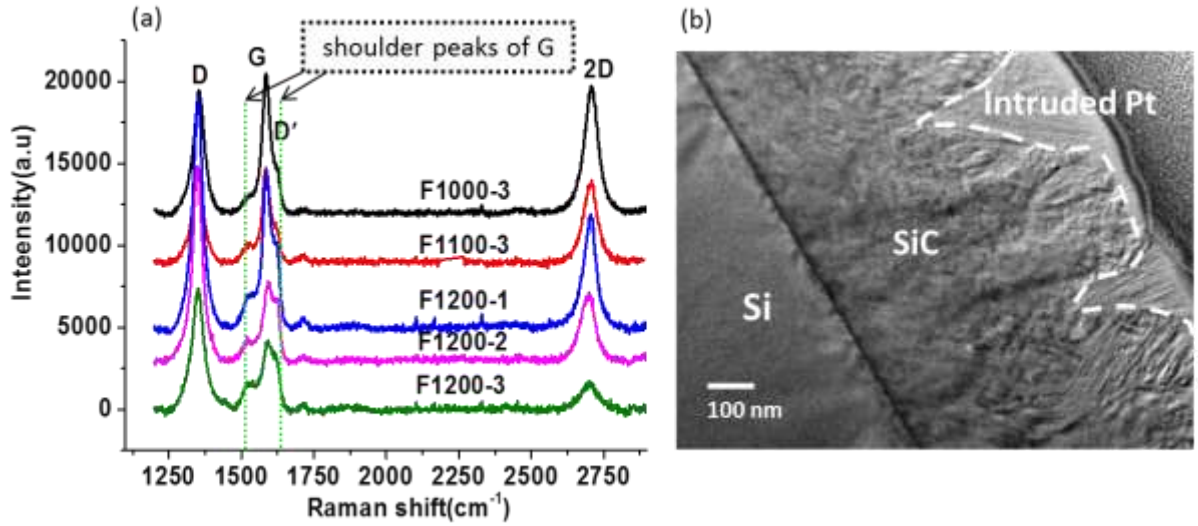

Figure 2. (a) Raman spectra of all graphenic samples, showing characteristic D, G and 2D peaks of graphene, plus two shoulder peaks of interest for the G band, including the D', and (b) A cross-sectional TEM image of the best -performing sample (F1200-3), showing the rugged profile of the top silicon carbide surface with deep dents or open porosity which largely enhance the total surface of the sample. The true surface profile is indicated by the white dashed line.

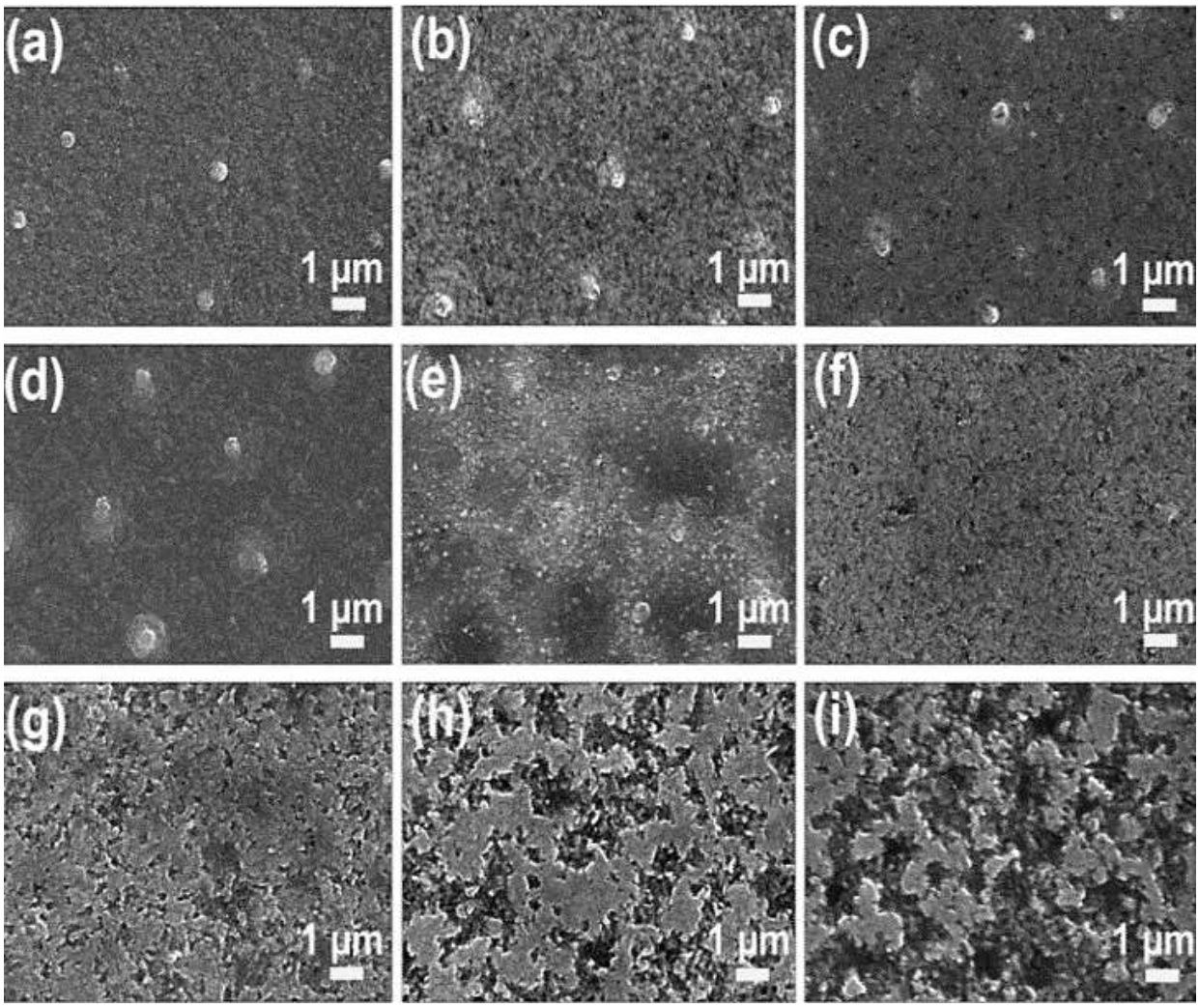

Figure 3. Scanning electron microscope images of samples at (a) Phase 1, (b) Phase 2, (c) Phase 3 after graphitization at 1000 °C; (d) Phase 1, (e) Phase 2, (f) Phase 3 after graphitization at 1100 °C; (g) Phase 1, (h) Phase 2, (i) Phase 3 after graphitization at 1200 °C, respectively. Increasing temperature and number of graphitization/etching cycles lead to progressively higher surface roughness.

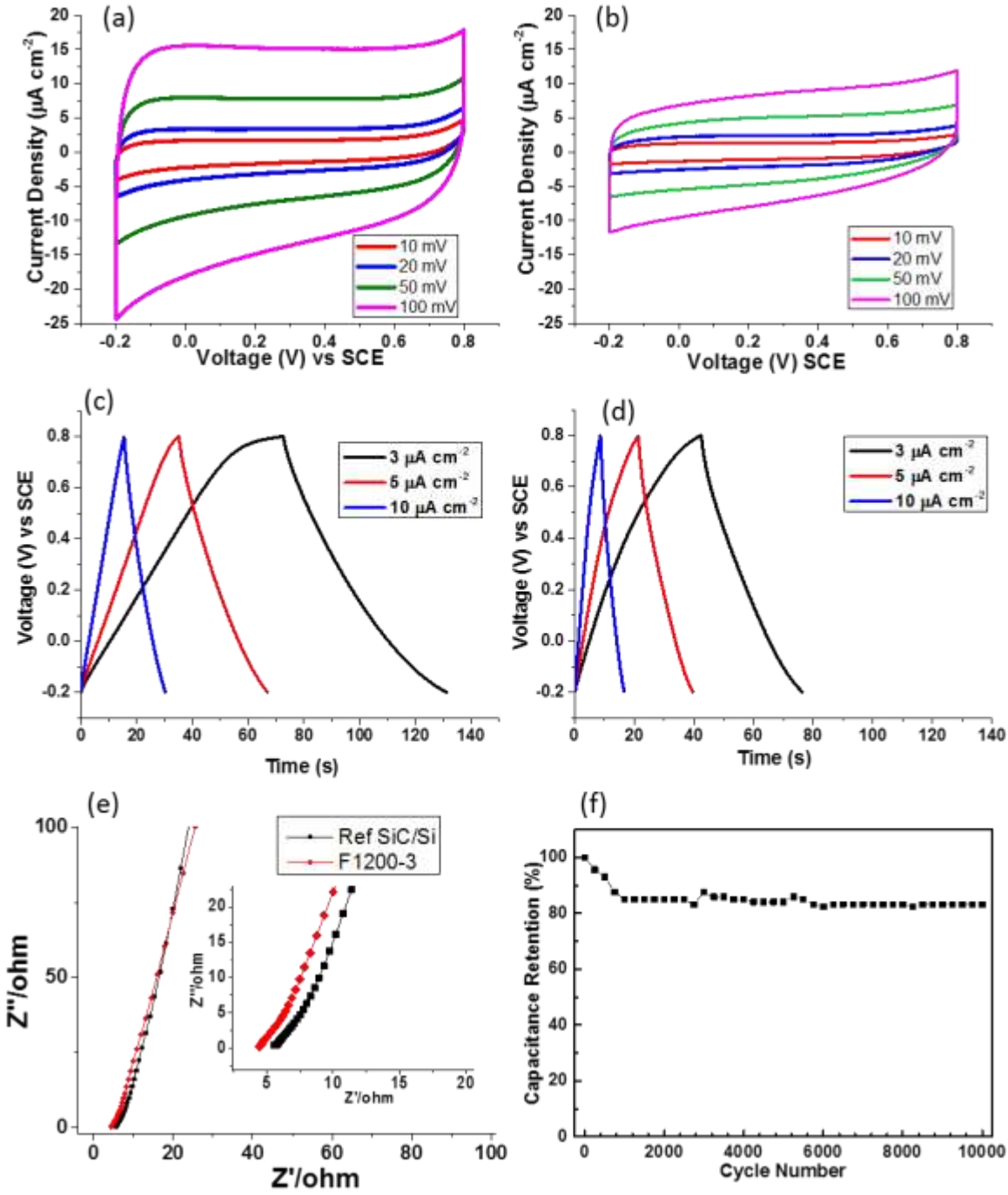

Figure 4. Supercapacitive performance comparison through CV curves of (a) F1200-3, the best -performing graphenic condition and (b) the reference bare silicon carbide on silicon (measurements in 3 M KCl at scan rates of 10-100 mV s^{-1}). Equivalent comparison this time through galvanostatic charge-discharge curves of (c) F1200-3 and (d) reference 3C-SiC/Si samples, (e) Nyquist plots of F1200-3 and reference, showing considerably lower transfer resistance for the graphenic sample and (f) long-term charge/discharge cycling test of the graphenic sample at a current rate of 10 μA cm^{-2}.

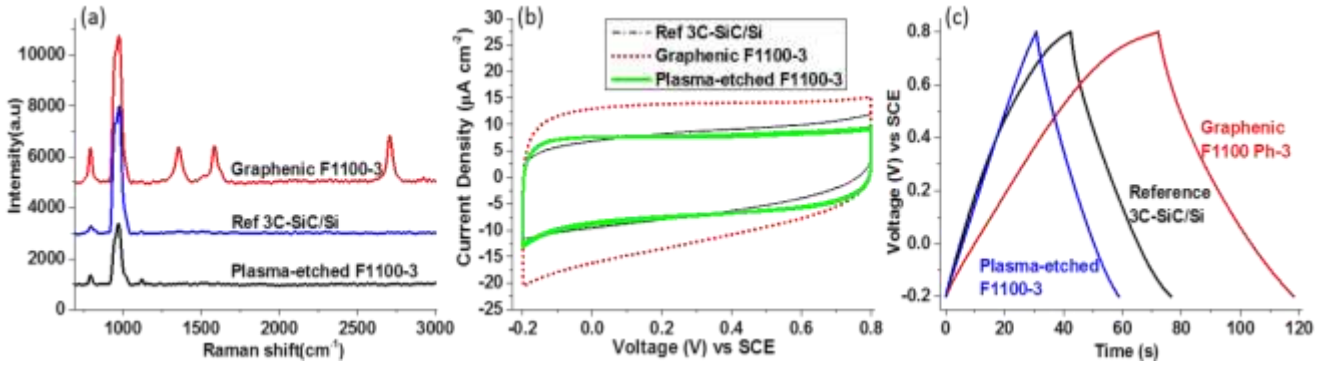

Figure 5. (a) Raman spectra, (b) CV curves 100 mV s^{-1}) and (c) galvanostatic charge-discharge curves (3 µA cm^{-2}) of the bare SiC reference, F1100-3 and plasma-etched F1100-3 samples. When the graphenic layer is fully removed, the etched sample behaves as poorly as (or worse than) the reference, emphasizing the central role of the nanocarbon in the supercapacitive performance. The Raman spectra indicate that the plasma etching process has successfully completely removed the graphene from the tested sample.

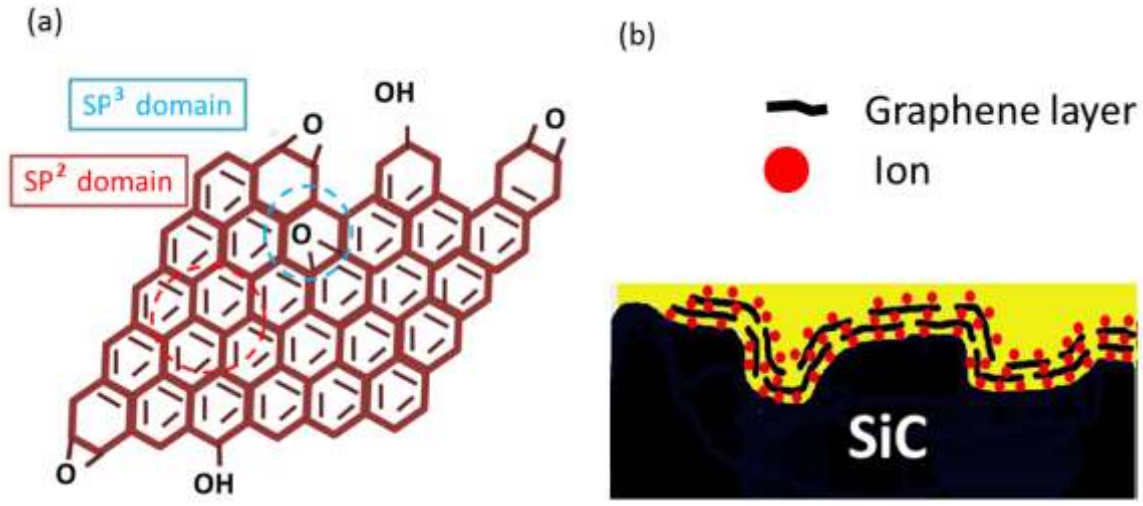

Figure 6. Schematic diagrams of (a) a defective graphenic carbon sheet including a fraction of sp^3 bonds and oxygen -containing functional groups; (b) the few-layer, highly defective, graphene on the porous SiC and how its discontinuities help an effective and extensive intercalation accommodating a maximum amount of ions from the electrolyte, greatly enhancing storage capacity.

Table 1. Sample characteristics and area capacitance (C_A)

Sample ID	I_D/I_G	FWHM (2D)	Estimated number of graphenic layers	RMS Roughness (nm)	C_A ($\mu F\ cm^{-2}$)
F1000-3	0.88±0.02	55±1	1-2	23±1	102±2
F1100-3	0.99±0.02	60±1	3-4	23±1	139±2
F1200-1	1.46±0.02	50±1	1-2	24±1	97±2
F1200-2	1.58±0.03	61±1	3-4	57±3	103±2
F1200-3	1.69±0.03	77±1	5-6	88±5	176±2
Plasma-etched F1100-3	--	--	--	23±1	84±2
Reference 3C-SiC/Si	--	--	--	~9	86±2

The graphenic samples are prepared at temperatures ranging from 1000 to 1200°C, with a progressive number of graphitization cycles (1 to 3). I_D/I_G indicates the intensity ratio of the graphene Raman D and G bands, a measure of the defectivity of the graphenic layers. The full width at half maximum (FWHM) of the 2D Raman band helps to estimate the number of graphenic layers (see Supporting Information). A reference, bare silicon carbide on silicon (3C-SiC/Si) and plasma-etched sample to fully remove the graphene layer are also reported for comparison. The area capacitance (C_A) is calculated from the galvanostatic charge-discharge curves.