Model Predictive Control Applied to a Single Phase Seven-Level Active Rectifier

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***Abstract*-- This paper presents an improved single phase seven-level active rectifier architecture controlled by finite control set model predictive control (FCS-MPC). The FCS-MPC is designed to enable power conversion with a unity power factor and generate seven level voltage waveform at the input. The proposed active rectifier architecture reduces harmonic contents of the rectifier input current by producing different voltage levels at the rectifier input. Owing to the architecture and multilevel operation, it reduces the EMI filter size, input current harmonic, the voltage rating on devices and switching losses that are lower than those of conventional three-level rectifier topologies. The proposed converter can also be operated as a multilevel inverter. Extensive simulation results are presented to verify the proposed converter when the load changes, the reference active and reactive power changes.**

***Index Terms*—Multilevel converter, model predictive control, bidirectional converter, power factor.**

I. INTRODUCTION

Integration of distributed energy sources (DESs) in the distribution network requires bidirectional power converter to implement the proper management of energy transfer from microgeneration units to utility grid towards distributed smart grid development. The power converters associated with the DES would have the ability to contribute to mitigate power quality problems in the power grid. These converters should be designed to permit bidirectional energy transfer and the current in the AC side should be sinusoidal with variable and controlled power factor. These converters operate as active rectifier during the energy storage devices charging. In addition, to inject the required real and reactive power into the grid from DES, these power converters operate as controlled inverter. It is essential to ensure that the converters should respond fast and accurately with the variations of environmental conditions and EV integration. The grid current should have low harmonic distortion, controlled power factor and controllable output voltage and current. A common topology of these type of converters is full-bridge three-level converter. This converter can fulfil the requirements through a very high switching frequency. However, high switching frequency operation will increase the switching losses, acoustic noise, and the level of EMI to other equipment. Therefore, it is essential to increase the voltage level to reduce harmonic contents, filter size and EMI [1]-[5].

Furthermore, during the charging of energy storage device and EV, large numbers of voltage levels at the rectifier input reduce the harmonic content of the grid current with less dv/dt stressing in the semiconductors. Similarly, multilevel inverters have nearly sinusoidal output voltage waveforms and consequently the output current shows a low total harmonic distortion (THD) using a small volume and size of the passive filters. Several approaches have been employed for dc-ac inverter and ac-dc power factor correction (PFC) rectifier to achieve controlled power factor (PF), low THD and controlled output voltage and current [14]-[16].

The most employed PFC converter topology is the diode-bridge rectifier followed by a dc-dc boost converter. An ac-dc three level PFC converter with phase shift modulation [1], a dc-dc dual output buck-boost PFC converter [2]. Furthermore, to avoid the front-end diode-bridge rectifier, the bridgeless three level topologies are analyzed in [3]. A review paper about performance evaluation of bridgeless PFC topologies is presented in [4], where the performance of the popular symmetrical and asymmetrical bridgeless PFC architectures are presented in [5]. Several PFC topologies including interleaved and the multi-level converters are presented in [6]-[9]. The main advantage of the multi-level converters is the possibility of reducing the voltage stress on the semiconductor devices, and the volume and size of the passive filter. Although the cascaded H-bridge (CHB) multilevel converter is the most employed architecture to synthesize multilevel output voltages and can be expanded indefinitely, these topologies require a large number of power switches and independent dc links [9]-[12]. To solve this problem, the CHB based topologies are modified by utilizing asymmetrical dc voltage sources to reduce the total component counts in [13]. However, this topology still requires increased number of independent input dc links in higher voltage levels generation. In addition, all such architectures were experimentally validated only operating an as inverter.

A simple circuit topology with reasonable component count is presented in [14]. Although the architecture requires only one dc source, the efficiency tends to degrade considerably with the increased number of semiconductors in the current flowing path in each level generation. One attractive multilevel converter architecture has been proposed in [5]. In contrast with the above-mentioned converters, this topology generates the same number of voltage levels with reduced number of power switches and current passing through less semiconductor devices in each level generation. In addition, this topology was validated only operating as an inverter and typically restricted to seven-level voltage generation only. An alternative method is presented in [15], in which the total component count is less compared

to other architectures and it utilizes a single dc source. However, this topology uses a bulky capacitor and the circulating current passes through three semiconductor devices in each voltage level generation. As a result, it increases conduction losses. Similarly, a five level inverter architecture specially dedicated for photovoltaic applications is presented in [16]. However, this topology requires three more semiconductor devices compared with the proposed topology. Furthermore, this topology was experimentally validated only operating as a grid connected inverter, not as an active rectifier.

This paper presents a modified H-bridge single-phase seven level active rectifier topology that can increase the number of output voltage levels with a reduced number of circuit components. The main advantage of the multi-level converters is the possibility of reducing the voltage stress in the semiconductors, and the volume and size of the passive filters. Large numbers of voltage levels at the rectifier input would reduce the harmonic content of the grid current with less *dv/dt* stressing in the semiconductor devices. In addition, the proposed converter can also be operated as a grid-tied seven level inverter.

The organization of this paper is as follows. Section II proposes the structure and operation of the proposed converter architecture. Its operation details are described during the operation as an active rectifier. Section III describes the FCS-MPC applied to the proposed converter. Section IV of the paper presents the simulation results of the proposed architecture that leverages the advantages of the proposed approach to operate in multi-levels. Finally, Section V concludes the paper.

II. Operation and Analysis

A. Converter Topology

The circuit topology of the proposed converter is presented in Fig. 1. This converter comprises a single phase H-bridge converter, two bidirectional switches, a split dc-link voltage formed by capacitors C_1, C_2 and C_3, and an LC low pass filter. The proposed architecture can be realized in increased voltage levels using a single dc voltage source with higher number of capacitor in series and minimum number of switching devices compared to existing topologies.

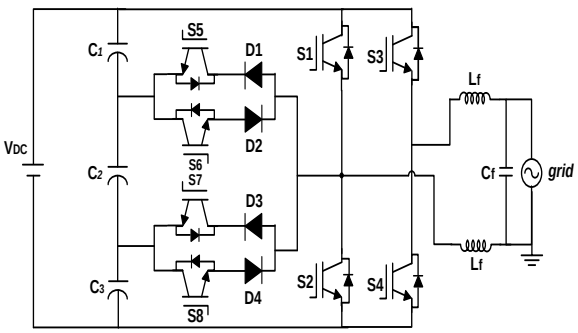


Fig. 1. Proposed converter topology.

B. Switching Scheme

Figs. 2(a) to 2(h) show the switching scheme for controlling the proposed converter to operate as an active rectifier. By comparing with the instantaneous value of the grid current reference, the FCS-MPC controller produces command signal to operate the active switches. There are eight switching states to generate seven voltage levels, where level zero can be generated using two different possible switching states.

Maximum positive input voltage: (Level $+V_{DC}$):

Fig. 2(a) shows a current path when the grid voltage is positive and the voltage produced by the converter assumes the distinct voltage level $+V_{DC}$ at the output of the rectifier. The current circulates through the antiparallel diode of switches S2 and S3.

Maximum negative input voltage: (Level $-V_{DC}$):

Fig. 2(b) shows a current path when the grid voltage is negative and the voltage produced by the converter assumes the distinct voltage level $-V_{DC}$ at the output of the rectifier. The current circulates through the antiparallel diode of switches S1 and S4.

0 input voltage: (Level 0):

Figs. 2(c) and 2(d) show the current path when the voltage produced by the converter assumes the distinct level 0 and two switching states can be considered. Switch S2 is turned on in this case. The current circulates through switch S2 and the antiparallel diode of switch S4. The alternative switching state is to turn on S1. The current circulates through switch S1 and the antiparallel diode of switch S3.

2/3 positive input voltage: (Level $+2V_{DC}/3$):

Fig. 2(e) shows a current path when the grid voltage is positive and the voltage produced by the converter assumes the distinct voltage level $2V_{DC}/3$ at the output of the rectifier. The current circulates through switch S8, diode D4 and the antiparallel diode of switch S3.

-2/3 negative input voltage: (Level $-2V_{DC}/3$):

Fig. 2(f) shows a current path when the grid voltage is negative and the voltage produced by the converter assumes the distinct voltage level $-2V_{DC}/3$ at the output of the rectifier. The current circulates through switch S5, diode D1 and the antiparallel diode of switch S4.

1/3 positive input voltage: (Level $+V_{DC}/3$):

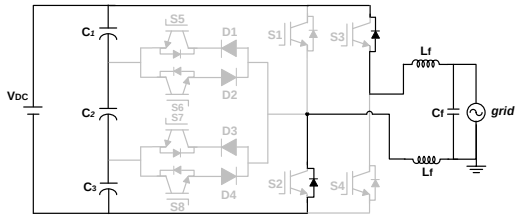
Fig. 2(g) shows a current path when the grid voltage is positive and the voltage produced by the converter assumes the distinct voltage level $V_{DC}/3$ at the output of the rectifier. The current circulates through switch S6, diode D2 and the antiparallel diode of switch S3.

-1/3 negative input voltage: (Level $-V_{DC}/3$):

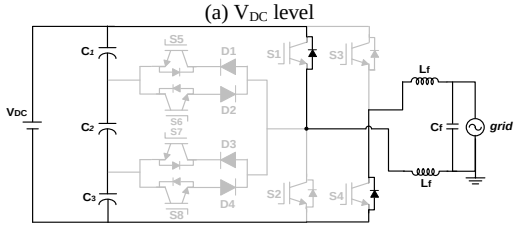
Fig. 2(h) shows a current path when the grid voltage is negative and the voltage produced by the converter assumes the distinct voltage level $-V_{DC}/3$ at the output of the rectifier. The current circulates through switch S7, diode D3 and the antiparallel diode of switch S4.

III. Model Predictive Current Control

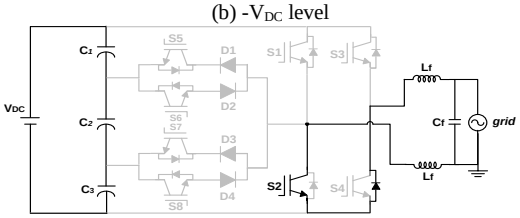
The formulation of the FCS-MPC algorithm for the proposed single-phase seven level active rectifier is described in detail in this section. The FCS-MPC controller



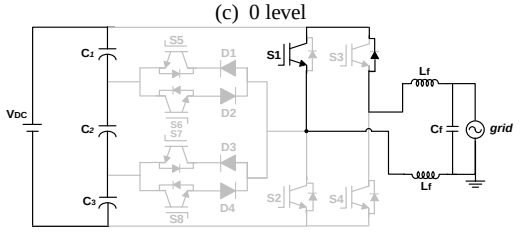
(a) V_{DC} level



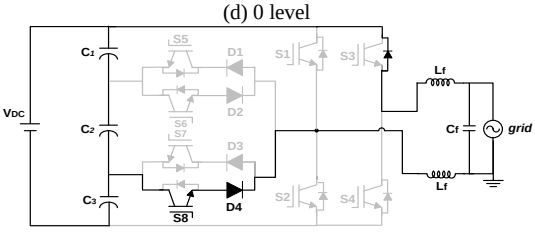
(b) -V_{DC} level



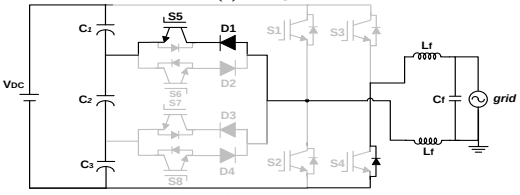
(c) 0 level



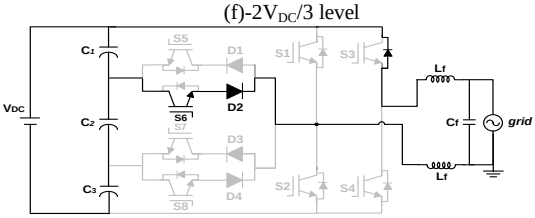
(d) 0 level



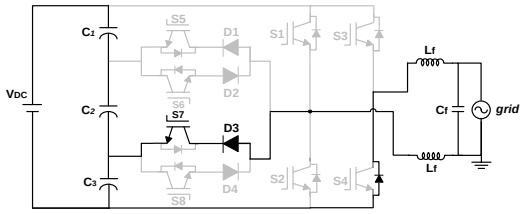
(e) $2V_{DC}/3$ level



(f)-$2V_{DC}/3$ level



(g) $V_{DC}/3$ level



(h) -$V_{DC}/3$ level

Fig. 2. Operation modes of the active rectifier.

is formulated in discrete time domain.

A. Rectifier Mode of Operation

In active rectifier mode operation, the reference grid current and the dc-link voltage of the converter are controlled in three steps.

1) Reference grid current calculation using power theory.
2) Phase-locked loop algorithm implementation to eliminate harmonic content in the calculated grid current reference.
3) Transformation of the dynamic system based on the circuit equations into discrete time domain at a specific sampling time *T*s to formulate the FCS-MPC controller.

B. Reference Grid Current Calculation

In order to maintain a unity power factor, the grid current reference (i_g^*) must be directly proportional to the grid voltage (v_g). The reference grid current is calculated by using the method proposed in [17]. This strategy uses the following control law:

$$i_g^* = G v_g \tag{1}$$

where G is the conductance seen from the grid. The conductance G is defined as:

$$G = \frac{I_G}{V_G} \tag{2}$$

where V_G is the rms value of the power grid voltage and I_G is the rms value of the grid current. The active power in the ac side of the converter is defined by (3), where the grid current is maintained in phase with the grid voltage.

$$P_G = V_G I_G \tag{3}$$

Substituting (2) into (3), the conductance G is calculated as:

$$G = \frac{P_G}{V_G^2} \tag{4}$$

Taking into account that the losses are negligible, the instantaneous grid current reference (i_g^*) is defined by:

$$i_g^* = \frac{P_G}{V_G{}^2} v_g \tag{5}$$

C. Predictive Model

The converter consists of an LCL input filter to achieve better harmonic attenuation for the grid current, a small equivalent parasitic resistance r of the filter inductors, three dc series connected capacitors C_1, C_2 and C_3, and a load resistor R. The dynamic model of the

system can be obtained using Kirchhoff laws at the ac side of the rectifier as:

$$L\frac{di}{dt} = -ri - V_{dc} + v_s \tag{6}$$

where parameter i represents the inductor current, V_{dc} is the dc output voltage, v_s *is* the single-phase grid voltage, i_s is the grid current, and r is the equivalent series resistance of the filter inductors. The capacitor current is

$$i_c = C\frac{dv_s}{dt} = i_s - i \tag{7}$$

The parameter (V_{dc}) in (6) can be expressed in terms of a tri-state function and the output voltage V as:

$$V_{dc} = \psi(t) \times V_S \tag{8}$$

where $\psi(t)$ can be obtained from the individual switching functions as shown in Table I:

TABLE I
SWITCHING STATE FOR THE ACTIVE RECTIFIER

State	S1	S2	S3	S4	S5	S6	S7	S8	ψ	V_{dc}
1	0	0	0	0	0	0	0	0	1	V_S
2	0	0	0	0	0	0	0	0	-1	$-V_S$
3	0	1	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	1	2/3	$2V_S/3$
5	0	0	0	0	1	0	0	0	-2/3	$-2V_S/3$
6	0	0	0	0	0	1	0	0	1/3	$V_S/3$
7	0	0	0	0	0	0	1	0	-1/3	$-V_S/3$

Substituting (7) into (6), the grid voltage v_s is calculated as:

$$v_s = L\frac{di}{dt} + ri + V_{dc} - LC\frac{d^2v_s}{dt^2} \tag{9}$$

Using the forward Euler approximation method with a sampling period T_S, (9) can be rewritten as:

$$v_s[k] = \frac{L}{T_S}(i_s(k+1) - i_s[k]) + V_{dc}[k] + r.i_s[k]) - \frac{LC}{T_S^2}(v_s[k+1] - 2v_s[k] + v_s(k-1)) \tag{10}$$

where k is discretized t.

Rearranging (10), in terms of the predicted grid current, $i_s[k+1]$ can be obtained as:

$$i_s[k+1] = i_s[k] + \frac{T_S}{L}(v_s[k] - V_{dc}[k]) + \frac{C}{T_S}(v_s[k+1] - 2v_s[k] + v_s[k-1]) - \frac{r}{T_S}i_s[k]) \tag{11}$$

where $v_s[k+1]$ can be obtained as [17]:

$$v_s[k+1] = 3v_s[k] - 3v_s[k-1] + v_s[k-2] \tag{12}$$

D. Cost Function

In the conventional model predictive decoupled power control, at each sampling instant, P^* and Q^* are calculated using (13), and the predicted values P^p and Q^p are calculated for each of the seven possible voltage vectors (as shown in Table I). Among these voltage vectors, the one that minimizes the cost function g is selected and applied to the converter untill the next sampling instant, when the optimization process is repeated. The real and reactive power can be predicted using the OSG reference signals as:

$$\begin{bmatrix} P[k+1] \\ Q[k+1] \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v_\alpha[k+1] & v_\beta[k+1] \\ v_\beta[k+1] & -v_\alpha[k+1] \end{bmatrix}\begin{bmatrix} i_\alpha[k+1] \\ i_\beta[k+1] \end{bmatrix} \tag{13}$$

The cost function g, which is to be minimized, is formulated from active and reactive power terms as:

$$g(k+1) = \frac{1}{P_{rated}}\left|P_{ref}(k+1) - P_{out}(k+1)\right| + \lambda\frac{1}{Q_{rated}}\left|Q_{ref}(k+1) - Q_{out}(k+1)\right| \tag{14}$$

where λ is the weighting factor of reactive power. The weighting factor is the only parameter in the cost function of the MPC that needs to be selected.

The proposed MPC has a fast transient response, similar to the conventional MPC. However, unlike the conventional MPC, the proposed MPC method uses a different cost function for the steady state. Equation (15) presents the proposed MPC cost function.

$$g = \lambda_1\left|i_{ref}(k+1) - i_{out}(k+1)\right| + \lambda_2\left(\left|P_{ref}(k+1) - P_{out}(k+1)\right|\right)^2 + \lambda_3\left(\left|Q_{ref}(k+1) - Q_{out}(k+1)\right|\right)^2 \tag{15}$$

IV. SIMULATION RESULTS

In this section, simulation results will be presented. Details simulation studies have been conducted using Matlab/Simulink environment.

Fig. 3 shows the rectifier input current and input voltage during active rectifier mode operation. In this operation mode, it is possible to confirm that the input current is sinusoidal and it is also possible to observe the seven distinct voltages of the rectifier input voltage. Fig. 4 shows the grid voltage and input current of the rectifier. The measured power factor is 0.99 at full load.

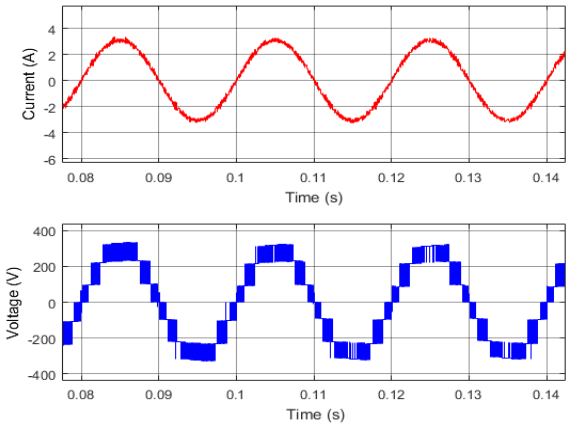


Fig. 3. (Top figure) rectifier input current, (bottom figure) rectifier input voltage.

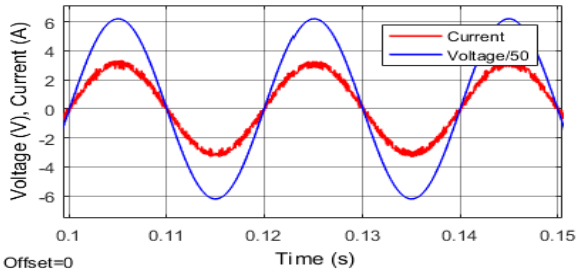


Fig. 4. Grid voltage and rectifier input current.

Fig. 5 shows the transient response of the rectifier input current, i.e., from the first to the second stage, it corresponds to a step load change. In this situation, the rectifier input current is following the current reference instantaneously between the stages. The magnified version of the Fig. 5 is shown in Fig. 6.

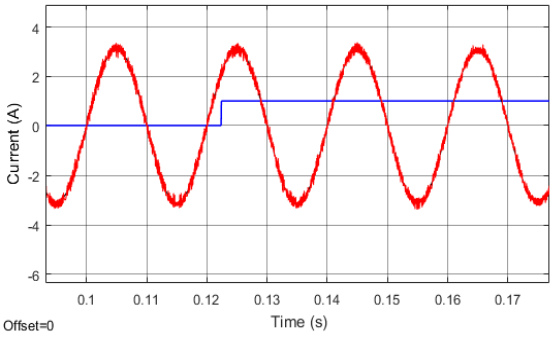


Fig. 5. Step load addition (blue), reference current (black), input current (red)

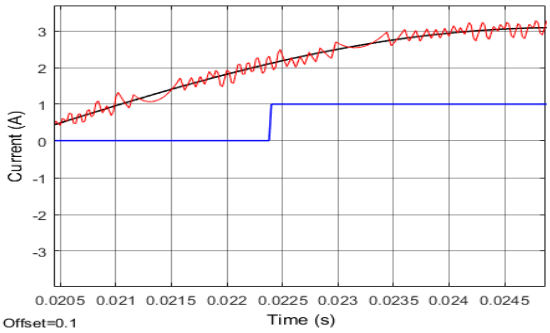


Fig. 6. Magnified version of Fig. 5.

The proposed converter is also operated as a grid connected inverter mode. The simulation results will be presented in the following. Fig. 7 shows the inverter output current and voltage during grid-tied inverter mode operation. In this operation mode, it is possible to confirm that the grid current is sinusoidal and it is also possible to observe the seven distinct voltages of the inverter, i.e., $+V_{DC}$, $+2V_{DC}/3$, $+V_{DC}/3$, 0, $-V_{DC}/3$, $-2V_{DC}/3$ and $-V_{DC}$. Fig. 7 also shows the transient response of the inverter output current i.e., from the first to the second stage it corresponds to a variation from 10 A to 15 A at 0.5s. In this situation, the grid current changes instantaneously between the stages.

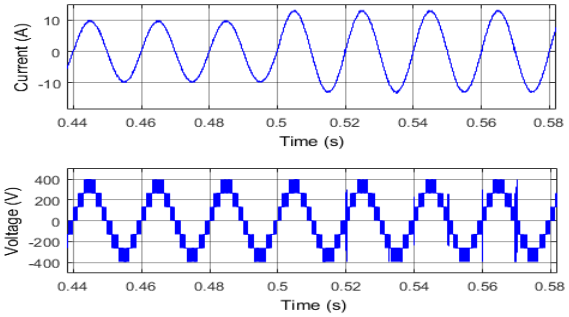


Fig. 7. (Top) inverter output current, (bottom) output voltage.

Fig. 8 shows the transient response of the active and reactive power reference changes for the proposed seven level converter, i.e., from the first to the second stage, it corresponds to an active power variation from 1500W to 2000W at 0.5s and from the second to the third stage to a reactive power variation from 0Var to 300Var at 0.7s.

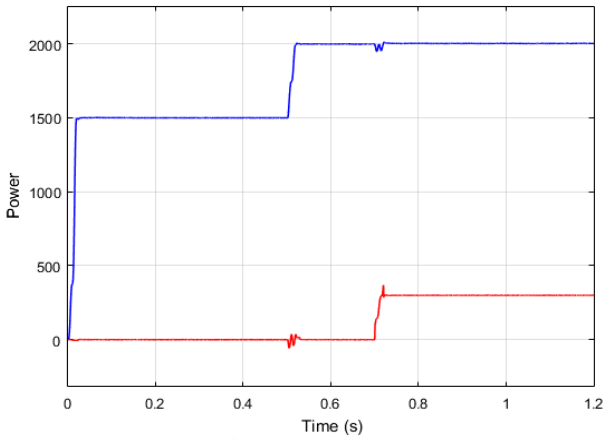


Fig. 8. Simulation results of power step responses: active power (blue), and reactive power (red).

In this condition, the converter output active and reactive powers change instantaneously according to the reference active power and reactive power after transient period. Specification of the converter is presented in Table II. The details comparison results are presented in Table III.

TABLE II
SPECIFICATION OF THE CONVERTER

Parameter	Value	Unit
Power Grid Voltage	230	V
Grid Frequency	50	Hz
DC-link Voltage	400	V
Total Power Factor (Full Load)	0.99	-
Sampling Frequency	50	kHz
Power factor at full load	0.99	-
LC Filter	5mH, 2.2μF	-

TABLE III
COMPARISON OF THE NUMBER OF CIRCUIT COMPONENTS

	3 level	5 level [17]	Proposed 7 level
THD (%) Inverter mode	2.1	2.9	5.7
THD (%) Rectifier mode	31.64	9.2	5.5

Switches	4	6	8
Diodes	0	2	4
Capacitors	0	2	3
Input DC sources	1	1	1

V. CONCLUSIONS

This paper introduces a utility interfaced multilevel converter architecture, which is suitable for bidirectional power conversion with the grid while injecting the controlled active and reactive power. An FCS-MPC has been designed for the proposed converter for seven level operation. The proposed FCS-MPC has shown an efficient and stable tracking of the reference current at steady-state and fast transient response. A multi objective cost function was defined. The tuning of the weighting factors was conducted successfully based on achieving high steady-state and dynamic tracking performances. In addition to enabling the lower THD and controlled power factor, the proposed architecture significantly decreases the voltage stress of the active and passive devices. This enables a low cost design with a small volume of EMI filter, which contributes to the converter miniaturization. Digital simulations were carried out in MATLAB/SIMULINK environment.

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