Programmable Topology Derivation and Analysis of Integrated Three-Port DC-DC Converters with Reduced Switches for Low-Cost Applications

Abstract—**Thanks to the favorable advantage of low cost, integrated three-port dc-dc converters with reduced switches have attracted extensive attention. In order to provide more new topologies, this paper aims to propose a programmable topology derivation method, which effectively simplifies the cumbersome process of the conventional combination method. Instead of the manual connection and examination, the proposed alternative can quickly and rigorously derive multiple viable integrated three-port dc-dc topologies from a great number of possible connections with the aid of computer program. Besides, generalized analysis is also accomplished, with which performance characteristics of all derived converters are simultaneously obtained and then a comprehensive comparison can be easily conducted to select a preferred one for the practical application. Finally, an example specific application with one input and two outputs is given, with topology selection, design and experimental results demonstrated in detail.**

Index Terms— **Generalized Analysis, Integrated Three-Port DC-DC Converters, Programmable Topology Derivation, Reduced Switches.**

I. INTRODUCTION

With the increase of different sources/loads in engineering applications, multi-port dc-dc converters are widely demanded to control power flow and regulate voltages among different ports, including photovoltaics, fuel cell, battery and auxiliary power supply [1-8]. To construct a multi-port system, employing multiple conventional single-input single-output (SISO) dc-dc converters is a feasible solution, but undesired high cost and large volume are incurred due to the large number of components. Actually, components such as magnetic elements and semiconductor devices in different power electronics converters can be multiplexed to achieve reduced cost, which have been adopted to derive a variety of integrated multi-port converters in [9-18].

In [9, 10], only one transformer with several secondary windings is demanded in the flyback converter to provide multiple outputs. And a common inductor is shared in the single-inductor multi-port converters to transfer power among multiple input and output ports in [11-15]. Therefore, magnetic components which usually account for a large proportion of converter weight and volume are effectively reduced in these multi-port converters. Nevertheless, they suffer from cross-regulation problem that load variation of one output would affect other output voltages, because the magnetic component functions as the energy storage element. Besides of the magnetic elements, semiconductor devices can also be

multiplexed. In [16-18], integrated three-port dc-dc converters with reduced switches/diodes are proposed, in which only three switches/diodes instead of four are utilized to generate the required two control variables for independent power control and voltage regulation. Therefore, not only low cost is obtained, but also no cross-regulation problem exists. However, only three different types of integrated three-port topologies have been proposed in [16-18], which cannot always be the best choice for different applications. For example, the current stresses of converters in [16, 18] will increase in comparison with the conventional two separate converters, and the sum of two output voltages have to be smaller than the input voltage in the converter in [17]. Therefore, more viable topologies should be explored, and then an optimum one can be selected by engineers according to the requirements.

With the purpose of providing more new topologies, several topology derivation methods including combination [19-22], duality [23-25] and addition/replacement of cells [26-28], have been presented in the past literatures, among which the combination method attracts increasing attentions recently thanks to its systematicness. With the combination method [19-22], multiple new topologies can be obtained through combining several basic cells in different appropriate ways. For example, a family of forward converters including two-switch forward converter and interleaved series input parallel output forward converter, are obtained in [19] after combination and simplification of three forward cells. Although the theoretical idea seems to be very simple, the practical implementation process of the combination method is complicated, because there are a great number of possible connecting relationships among different cells, and their effectiveness are needed to be one-by-one manually examined to select viable ones. In common practical applications, researchers may prefer to figuring out some viable topology configurations from all possible connections by their experience instead of examining all configurations one-by-one, and as a result, it is quite often that some preferred topologies are not found. In a word, the conventional manual topology derivation process of combination method is either complex or not precise enough.

From above, integrated three-port dc-dc converters with reduced switches are attractive in the engineering applications with low cost requirements. In order to derive more integrated three-port topologies for selection, this paper intends to use the combination method. However, the conventional manual effort of combination method would result in either complex or non-rigorous topology derivation process. Based on this, a programmable topology derivation method is proposed in this paper. It uses an algebraic array to represent the connections among converter components, transforms the electrical criterions into math relationships, and achieves all viable

solutions simultaneously through computer program. With the proposed method, 10 viable integrated three-port converters with reduced switches including those proposed in [16-18, 28, 31], are quickly and rigorously derived from all possible connections. Compared with the topology synthesis in [29, 30], the transformation from the topology derivation to the mathematical problem is easier in this paper, since the state equation is eliminated and its electrical criterions are simpler. Besides, in order to conveniently select an optimum one for the practical application, generalized analysis is accomplished to simultaneously obtain performance characteristics of all proposed converters with the computer program. It can further avoid the huge one-by-one manual analysis, and then the comparison can be easily conducted. As a summary, this paper aims to explore a programmable method to conveniently provide more viable integrated three-port topologies for engineers and help to fast select the most preferred one according to the real application requirements.

The paper is organized as follows. The proposed programmable topology derivation method is introduced and employed to derive viable integrated multi-port dc-dc converters in section II. And the generalized analysis of all derived topologies is conducted in section III. In section IV, experimental verification on a specific application is taken as an example to be illustrated and finally, conclusions are drawn in section V.

II. PROGRAMMABLE TOPOLOGY DERIVATION

A. Integrated three-port circuit configuration

In the conventional three-port dc-dc system, two separate converters are typically employed to control the power flow and voltage regulation among three ports, as illustrated in Fig. 1 (a). The drive signals of the switches $S_{s1} \sim S_{s2}$ in the converter 1 are complementary and so are those for the switches $S_{s3} \sim S_{s4}$ in the converter 2. These drive signals are used to generate duty-cycles $D_1 \sim D_2$ in Fig. 1(b) which are employed to independently regulate the relationships among V_1, V_2 and V_3. However, because two separate converters are employed, the

number of components is doubled, which results in undesired high cost. Actually, from Fig. 1(b), in order to obtain the two duty-cycles $D_1 \sim D_2$, three switches $S_1 \sim S_3$ are enough, instead of four. The duty-cycles $D_1 \sim D_2$ are respectively equal to $1-D_{s2}$ and $1-D_{s3}$. Therefore, by adjusting the duty-cycles $D_{s2} \sim D_{s3}$ of switches $S_2 \sim S_3$, the desired $D_1 \sim D_2$ can be obtained. And the duty-cycle D_{s1} of switch S_1 is equal to $2-D_{s2}-D_{s3}$ to ensure that there are always two switches in conduction. The circuit configuration of integrated three-port dc-dc converters is presented in Fig. 1(c), which retains the independent control among three ports with reduced overall cost.

From Fig. 1(c), nodes {①, ②}, {③, ④} and {⑤, ⑥} of $V_1 \sim V_3$ can be theoretically connected to any two different nodes among {a, b, c, d, e, f}, and thus there are $(A_6^5)^3 = 27000$ different possible connections in total. However, most of them cannot work because of violating the following two fundamental electrical criterions.

Criterion 1: Average voltages $V_{1\_avg} \sim V_{3\_avg}$ of three ports must be larger than zero, and they should be independently controlled.

Criterion 2: At any switching interval, ports $V_1/V_2/V_3$ and their combinations cannot be short-connected or parallel-connected due to the conduction of switches.

Theoretically, according to above two electrical criterions, viable integrated three-port topologies can be selected from all possible connections through one-by-one manual judgement. However, the required workload is very heavy since there are too many possible connections. And with such heavy workload, some viable topologies may be undesired left out. In order to avoid these problems, a programmable alternative is proposed, with which multiple viable integrated three-port dc-dc topologies can be systematically and simply derived with only three steps.

B. Proposed programmable topology derivation

Unlike deriving topology with one-by-one manual examination in the conventional method, the proposed method can rigorously and conveniently select all viable topologies
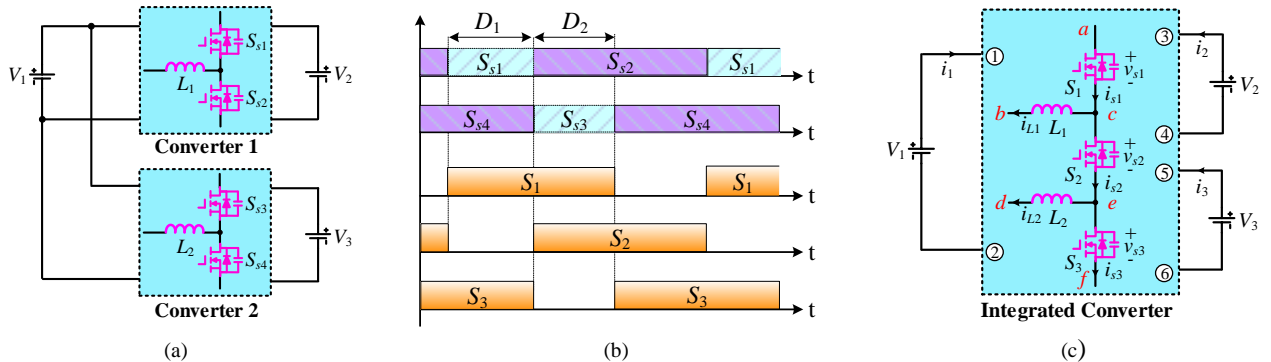

Fig. 1. Three-port system: (a) conventional, (b) drive signals and (c) integrated circuit configuration.
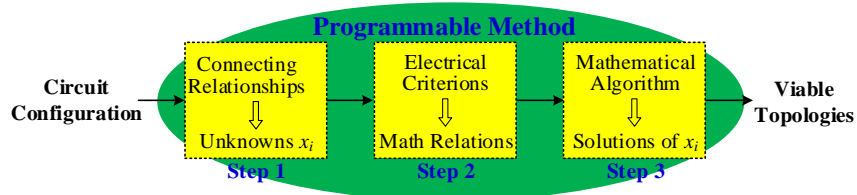

Fig. 2. Three steps of the proposed programmable topology derivation.

from possible connections through computer program. It only needs three steps, as illustrated in Fig. 2. Firstly, define the connecting relationships in the converter by unknowns x_i (i=1, 2, … 6) and the value of x_i represents the connecting position of ports $V_1/V_2/V_3$. This step enables the transformation from deriving viable topologies into a mathematical problem of finding feasible solutions to x_i. Secondly, the electrical criterions which must be satisfied to ensure the normal operation of converters are modeled by mathematical relations of x_i, e.g. equations and inequalities. Finally, according to the mathematical relations, all solutions to x_i can be found for the problem through computer implementable algorithms and then all viable topologies can be simultaneously obtained.

To be specific, the detailed programmable topology derivation process of integrated three-port dc-dc converters from the circuit configuration in Fig. 1(c) is depicted in the following.

Firstly, turn the topology derivation process into a mathematical problem. Because each node among {①, ②, ③, ④, ⑤, ⑥} will connect to one node among {a, b, c, d, e, f}, define the connecting position of node ① by x_i (i=1, 2, … 6). x_i is equal to 1, 2, 3, 4, 5 or 6, which respectively represents that node ① is connected to node a, b, c, d, e or f. Then, the problem of deriving all viable connecting relationships among nodes {①, ②, ③, ④, ⑤, ⑥} and nodes {a, b, c, d, e, f} is transformed to calculate the feasible solutions of x_i in the array A in (1).

$$A = [x_1, x_2, x_3, x_4, x_5, x_6] \qquad (1)$$

Secondly, in order to find the feasible solutions of x_1~x_6, list their mathematical relations according to the aforementioned fundamental electrical constraints. According to **Criterion 1**, (2) and (3) are respectively derived to ensure that average voltages V_{1_avg}~V_{3_avg} of three ports are larger than zero and they can be independently controlled. And from **Criterion 2**, (4) and (5) are respectively obtained to guarantee that ports $V_1/V_2/V_3$ and their combinations cannot be short-connected or parallel-connected due to the conduction of switches at any time. V_{1_sw}~V_{3_sw} respectively represent the connecting voltages of V_1~V_3 in the switching interval.

$$V_{i\_avg} > 0 \qquad i = 1, 2, 3 \qquad (2)$$

$$\begin{cases} V_{i\_avg} \neq V_{j\_avg} \\ V_{i\_avg} \neq V_{j\_avg} + V_{k\_avg} \end{cases} \quad i, j, k = 1, 2, 3; i \neq j \neq k \qquad (3)$$

$$\begin{cases} V_{i\_sw} \neq 0 \\ V_{i\_sw} + V_{j\_sw} \neq 0 \\ V_{i\_sw} + V_{j\_sw} + V_{k\_sw} \neq 0 \end{cases} \quad i, j, k = 1, 2, 3; i \neq j \neq k \qquad (4)$$

$$\begin{cases} V_{i\_sw} \neq V_{j\_sw} \\ V_{i\_sw} \neq V_{j\_sw} + V_{k\_sw} \end{cases} \quad i, j, k = 1, 2, 3; i \neq j \neq k \qquad (5)$$

In (2)~(5), V_{1_avg}~V_{3_avg} and V_{1_sw}~V_{3_sw} should be expressed as a function of x_1~x_6 to get the solutions. Denote the average voltage potential of nodes {a, b, c, d, e, f} as V_{node_avg} in (6). Because the average voltages across inductors L_1~L_2 are zero due to the flux balance, the average voltage potentials of nodes {b, c}, {d, e} are equal, i.e. $V_{b\_avg} = V_{c\_avg}$, $V_{d\_avg} = V_{e\_avg}$. And the average voltages across switches S_1~S_3 are larger than zero, so

that $V_{a\_avg} > V_{c\_avg} > V_{e\_avg} > V_{f\_avg}$ can be obtained. From Fig. 1(c), voltages V_{1_avg}~V_{3_avg} can be calculated in terms of x_1~x_6, as shown in (7). Likewise, voltages V_{1_sw}~V_{3_sw} can also be calculated in terms of x_1~x_6 and V_{node_sw}, as illustrated in (8). V_{node_sw} is the voltage potentials of nodes {a, b, c, d, e, f} in the switching interval. From the proposed drive signals of S_1~S_3 in Fig. 1(b), a switching period consists of three intervals, and in each interval, there are always two different switches in on-state. When S_1 and S_2 are on, voltage potentials of nodes a, c, e are the same and V_{node_sw} is denoted as V_{node_s1s2} in (9). Likewise, when S_2, S_3 or S_3, S_1 are on, V_{node_sw} is correspondingly denoted as V_{node_s2s3} or V_{node_s3s1} in (9).

$$V_{node\_avg} = [V_{a\_avg}, V_{b\_avg}, V_{c\_avg}, V_{d\_avg}, V_{e\_avg}, V_{f\_avg}] \qquad (6)$$

$$V_{i\_avg} = V_{node\_avg}(x_{2i-1}) - V_{node\_avg}(x_{2i}), \quad i = 1, 2, 3 \qquad (7)$$

$$V_{i\_sw} = V_{node\_sw}(x_{2i-1}) - V_{node\_sw}(x_{2i}), \quad i = 1, 2, 3 \qquad (8)$$

$$V_{node\_S_1S_2} = [V_{ace\_S_1S_2}, V_{b\_S_1S_2}, V_{ace\_S_1S_2}, V_{d\_S_1S_2}, V_{ace\_S_1S_2}, V_{f\_S_1S_2}]^T,$$
$$V_{node\_S_2S_3} = [V_{a\_S_2S_3}, V_{b\_S_2S_3}, V_{cef\_S_2S_3}, V_{d\_S_2S_3}, V_{cef\_S_2S_3}, V_{cef\_S_2S_3}]^T,$$
$$V_{node\_S_3S_1} = [V_{ac\_S_3S_1}, V_{b\_S_3S_1}, V_{ac\_S_3S_1}, V_{d\_S_3S_1}, V_{ef\_S_3S_1}, V_{ef\_S_3S_1}]^T$$
$$(9)$$

Finally, with the constraints in (2)~(5) and the expressions in (6)~(9), multiple sets of solutions x_1~x_6 can be obtained through computer program. Among these solutions, there are redundant and equivalent ones. The redundant ones are defined as the different solutions of x_1~x_6 which only swap the connecting positions of V_1, V_2, V_3. Except for the redundant solutions, equivalent ones which have different connecting relationships but have same performances are also needed to be excluded.

Following the above three steps, a Matlab code is written and its flowchart is depicted in Fig. 3. Firstly, list all possible A=[x_1, x_2, x_3, x_4, x_5, x_6]. Because voltage potentials of positive nodes {①, ③, ⑤} of V_1~V_3 are respectively higher than their negative nodes {②, ④, ⑥}, there are 13 kinds of possible sets {12, 13, 14, 15, 16, 24, 25, 26, 34, 35, 36, 46, 56} for x_1x_2, x_3x_4 or x_5x_6. Therefore, 13^3=2197 different array A is obtained, which forms a matrix B=[A_1, A_2, … A_{2197}]^T. Afterwards, for each A_i(i=1, 2…2197), judging whether constraints (2)~(5) are satisfied or not. If they are not all satisfied, A_i is not the correct solution and would be deleted from matrix B. After 2197 iterations, all viable solutions of array A would be obtained. However, it includes the redundant and equivalent ones, and hence the further exclusion is demanded. In order to exclude the redundant solutions, denote X_{v1}={x_1, x_2}, X_{v2}={x_3, x_4} and X_{v3}={x_5, x_6}. Then by checking whether any of the (X_{V1}, X_{V2}, X_{V3}), (X_{V1}, X_{V3}, X_{V2}), (X_{V2}, X_{V1}, X_{V3}), (X_{V2}, X_{V3}, X_{V1}), (X_{V3}, X_{V1}, X_{V2}), (X_{V3}, X_{V2}, X_{V1}) have already appeared in the obtained set of x_1~x_6, redundant solutions can be easily excluded and 22 non-redundant ones are obtained. Next, the exclusion of equivalent ones is further completed by judging whether all loops of two converters are totally the same. Search of the loops of different topologies can use the depth-first search. With the computer program, 10 sets of different x_1~x_6 whose topologies are non-redundant and non-equivalent are finally obtained in Table 1. It takes 1.843 seconds to run on a personal computer with Intel Xeon E3-1231 v3 CPU, 3.4GHz and 64G RAM. Then, 10 integrated three-port dc-dc topologies are correspondingly derived in Fig. 4. Except that four topologies
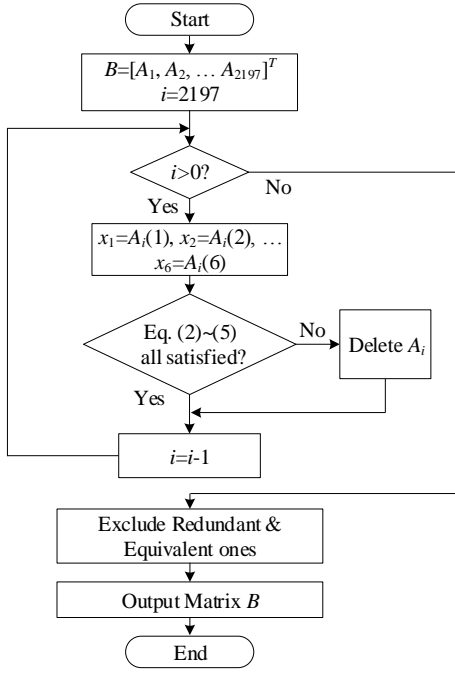
Fig. 3. Flowchart of Matlab code.

Table 1. 10 feasible sets of x_1~x_6.

	x_1	x_2	x_3	x_4	x_5	x_6
Fig. 4 (a)	1	6	1	4	2	6
Fig. 4 (b)	1	6	2	6	4	6
Fig. 4 (c)	1	6	2	4	4	6
Fig. 4 (d)	1	6	2	4	2	6
Fig. 4 (e)	1	4	2	6	4	6
Fig. 4 (f)	1	4	2	4	4	6
Fig. 4 (g)	1	4	2	4	2	6
Fig. 4 (h)	1	2	2	6	4	6
Fig. 4 (i)	1	2	2	4	4	6
Fig. 4 (j)	1	2	1	6	4	6

Table 2. Calculation results of integrated N-port dc-dc topologies.

Number of ports(N)	2	3	4	5
Number of feasible topologies	2	10	96	1564
Calculation time	1.327s	1.843s	8.477s	204.761s

results of integrated two-port, three-port, four-port and five-port dc-dc converters, including the number of feasible topologies and the corresponding calculation time. It is noted that when N=2, the derived two-port topologies are well-known bidirectional buck/boost and buck-boost/ buck-boost converters.

similar with (b), (h), (i) and (j) have been presented in [16-18, 28, 31], all remaining topologies are firstly proposed in the paper. All proposed converters can work normally that ports V_1~V_3 are independently controlled with the drive signals of switches S_1~S_3 in Fig. 1(b). Due to the different configurations, their performance characteristics are various and hence are preferred in different applications, such as auxiliary power supply, PV/battery hybrid system and battery cell equalizer.

C. Extension to integrated N-port topologies

Apart from the integrated three-port dc-dc converters, the proposed programmable topology derivation method can also be applied to other N-port topologies with simple modification as follows. For an integrated N-port circuit configuration, the number of elements x_i in the array A in (1) is modified as $2N$, and the value of each x_i can be one of $\{1, 2, \ldots 2N\}$. The number of voltage source in constraints (2)~(5) and the available connecting nodes in (6)~(9) are both changed to N. Then, referring to the aforementioned solving process step-by-step, viable integrated N-port topologies can be easily obtained from the similar computer code. Table 2 summarizes the calculation

III. GENERALIZED ANALYSIS

After topology derivation, performance analysis of all proposed topologies in Fig. 4 should be conducted to have a comprehensive comparison under the specific application so that a most preferred one can be selected. Although one-by-one manual evaluation of all topologies is feasible, it would be also a tedious and cumbersome work for engineers. Fortunately, because the circuit configurations of these proposed topologies are similar and only the connecting relationships of V_1~V_3 are different, their performance analysis can be expressed in a generalized form with different $x_i(i=1, 2, \ldots 6)$. Then, through a computer program, the performance characteristics of all proposed topologies including voltage/current relationship, ZVS operation and small-signal model, can also be simultaneously obtained.
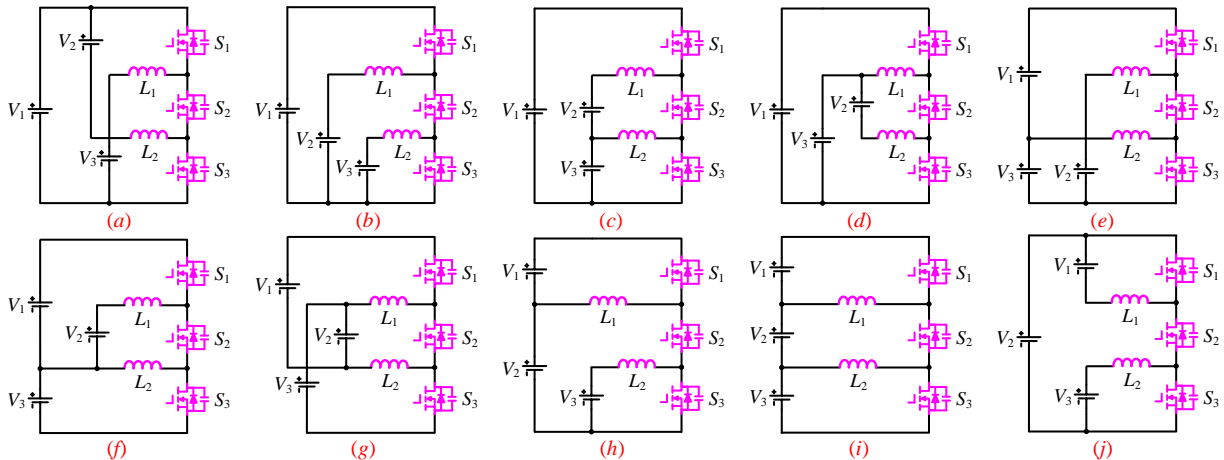

Fig. 4. 10 integrated three-port dc-dc converters with reduced switches.

A. Operational Principle

From the drive signals in Fig. 1(b), two and only two switches (or their parasitic diodes) among S_1~S_3 should be in on-state at any time, to ensure that inductors L_1~L_2 would not be disconnected and voltage source across $\{a, f\}$ would not be shorted. According to the different phase relation, except for the drive signals in Fig. 1 (b) which is re-defined as DRA in Fig. 5(a), there is another drive signals DRB as shown in Fig. 5 (b). No matter with drive signal DRA or DRB, the operation of all proposed converters working in continuous conduction mode (CCM) is consisted of three different stages ($St1$, $St2$, $St3$) in a switching period, and their equivalent circuits in different stages are illustrated in Fig. 6. Because the switching process is relatively short, it is neglected. It is noted that operation with drive signal DRA and DRB are almost the same, except for the different sequence of stage $St1$ and $St2$. This difference only has an impact on the soft-switching operation of switches S_1~S_3, which will be detailed analyzed afterwards.
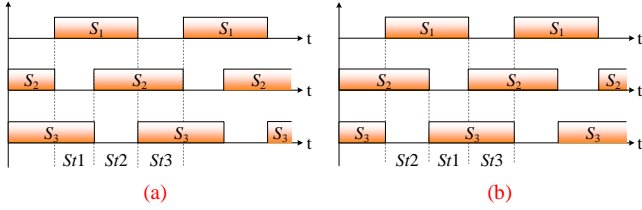

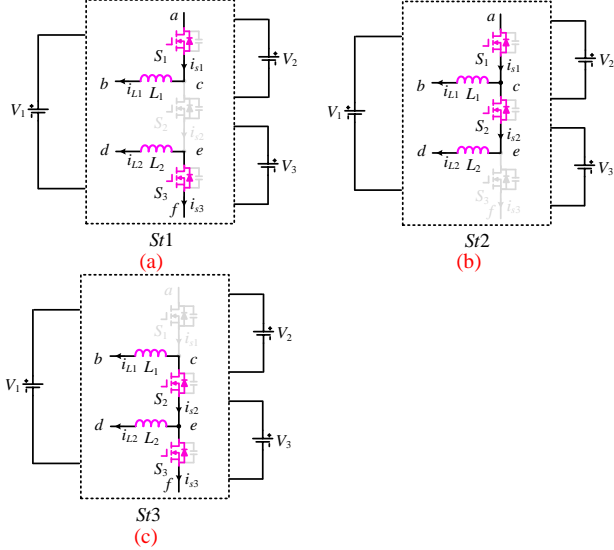Fig. 5. Two types of drive signals: (a) DRA and (b) DRB.

Fig. 6. Equivalent circuits in different stages: (a) $St1$, (b) $St2$ and (c) $St3$.

B. Voltage Relationship

From (7), average voltages $V_{1,avg}$~$V_{3,avg}$ of all proposed converters can be expressed as a function of voltage potentials $\{V_{a\_avg}, V_{b\_avg}, V_{c\_avg}, V_{d\_avg}, V_{e\_avg}, V_{f\_avg}\}$ and x_i. Meanwhile, according to Fig. 1(c), the average voltages across two nodes (a, c), (c, e) and (e, f) are respectively equal to the average drain-to-source voltages $\bar{v}_{s1}$ ~ $\bar{v}_{s3}$ of switches S_1~S_3, and $V_{b,avg}=V_{c,avg}$, $V_{d,avg}=V_{e,avg}$ can be obtained owing to the flux balance of inductors L_1~L_2, which are summarized in (10). Then, voltage relationships among $V_{1,avg}$~$V_{3,avg}$ of all proposed three-port converters in Fig. 4 are easily derived in Table 3 from (7) and (10) by plugging in the x_i in Table 1, which also could be implemented by computer program. Taking the

converter in Fig. 4(a) as an example, $x_1=1$, $x_2=6$, $x_3=1$, $x_4=4$, $x_5=2$ and $x_6=6$ are obtained from Table 1. Then, voltages of three ports are $V_{1,avg}=V_{a,avg}-V_{f,avg}$, $V_{2,avg}=V_{a,avg}-V_{d,avg}=(2-D_{s1}-D_{s2})(V_{a,avg}-V_{f,avg})$, and $V_{3,avg}=V_{b,avg}-V_{f,avg}=(2-D_{s2}-D_{s3})(V_{a,avg}-V_{f,avg})$. From the drive signals of switches S_1~S_3 in Fig. 5, there are always two switches in on-state at any time and hence $D_{s1}+D_{s2}+D_{s3}=2$ are obtained. Then, voltage gains $V_{2,avg}/V_{1,avg}=D_{s3}$, $V_{3,avg}/V_{1,avg}=D_{s1}$ and $V_{3,avg}/V_{2,avg}=D_{s1}/D_{s3}$ can be derived. Besides, the voltage stresses $V_{s1,2,3}$ of switches S_1~S_3 in all proposed converter in terms of V_1~V_3 are also summarized in Table 3 from Fig. 4.

$$\begin{cases} V_{a\_avg} - V_{c\_avg} = \bar{v}_{s1} = (1-D_{s1})(V_{a\_avg} - V_{f\_avg}) \\ V_{c\_avg} - V_{e\_avg} = \bar{v}_{s2} = (1-D_{s2})(V_{a\_avg} - V_{f\_avg}) \\ V_{e\_avg} - V_{f\_avg} = \bar{v}_{s3} = (1-D_{s3})(V_{a\_avg} - V_{f\_avg}) \\ V_{b\_avg} = V_{c\_avg}, \ V_{d\_avg} = V_{e\_avg} \end{cases} \quad (10)$$

where D_{s1}~D_{s3} are the duty-cycles of switches S_1~S_3, respectively.

Table 3. Voltage gains and voltage stresses of all proposed converters.

Fig. 4	Voltage Gains			Voltage Stresses
	$V_{2,avg}/V_{1,avg}$	$V_{3,avg}/V_{1,avg}$	$V_{3,avg}/V_{2,avg}$	$V_{s1,2,3}$
(a)	D_{s3}	D_{s1}	D_{s1}/D_{s3}	V_1
(b)	D_{s1}	$1-D_{s3}$	$(1-D_{s3})/D_{s1}$	V_1
(c)	$1-D_{s2}$	$1-D_{s3}$	$(1-D_{s3})/(1-D_{s2})$	V_1
(d)	$1-D_{s2}$	D_{s1}	$D_{s1}/(1-D_{s2})$	V_1
(e)	D_{s1}/D_{s3}	$(1-D_{s3})/D_{s3}$	$(1-D_{s3})/D_{s1}$	V_1+V_3
(f)	$(1-D_{s2})/D_{s3}$	$(1-D_{s3})/D_{s3}$	$(1-D_{s3})/(1-D_{s2})$	V_1+V_3
(g)	$(1-D_{s2})/D_{s3}$	D_{s1}/D_{s3}	$D_{s1}/(1-D_{s2})$	$V_1+V_3-V_2$
(h)	$D_{s1}/(1-D_{s1})$	$(1-D_{s3})/(1-D_{s1})$	$(1-D_{s3})/D_{s1}$	V_1+V_2
(i)	$(1-D_{s2})/(1-D_{s1})$	$(1-D_{s3})/(1-D_{s1})$	$(1-D_{s3})/(1-D_{s2})$	$V_1+V_2+V_3$
(j)	$1/(1-D_{s1})$	$(1-D_{s3})/(1-D_{s1})$	$1-D_{s3}$	V_2

C. Current Relationship

According to the operational principle, drain-to-source currents i_{s1}~i_{s3} in different stages $St1$~$St3$ of all proposed converters are obtained in Table 4, as a function of inductor currents i_{L1}~i_{L2}. Define k_{ij}=isequal($x_i=j$), i, j=1,2…6, which is equal to 1 if the node ⓘ is connected to the jth node in $\{a, b, c, d, e, f\}$ and is equal to 0 if not connected. Then, from Fig. 4, relationship among inductor currents i_{L1}~i_{L2} and port currents i_1~i_3 is obtained in (11). Afterwards, the average inductor currents I_{L1}~I_{L2} in terms of average port current I_1~I_3 of all proposed converters can be easily calculated by plugging in the corresponding k_{ij} through the computer program, as illustrated in Table 5. Likewise, take the converter in Fig. 4(a) as an example. Because it has $x_1=1$, $x_2=6$, $x_3=1$, $x_4=4$, $x_5=2$ and $x_6=6$, $k_{11}=k_{26}=k_{31}=k_{44}=k_{52}=k_{66}=1$ can be obtained and the value of other k_{ij} is 0. Then according to (11), $I_{L1}=-I_3$ and $I_{L2}=I_2$ can be achieved.

Table 4. Drain-to-source currents i_{s1}~i_{s3} in different stages.

Stages	i_{s1}	i_{s2}	i_{s3}
$St1$	i_{L1}	0	$-i_{L2}$
$St2$	$i_{L1}+i_{L2}$	i_{L2}	0
$St3$	0	$-i_{L1}$	$-i_{L1}-i_{L2}$

$$\begin{cases} i_{L1} = (k_{22} - k_{12})i_1 + (k_{42} - k_{32})i_2 + (k_{62} - k_{52})i_3 \\ i_{L2} = (k_{24} - k_{14})i_1 + (k_{44} - k_{34})i_2 + (k_{64} - k_{54})i_3 \end{cases} \quad (11)$$

Table 5. Average inductor currents $I_{L1} \sim I_{L2}$ in terms of $I_1 \sim I_3$.

Fig. 4	(a)	(b)	(c)	(d)	(e)
I_{L1}	$-I_3$	$-I_2$	$-I_2$	$-I_2-I_3$	$-I_2$
I_{L2}	I_2	$-I_3$	I_2-I_3	I_2	I_1-I_3
Fig. 4	(f)	(g)	(h)	(i)	(j)
I_{L1}	$-I_2$	$-I_2-I_3$	I_1-I_2	I_1-I_2	I_1
I_{L2}	$I_1+I_2-I_3$	I_1+I_2	$-I_3$	I_2-I_3	$-I_3$

D. ZVS Operation

From Table 4, drain-to-source currents $i_{s1} \sim i_{s3}$ in different stages $St1 \sim St3$ of all proposed converters are equal to $\pm I_{L1}$, $\pm I_{L2}$ or $\pm(I_{L1}+I_{L2})$, with the neglect of ripple current. Comparing I_{L1}, I_{L2} and $I_{L1}+I_{L2}$ with zero, six divided regions R1~R6 are obtained, as illustrated in Fig. 7. In different regions, ZVS operation of one switch among $S_1 \sim S_3$ in all proposed converters

R1: $I_{L1} < 0, I_{L2} > 0, I_{L1} + I_{L2} > 0$
R2: $I_{L1} > 0, I_{L2} < 0, I_{L1} + I_{L2} < 0$
R3: $I_{L1} < 0, I_{L2} < 0, I_{L1} + I_{L2} < 0$
R4: $I_{L1} > 0, I_{L2} > 0, I_{L1} + I_{L2} > 0$
R5: $I_{L1} > 0, I_{L2} < 0, I_{L1} + I_{L2} > 0$
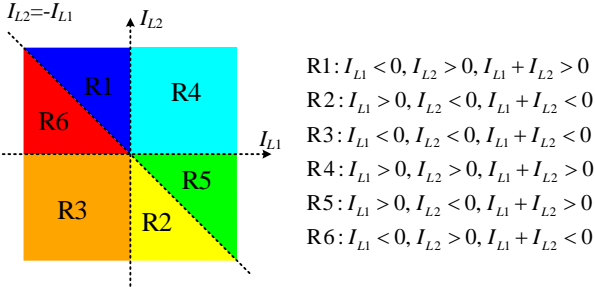R6: $I_{L1} < 0, I_{L2} > 0, I_{L1} + I_{L2} < 0$

Fig. 7. Six divided regions with $I_{L1}=0$, $I_{L2}=0$ and $I_{L1}+I_{L2}=0$.
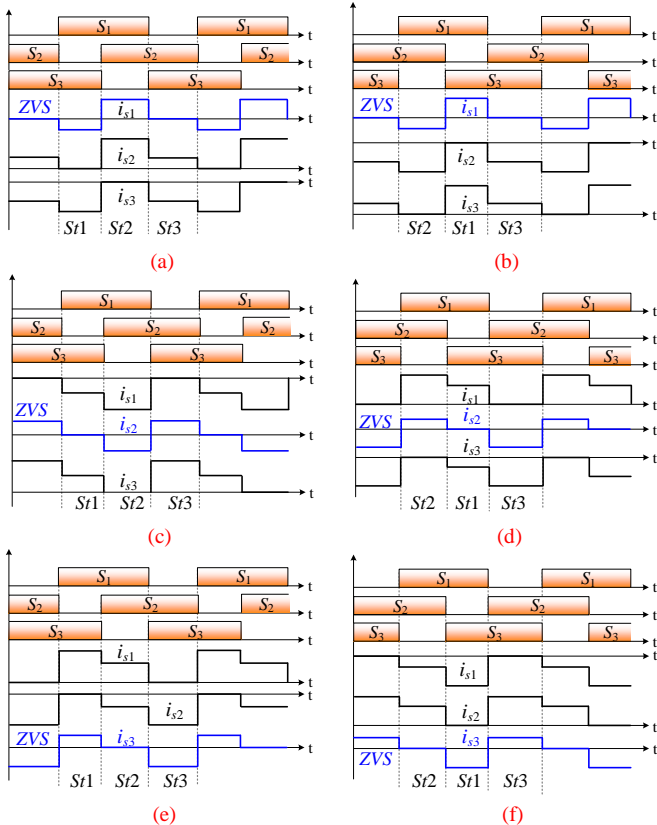

Fig. 8. ZVS realization in different regions with different drive signals: (a) R1+DRA, (b) R2+DRB, (c) R3+DRA, (d) R4+DRB, (e) R5+DRA and (f) R6+DRB.

can always be realized with drive signals DRA or DRB, as shown in Fig. 8. In Fig. 8(a), drive signals DRA are employed when the relationship between I_{L1} and I_{L2} is in region R1 ($I_{L1}<0$, $I_{L2}>0$, $I_{L1}+I_{L2}>0$). According to Table 4, $i_{s1}=I_{L1}$ is negative in stage $St1$ and $i_{s1}=I_{L1}+I_{L2}$ is positive in stage $St2$. Therefore, current i_{L1} flows through the parasitic diode of switch S_1 before its turn-on, while current $i_{L1}+i_{L2}$ flows through the Mosfet channel of S_1 before its turn-off. Hence, ZVS operation of S_1 is achieved. Likewise, when $I_{L1} \sim I_{L2}$ are in region R2($I_{L1}>0$, $I_{L2}<0$, $I_{L1}+I_{L2}<0$), ZVS operation of S_1 is also realized as illustrated in Fig. 8(b), but with the drive signals DRB instead of DRA. Similarly, in regions R3 and R4, S_2 achieves ZVS operation with drive signals DRA and DRB, respectively. And in region R5 and R6, S_3 achieves ZVS operation with drive signals DRA and DRB, respectively. As a summary, one switch among $S_1 \sim S_3$ in all proposed converters can always achieve ZVS operation over the whole current range of I_{L1} and I_{L2} when appropriate drive signal DRA or DRB is employed, contributing to reduced switching losses.

E. Small-Signal Model

From the aforementioned analysis, average drain-to-source voltages and currents of switches $S_1 \sim S_3$ in all proposed converters are calculated in (12) and (13), respectively. In order to obtain small-signal linearized equation, all variables in (12) and (13) are assumed to be equal to their given quiescent values plus some superimposed small ac variations [32]. After neglecting the dc terms as well as second-order terms, their first-order ac terms are respectively derived in (14)~(15), based on which a unified small-signal model are obtained in Fig. 9. From Fig. 9, all proposed integrated three-port converters can easily derive their small-signal models through connecting nodes $\{①, ②, ③, ④, ⑤, ⑥\}$ to the corresponding nodes $\{a, b, c, d, e, f\}$.

$$\begin{cases} \langle v_{s1}(t) \rangle_{T_s} = (1 - d_{s1}(t))\langle v_{af}(t) \rangle_{T_s} \\ \langle v_{s2}(t) \rangle_{T_s} = (1 - d_{s2}(t))\langle v_{af}(t) \rangle_{T_s} \\ \langle v_{s3}(t) \rangle_{T_s} = (1 - d_{s3}(t))\langle v_{af}(t) \rangle_{T_s} \end{cases} \quad (12)$$

$$\begin{cases} \langle i_{s1}(t) \rangle_{T_s} = d_{s1}(t)\langle i_{L1}(t) \rangle_{T_s} + (1 - d_{s3}(t))\langle i_{L2}(t) \rangle_{T_s} \\ \langle i_{s2}(t) \rangle_{T_s} = -(1 - d_{s1}(t))\langle i_{L1}(t) \rangle_{T_s} + (1 - d_{s3}(t))\langle i_{L2}(t) \rangle_{T_s} \\ \langle i_{s3}(t) \rangle_{T_s} = -(1 - d_{s1}(t))\langle i_{L1}(t) \rangle_{T_s} - d_{s3}(t)\langle i_{L2}(t) \rangle_{T_s} \end{cases} \quad (13)$$

$$\begin{cases} \hat{v}_{s1}(t) = (1 - D_{s1})\hat{v}_{af}(t) - V_{af}\hat{d}_{s1}(t) \\ \hat{v}_{s2}(t) = (1 - D_{s2})\hat{v}_{af}(t) - V_{af}\hat{d}_{s2}(t) \\ \hat{v}_{s3}(t) = (1 - D_{s3})\hat{v}_{af}(t) - V_{af}\hat{d}_{s3}(t) \end{cases} \quad (14)$$

$$\begin{cases} \hat{i}_{s1}(t) = \hat{i}_{ss}(t) + D_{s1}\hat{i}_{L1}(t) + (1 - D_{s3})\hat{i}_{L2}(t) \\ \hat{i}_{s2}(t) = \hat{i}_{ss}(t) - (1 - D_{s1})\hat{i}_{L1}(t) + (1 - D_{s3})\hat{i}_{L2}(t) \\ \hat{i}_{s3}(t) = \hat{i}_{ss}(t) - (1 - D_{s1})\hat{i}_{L1}(t) - D_{s3}\hat{i}_{L2}(t) \end{cases} \quad (15)$$

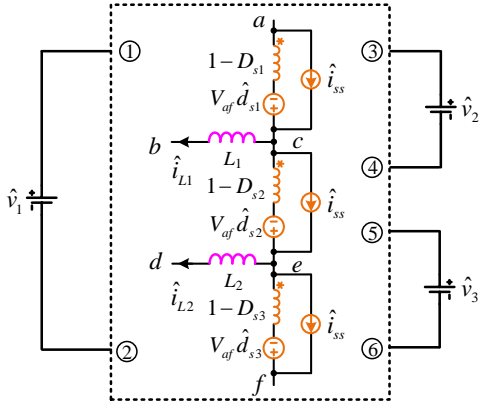where $\hat{i}_{ss}(t) = I_{L1}\hat{d}_{s1}(t) - I_{L2}\hat{d}_{s3}(t)$

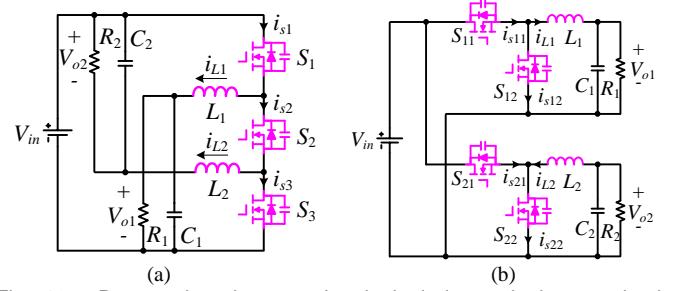Fig. 9. Unified small-signal model of all proposed three-port converters.

Fig. 10. Proposed and conventional single-input dual-output buck converter: (a) proposed and (b) conventional.

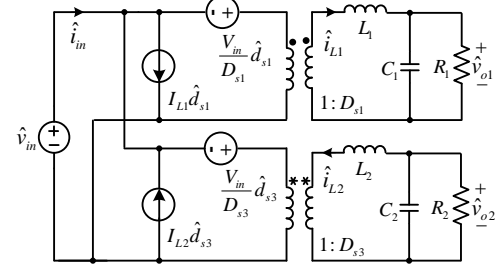Fig. 11. Small-signal model of the proposed SIDO buck converter.

IV. EXPERIMENTAL VERIFICATION ON A SPECIFIC APPLICATION

After the above generalized analysis, performance characteristics of all proposed converters are obtained simultaneously. Then, according to the system parameters of the specific application, a preferred one can be easily selected out after comparison. In this section, an example application with one input V_{in}=48V, and two outputs V_{o1}=36V, $I_{o1,max}$=3A, V_{o2}=24V, $I_{o2,max}$ =2A will be analyzed to gain a comprehensive understanding.

A. Topology Selection and Design

Firstly, according to Table 3 in the voltage relationship analysis, the topology in Fig. 4(c) and (j) cannot work normally with the system parameters, because the sum of two small voltages is smaller than the large one in these two converters while V_{o1}+V_{o2}>V_{in} is required in the example application. Among the rest eight topologies, the ones in Fig. 4(a), (b) and (d) are preferred due to their relatively lower voltage stresses of switches. Secondly, according to Table 5 in the current relationship analysis, the average inductor currents are respectively I_{o1}, I_{o2} in the topologies Fig. 4 (a)~(b) while they are respectively I_{o1}+I_{o2}, I_{o2} in the topology Fig. 4(d). Hence, thanks to lower average inductor current, topologies in Fig. 4 (a)~(b) will be further compared. Finally, from Table 4, the current stresses of switches are smaller in the topology Fig. 4(a) because of the opposite directions of inductor currents i_{L1}~i_{L2}. Therefore, after the comprehensive comparison, the topology in Fig. 4(a) which can achieve relatively lower voltage/current stresses, is selected for the example application. The converter in Fig. 4(a) is re-depicted in Fig. 10(a) with port V_1 as the input and ports V_2~V_3 as the outputs. In the example application, it is not only superior to other proposed converters in Fig. 4, but also can achieve lower cost as well as higher efficiency compared with conventional two separate buck converters in Fig. 10(b) due to the reduced switches and ZVS operation.

According to the generalized analysis, both the steady-state and dynamic characteristics of the proposed single-input dual-output (SIDO) buck converter in Fig. 10(a) can be easily obtained. The voltage gains among V_{in}, V_{o1} and V_{o2} are V_{o1}/V_{in}=D_{s1} and V_{o2}/V_{in}=D_{s3}. Therefore, D_{s1} and D_{s3} are employed to independently control the output voltages V_{o1} and V_{o2}. The duty-cycle D_{s2} is equal to 2-D_{s1}-D_{s3}. The average inductor currents I_{L1}, I_{L2} are respectively equal to output

currents I_{o1}, -I_{o2}. Because all switches S_1~S_3 are clamped by input voltage when they are off, their voltage stresses are equal to V_{in}. Because V_{in} is relatively low, the improved switching losses of buck converter working in triangular conduction mode is limited, but the increased current stresses caused by the triangular current have an adverse effect on both the conduction losses and the power rating of switches as well as inductors, resulting in higher cost. Therefore, after comprehensive consideration of both efficiency and cost, the proposed and conventional SIDO buck converters in Fig. 10 are designed to work in the typical continuous conduction mode. Then from Table 4, the root mean square (RMS) values of drain-to-source currents i_{s1}~i_{s3} are calculated in (16), with the neglect of ripple current of inductors. Then, the parameters of hardware can be designed, which are summarized in Table 6.

$$\begin{cases} I_{s1,rms} = \sqrt{(1-D_{s2})I_{L1}^2 + (1-D_{s3})(I_{L1}+I_{L2})^2} \\ I_{s2,rms} = \sqrt{(1-D_{s3})I_{L2}^2 + (1-D_{s1})I_{L1}^2} \\ I_{s3,rms} = \sqrt{(1-D_{s2})I_{L2}^2 + (1-D_{s1})(I_{L1}+I_{L2})^2} \end{cases} \quad (16)$$

Table 6. System and hardware parameters.

Parameter	Value	Parameter	Value
Input Voltage V_{in}	48V	Switching Period T_s	10μs
Output Voltage V_{o1}	36V	Inductance L_1, L_2	150, 300 μH
Output Current $I_{o1,max}$	3A	Capacitance C_1, C_2	100, 470 μF
Output Voltage V_{o2}	24V	Switches S_1~S_3	IPP530N15N3
Output Current $I_{o2,max}$	2A	Control Unit	TMS320FDSP2808

In addition, according to Fig. 9, the small-signal model of the proposed SIDO buck converter is obtained in Fig. 11. The small-signal model of the proposed SIDO buck converter is the same as two separate buck converters connecting to a common input. Therefore, no cross-regulation problem exists in the proposed converter and good dynamic response can be achieved. The control-to-output and input-to-output transfer functions are respectively derived in (17) and (18), based on

which a proportional-integral (PI) compensator can be designed and added into each control loop to improve converter performance, as illustrated in Fig. 12(a).

$$\begin{cases} G_{vd1} = \dfrac{\hat{v}_{o1}(s)}{\hat{d}_{s1}(s)}\bigg|_{\hat{v}_{in}(s)=0} = \dfrac{V_{in}}{L_1 C_1 s^2 + L_1 / R_1 s + 1} \\ G_{vv1} = \dfrac{\hat{v}_{o1}(s)}{\hat{v}_{in}(s)}\bigg|_{\substack{\hat{d}_{s1}(s)=0 \\ \hat{d}_{s3}(s)=0}} = \dfrac{D_{s1}}{L_1 C_1 s^2 + L_1 / R_1 s + 1} \end{cases} \quad (17)$$

$$\begin{cases} G_{vd2} = \dfrac{\hat{v}_{o2}(s)}{\hat{d}_{s3}(s)}\bigg|_{\hat{v}_{in}(s)=0} = \dfrac{V_{in}}{L_2 C_2 s^2 + L_2 / R_2 s + 1} \\ G_{vv2} = \dfrac{\hat{v}_{o2}(s)}{\hat{v}_{in}(s)}\bigg|_{\substack{\hat{d}_{s1}(s)=0 \\ \hat{d}_{s3}(s)=0}} = \dfrac{D_{s3}}{L_2 C_2 s^2 + L_2 / R_2 s + 1} \end{cases} \quad (18)$$
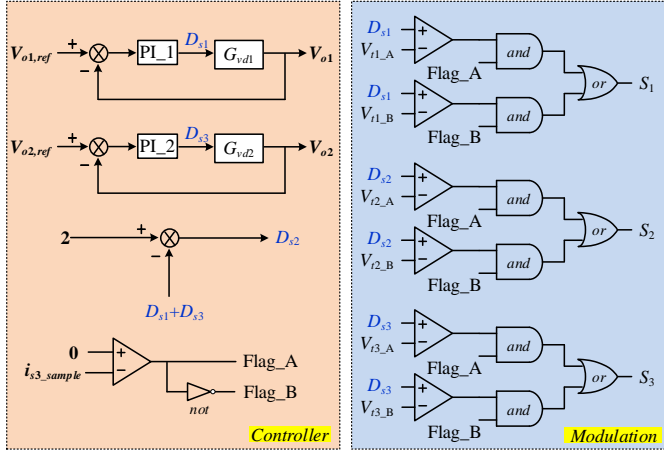

Fig. 12. Control, modulation and drive-signals generation: (a) control and modulation and (b) drive-signals generation.

In the proposed SIDO buck converter, because $i_{L1}=i_{o1}$ is larger than zero and $i_{L2}=-i_{o2}$ is smaller than zero, i_{L1} and i_{L2} may locate in region R2 or R5 in Fig. 7 under different load condition, depending on whether $i_{L1}+i_{L2}$ is larger than zero or not. According to Fig. 8(b) and (e), S_1 can achieve ZVS operation with drive signals DRB and $i_{L1}+i_{L2}<0$, while S_3 can achieve ZVS operation with drive signals DRA and $i_{L1}+i_{L2}>0$. Therefore, ZVS operation is achieved for either S_1 or S_3 in the proposed SIDO buck converter over the whole load range if appropriate drive signals are employed according to the relationship between $i_{L1}+i_{L2}$ and 0. $i_{L1}+i_{L2}$ can be acquired by sampling the drain-to-source current i_{s3_sample} of switch S_3 at the middle of stage $St3$ which is always equal to $-(i_{L1}+i_{L2})$. The sample point is denoted as SP in Fig. 12(b). When the sampled current i_{s3_sample} is smaller than zero which means $i_{L1}+i_{L2}>0$, Flag_A is set to 1 and then drive signals DRA in Fig. 12(b) are employed to achieve ZVS operation for S_3. On the contrary,

when I_{s3_sample} is larger than zero, Flag_B is equal to 1 and hence drive signals DRB in Fig. 12(b) is utilized to realize ZVS operation for S_1. Therefore, with the control and modulation strategy in Fig. 12, ZVS operation can be achieved for either S_1 or S_3 in the proposed SIDO buck converter over the whole load range. The triangular waveforms $\{V_{t1\_A}, V_{t2\_A}, V_{t3\_A}\}$ and $\{V_{t1\_B}, V_{t2\_B}, V_{t3\_B}\}$ only have difference in their phase relationship. V_{t1_A} is $D_{s3}\times\pi$ in advance of V_{t2_A} and V_{t2_A} is $D_{s1}\times\pi$ in advance of V_{t3_A}, while V_{t1_B} is $D_{s3}\times\pi$ after V_{t2_B} and V_{t2_B} is $D_{s1}\times\pi$ after V_{t3_B}.

From above, the proposed integrated SIDO buck converter in Fig. 10(a) operates similarly with the conventional scheme consisting of two separate buck converters in Fig. 10(b), and their voltage gains, voltage stresses of switches, average inductor currents and small-signal models are also the same. However, the number of switches is reduced, switching losses are decreased and current stresses of switches are improved in the proposed converter, contributing to lower cost and higher efficiency.

(i) Number of switches: Only three switches $S_1 \sim S_3$ are employed in the proposed SIDO buck converter while four switches $S_{11} \sim S_{22}$ are demanded in the conventional converter.

(ii) Switching losses: Because one switch in the proposed converter can always achieve ZVS operation, and the remaining two switches are respectively hard-switching and operating as the synchronous switch. Therefore, in comparison with the conventional two separate buck converters in which two switches are hard-switching and the other two operate as the synchronous switch, switching losses are effectively alleviated in the proposed converter.

(iii) Current stresses: The current stresses of switches $S_{11} \sim S_{22}$ in Fig. 10(b) are calculated in (19). Duty-cycles D_{s11} and D_{s21} are respectively equal to D_{s1} and D_{s3}. Then, combining with the current stresses of switches $S_1 \sim S_3$ in (16), the total RMS currents of switches in the proposed converter ($Total\_rms(Pro)$) and in the conventional converter ($Total\_rms(Con)$) are derived as shown in (20). With the parameters in Table 6, comparison result between the proposed ($Total\_rms(Pro)$) and conventional ($Total\_rms(Con)$) converter is depicted in Fig. 13. From Fig. 13, $Total\_rms$ of the proposed converter is smaller than that of the conventional one over wider load range. And smaller $Total\_rms$ achieved at rated load condition ($I_{L1}=3A$, $I_{L2}=-2A$) also indicates that current stresses of switches are reduced in the proposed converter. In addition, at rated load condition, the square of RMS current of each switch is respectively $I_{s1,rms}^2 = 2.75$, $I_{s2,rms}^2 = 4.25$, $I_{s3,rms}^2 = 1.25$ for the proposed SIDO buck converter and $I_{s11,rms}^2 = 6.75$, $I_{s12,rms}^2 = 1.5$, $I_{s21,rms}^2 = 2$, $I_{s22,rms}^2 = 2$ for the conventional SIDO buck converter. Therefore, the conduction losses are distributed more equal in the proposed converter, which is also beneficial for the thermal design.

$$\begin{cases} I_{s11,rms} = \sqrt{D_{s11}}I_{L1}, \; I_{s12,rms} = \sqrt{(1-D_{s11})}I_{L1} \\ I_{s21,rms} = -\sqrt{D_{s21}}I_{L2}, \; I_{s22,rms} = -\sqrt{(1-D_{s21})}I_{L22} \end{cases} \quad (19)$$

$$\begin{cases} Total\_rms(Pro) = \sqrt{I_{s1,rms}^2 + I_{s2,rms}^2 + I_{s3,rms}^2} \\ Total\_rms(Con) = \sqrt{I_{s11,rms}^2 + I_{s12,rms}^2 + I_{s21,rms}^2 + I_{s22,rms}^2} \end{cases} \quad (20)$$
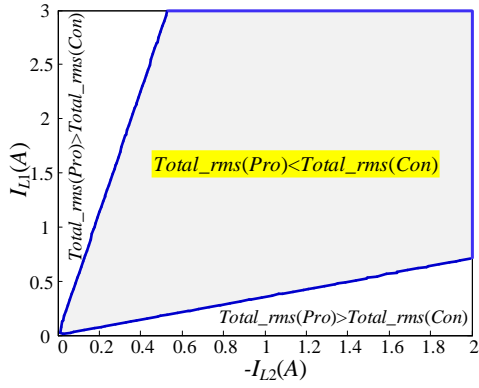
Fig. 13. Comparison between the proposed and conventional SIDO buck converter in terms of total RMS current.

B. Experimental results

Fig. 14 and Fig. 15 respectively show the steady-state waveforms of the proposed converter under condition A: I_{o1}=3A, I_{o2}=2A and condition B: I_{o1}=0.3A, I_{o2}=2A. According to the theoretical analysis, drive signals DRA and DRB should be respectively employed for these two load conditions, as illustrated in Fig. 14(a) and Fig. 15(a). Then ZVS operation is achieved for S_3 under condition A as shown in Fig. 14(d), and it is achieved for S_1 under condition B as shown in Fig. 15(d). Besides, experimental waveforms of inductor currents i_{L1}~i_{L2} and drain-to-source currents i_{s1}~i_{s3} are also demonstrated in Fig. 14(b)~(c) and Fig. 15(b)~(c), which are in well coincidence with the theoretical analysis. It is noted that the spikes of drain-to-source currents i_{s1}~i_{s3} are caused by the normal reverse recovery phenomenon of the parasitic diode of S_2, which operates as a synchronous switch.

Dynamic response of the proposed integrated SIDO buck converter with load variations between half and full rated load, is also shown in Fig. 16(a). Change of i_{o1} mainly has an impact on v_{o1} and nearly has no influence on v_{o2}. Similarly, when i_{o2} varies, v_{o2} is influenced while v_{o1} almost remains unchanged. Therefore, no cross-regulation exists in the proposed converter that two output voltages v_{o1} and v_{o2} are independently controlled. In Fig. 17, measured efficiencies of the proposed and conventional SIDO buck converters are demonstrated. The components of conventional SIDO buck converter use the same ones in Table 6. The voltages/currents of input (V_{in}, I_{in}) and two outputs (V_{o1}, I_{o1}, V_{o2}, I_{o2}) are measured, and then the efficiency $\eta_{eff} = (V_{o1}I_{o1} + V_{o2}I_{o2})/V_{in}I_{in}$ is calculated. Thanks to the improved current stresses and ZVS operation of switches, higher efficiency is achieved in the proposed converter over whole load range, especially for the light load condition in which switching losses are dominant. Photo of the prototype circuit is shown in Fig. 16(b).
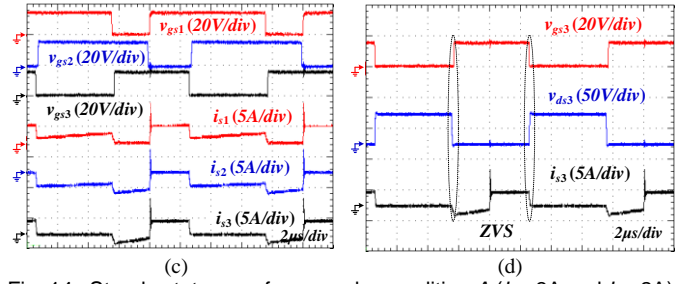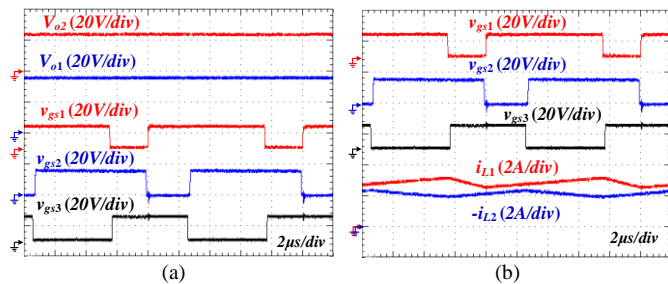

(a) (b)

Fig. 14. Steady-state waveforms under condition A (I_{o1}=3A and I_{o2}=2A): (a) output voltages and drive signals DRA, (b) drive signals DRA and inductor currents, (c) drive signals DRA and drain-to-source currents and (d) ZVS operation of S_3.
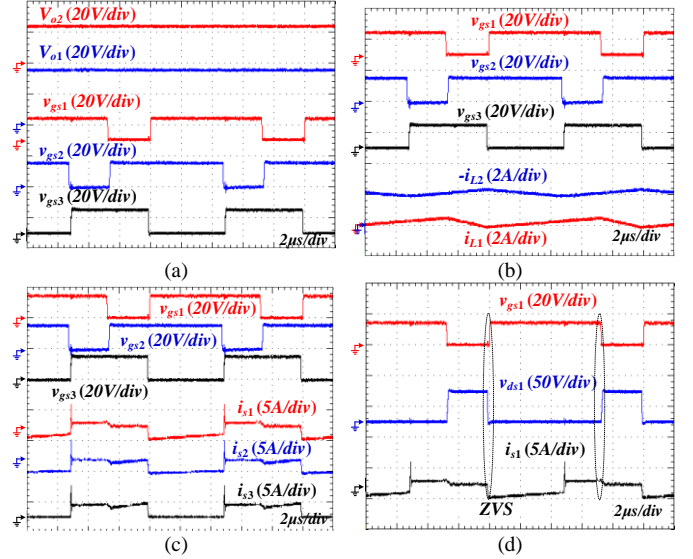

Fig. 15. Steady-state waveforms under condition B (I_{o1}=0.3A and I_{o2}=2A): (a) output voltages and drive signals DRB, (b) drive signals DRB and inductor currents, (c) drive signals DRB and drain-to-source currents and (d) ZVS operation of S_1.
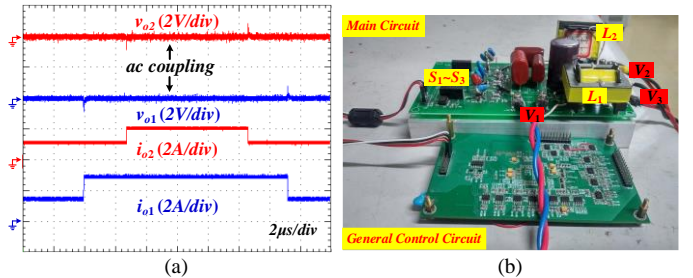

Fig. 16. Dynamic response and the prototype of the proposed integrated SIDO buck converter: (a) dynamic response and (b) prototype.
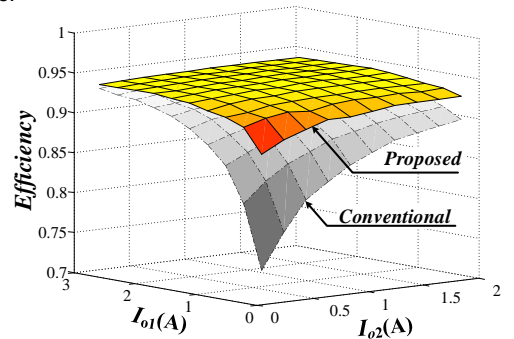

Fig. 17. Measured efficiencies of the proposed integrated and conventional SIDO buck converter.

V. Conclusion

A programmable approach was introduced in the paper to achieve systematic topology derivation and analysis of integrated three-port dc-dc converters, with which 10 viable topologies were conveniently derived from multiple possible connections and their performance characteristics are simultaneously obtained. Because the undesired manual effort is eliminated, the proposed programmable method is beneficial to provide more viable choices for engineers and help to fast select the most preferred one according to the requirement of the real application. And an example application was also detailed illustrated in the paper, which validates that the integrated SIDO buck converter in Fig. 10(a) achieves lower cost and higher efficiency in this application when compared with the conventional two separate buck converters due to the reduced switches number and ZVS operation.

Besides the integrated three-port dc-dc converters, the proposed programmable topology derivation method has also been applied to the other *N*-port converters, such as four-port and five-port dc-dc converters. In the future work, authors will continue to extend this method to other types of converters, aiming to find more favorable new topologies for various engineering applications.

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