Single-Phase Switched-Capacitor Integrated-Boost Five-level Inverter

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***Abstract*— This paper proposes a novel five-level single-phase inverter topology. The inverter uses eight power switches, two capacitors, one inductor, one diode, and a small LC filter at the output. Compared to other multilevel inverters, the proposed inverter can achieve up to 400% more output voltage for the same DC link voltage. As a result, it requires only ¼ of the conventional multilevel inverter topology. The operational states are discussed in brief with the theoretical explanation. A comparison table is illustrated to show the importance of proposed topology compared with existing topologies. The key simulation waveforms and the preliminary experimental results are presented. More explanation of the proposed inverter will be discussed in the final paper.**

Keywords*— Multilevel inverter, LC filter, single-phase photovoltaic (PV) systems.

I. INTRODUCTION

Multilevel inverter nowadays is comprehensively investigated in power electronics applications due to its improved power quality, lower harmonic content, fewer component requirement and high modularity [1]. Increasing the voltage level with achieving the expected outcome, multilevel converter is the best solution. Hence, multilevel converters are used in high power application especially utility application and wind generation systems (WGS). In the case of reducing inverter losses, achieving lower harmonic distortion and electromagnetic interference (EMI), a multilevel inverter can be chosen due to its high performance [2]. Therefore, the attention on multilevel inverter has been increasing significantly in industries for high-power applications such as compressors, pumps, fans, rolling mills, conveyors, gas turbine starters, mixers, mine hoists, marine propulsion, high-voltage direct-current (HVDC) transmission, hydro pumped storage and so on [3] [4] [5] [6]. Owing to numerous advantages of multilevel inverter over the two-level inverter, it has been used in many high-power and voltage applications such as Photovoltaic (PV) [7], wind turbine systems [8], grid-connected systems [9], and motor drive systems [10].

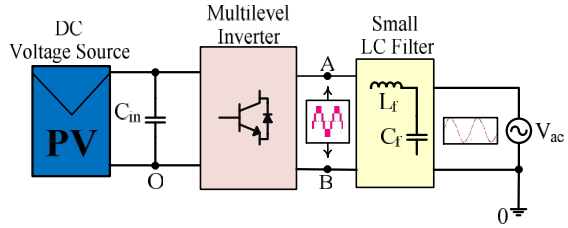

Fig. 1. Multilevel inverter topology along with small LC filter.

Fig. 1 illustrates a multilevel inverter topology. The inverter is connected with a small LC filter to achieve smooth grid connection. The most popular multilevel converters include the neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC) [3]. Five-level active NPC has been introduced by ABB for achieving advantages of multilevel floating capacitor converters which are combined with NPC [4]. The multilevel CHB inverter requires an isolated DC source for each H-bridge and one DC-AC cascaded inverter topology [5], and it attracts more research interest due to the lower number of power electronics devices for producing a higher number of voltage levels. Moreover, one of the advantages of using this topology is without the need of any additional diodes or capacitors [11]. A flying capacitor topology is similar to the NPC multilevel, and it is based on the redundant switch states of the inverter [7]. However, all of these topologies require higher DC-link voltages and the higher number of components for multi-stage power processing.

Considering the above aspects, a novel five-level boost inverter is presented which reduces the DC link voltage requirement with higher efficiency and better power quality. A new multilevel inverter topology with operation principle is presented in Section II. Section III compares existing multilevel inverter topologies with the proposed one. The simulation and preliminary experimental results are shown in Section IV. The paper is summarized and concluded in Section V.

II. PROPOSED INVERTER TOPOLOGY

The proposed five-level inverter topology is shown in Fig. 2(a). It consists of eight switches, one diode, one inductor and two capacitors. The input voltage is boosted with an integrated pre-boost stage. This stage consists of inductor L_B, switch S_B and diode D_B. It is then followed by the switched capacitor voltage doubler circuit with three switches (S_{C1}, S_{C2} and S_{C3}) and two capacitors (C_{S1} andC_{S2}). The switching state of S_B is independent of the switching of the following voltage doubler and unfolding circuit. By appropriately switching the voltage doubler MOSFETs, a precise two-level voltage (V_d and $2V_d$) can be achieved before the unfolding circuit (S_1, S_2, S_3 and S_4). The required level of voltage in C_{S1} and C_{S2} can be precisely controlled by the duty cycle of the switch S_B. The pre-boost stage can be used to track the maximum

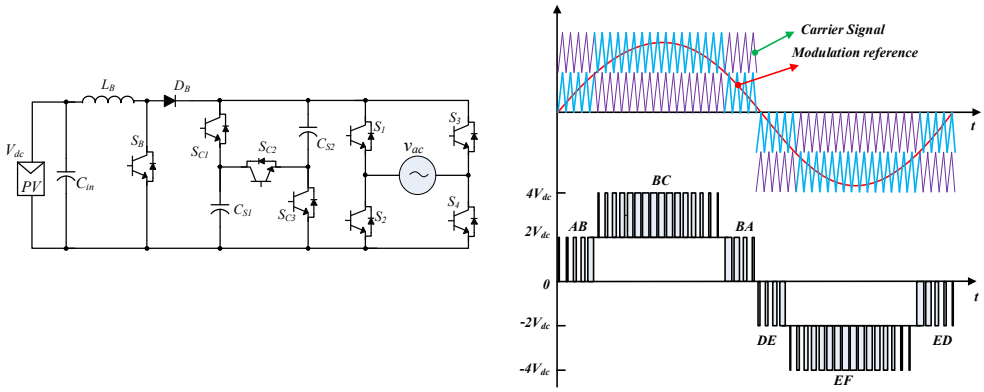

Figure 2. Illustration of (a) the proposed 5-level switched-capacitor single-phase boost inverter, and (b) its required modulation technique.

power point (MPP) of the PV panel, thereby facilitating an integrated and compact solution for grid connected PV systems.

As shown in Fig. 2(b), switching signals are generated by comparing four carrier signals with one reference signal. The proposed inverter circuit is capable to generate five levels of output voltages as +4 V_{dc}, +2 V_{dc}, 0, −4 V_{dc}, and −2 V_{dc} (which are defined as + 2, + 1, 0, – 1, and – 2 respectively).

Table 1 shows the voltage states relation for different switching operation. The operational mode of proposed topology is described below.

III. OPERATION PRINCIPLE OF PROPOSED TOPOLOGY

Fig.3 illustrates the different operation modes of the inverter. Fig 3(a) and Fig. 3(d) display the zero states at level 1 and Fig. 3(e) shows the active states at level 1. Fig. 3(c) and Fig. 3(f) illustrate the active state at level 2. These operating modes are appropriately selected to maintain the five-level voltage at the inverter output, e.g. ABAB for +1 level, BCBC for +2 level, DEDE for -1 level and EFEF for -2 level. These states are discussed below in brief:

Active state 1 (A): Fig. 3 (a) shows the active state 1. In this mode, switch S_B is conducting; hence the current flows from the positive side to negative side of the inductor L_B and through the DC link capacitor C_{i_1} . As a result, inductor L_B is charged. On the other hand, AC current will flow through the switch S_1 and antiparallel diode of switchS_3.

Active state 2 (B): When S_B turns off, current flows through the switches S_{C1} and S_{C3} while the capacitor C_{S1} and C_{S2} will charge continuously until completing the cycle. Moreover, the current flows into the load impedance through S_1 and S_4 switches for the positive half cycle, and the obtained output voltage is +2 V_{dc}. Fig.3 (b) displays this operation.

Active state 3 (C): In this state (Fig. 3(c)), the switches S_{C1} and S_{C3} are in the "off" condition. The capacitors C_{S1} and C_{S2} are in the discharging mode, and the discharging path is from the switch S_{C2} to the switches S_1 and S_4 for the positive half cycle. Hence, it will work until discharging is completed. Indeed, the output voltage is boosted up to four times.

Active state 4 (D): In zero state for the negative half cycle as shown in Fig. 3(d), capacitor switched integrated part is in the "off" condition, and the switch S_B is on. The current flows through the DC link capacitor and inductor. On the other hand, the input side is fully separated from the output side. Hence, the output current flows through the switch S_2, and antiparallel diode of switch S_4 until the positive half cycle starts.

Active state 5 (E): In this state (Fig. 3(e)), the switches S_{C1} and S_{C3} are on, and the capacitors C_{S1} and C_{S2} are charged continuously until the negative half cycle is completed. Meanwhile, the current flows through the switches S_3 and S_2 to the load, and the output voltage is doubled (-2 V_{dc}) relative to the input voltage.

Active state 6 (F): Similar to state 3, -2 level in state 6 (Fig. 3(f)) is generated when the switches S_{C1} and S_{C3} are in the "off" condition. The capacitors C_{S1} and C_{S2} are in the discharging mode. Moreover, the discharging path is from the switch S_{C2} to the switches S_3 and S_2 until the discharging is completed. As a result, the obtained output voltage is four times (-4 V_{dc}) of the input voltage.

TABLE I
OPERATIONAL MODE OF SWITCH WITH VOLTAGE STATES

Mode	Switches							Output Voltage Level
	S_{C1}	S_{C2}	S_{C3}	S_1	S_2	S_3	S_4	
A	0	0	0	1	0	1	0	0
B	1	0	1	1	0	0	1	1
C	0	1	0	1	0	0	1	2
D	0	0	0	0	1	0	1	0
E	1	0	1	0	1	1	0	−1
F	0	1	0	0	1	1	0	−2

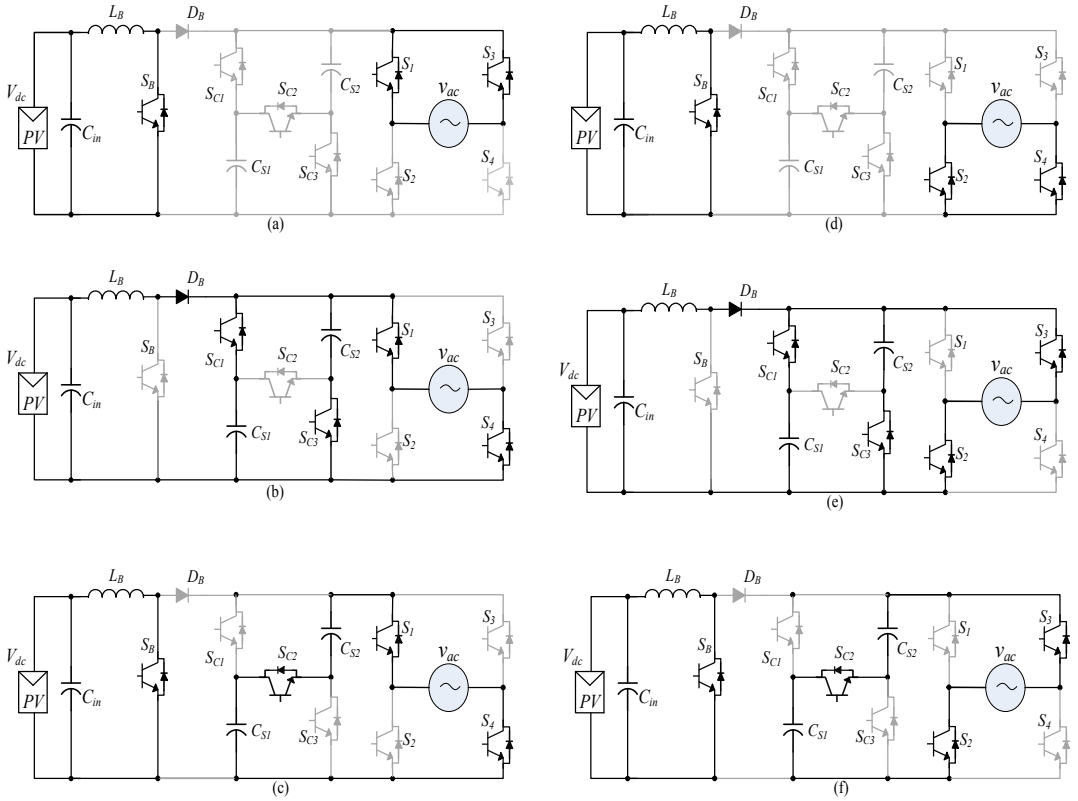

Fig. 3. Operational modes (a) mode A, (b) mode B, (c) mode C, (d) mode D, (e) mode E (f) mode F.

IV. COMPARISON WITH EXISTING TOPOLOGIES

A Multilevel inverter is a high-efficiency based inverter with less total harmonic distortion (THD). However, the main issue is that more power devices are used; hence, the inverter cost, as well as maintenance costs, are increased. Table II below illustrates the comparison of different single-phase multilevel inverter topologies based on the input voltage and power devices. The NPC five-level inverter needs eight power switches and four diodes to achieve five voltage levels, while ANPC and t-type five-level inverter do not need any diodes. Instead, they require additional capacitors. All of these three topologies need 800 V_{dc} to produce the 230 V AC signal. The common five-level inverters, such as diode clamped, FC and CHB are constructed by eight power switches; however, the diode clamped needs extra four capacitors and 12 diodes to achieve five levels of voltage. Table II tabulates the component list of different circuits together with the required number of components for the circuits. All topologies need 400 V DC to achieve the 230 V AC grid voltage. On the other hand, the proposed topology needs only 110 V_{dc} input voltage with one diode, one inductor, two capacitors and eight power switches.

TABLE II
COMPARISON BETWEEN VARIOUS SINGLE-PHASE FIVE LEVEL INVERTER TOPOLOGIES [11-23].

Name	DC Input Voltage (V_{dc})	Semiconductor Devices		Additional Devices	
		Diode	Switch	Inductor	Capacitor
NPC	800	4	8	0	0
ANPC	800	0	8	0	1
T type	800	0	8	0	4
Diode clamped	400	12	8	0	4
Flying capacitor	400	0	8	0	10
Cascaded H-bridge	400	0	8	0	0
Topology in [11]	400	2	8	0	0
Topology in [18] [19]	400	8	6	0	0
Topology in [20]	400	6	11	0	1
Topology in [21]	400	0	6	0	3
Topology in [22]	400	1	9	1	2
Topology in [23]	400	0	9	0	3
Proposed Inverter	110	1	8	1	2

V. SIMULATION AND EXPERIMENT RESULTS

Simulations have been carried out in MATLAB-Simulink using the PLECS toolbox to analyze the inverter operation. Table III shows the parameters for simulation and experimental verification. Simulation result of the novel multilevel inverter is shown in Fig. 4 where the applied input is 110 V_{dc} and an output of 230 V_{ac}, 50 Hz frequency and 1 kW power is achieved. This figure shows the input DC voltage, five-level inverter output, output voltage and current after applying the small LC filter and the voltage across the capacitors (C_{S1} and C_{S2}). On the other hand, Fig. 5 illustrates the voltage across the switches.

In the experimental work, a four-layer printed circuit board (size is 117.221 mm × 114.554 mm) is designed for the 1 kW prototype implementation. The control signals for the switches are provided through the TMS320F28335 digital signal processor from Texas Instruments. Fig. 6 displays prototype of the proposed topology and preliminary result of the proposed inverter for 10 V DC input and 50 Ω load. It shows the five-level output voltage and the output voltage after LC filter..

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TABLE III
PARAMETERS AND COMPONENTS USED FOR SIMULATION AND PROTOTYPE DESIGN.

Parameter/ component	Values used for simulation	Values used for Experiment
DC link Capacitor (C_{in})	680 µF	680 µF (LLS2E681MELA)
Switching Frequency (Fsw)	15 kHz	15 kHz
Line frequency	50 Hz	50 Hz
Boost Inductor (L_b)	0.9 mH	0.9 mH
Boost Diode (D_b)	-	C5D50065D
Switched Capacitors (C_{S1} and C_{S2})	680 µF	680 µF (LLS2E681MELA)
Switches (S_b, S_{C1}, S_{C2}, S_{C3}, S_1, S_2, S_3 and S_4)	-	SCT3022ALGC11
Filter inductor (L_f)	0.40 mH	0.60 mH
Filter Capacitor (C_f)	4.7 µF	4.7 µF
Controller	-	TMS320F28335 DSP

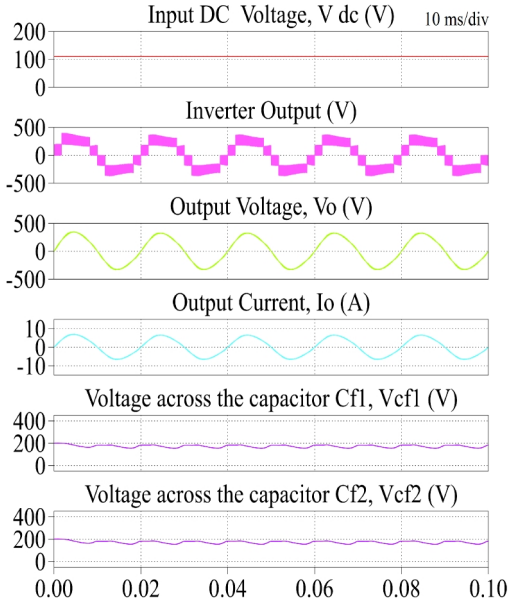

Fig. 4. Output Voltage and Current waveforms of the proposed 5-level inverter with voltage across the capacitors.

VI. CONCLUSION AND FUTURE WORK

In this paper, a novel single-phase 5-level inverter for PV systems is proposed. This topology reduces the DC-link voltage requirement to 1/8 of the conventional multilevel (FC, CHB, NPC, ANPC) and ¼ of the conventional H-bridge topologies. Operational mode of the proposed topology is discussed briefly. Experimental setup of the proposed circuit is constructed, and the preliminary waveform of the 5-level inverter output is achieved. Finally, simulation waveforms of the proposed topology are shown for the experimental setup, and the preliminarily 5-level inverter is achieved for the low input

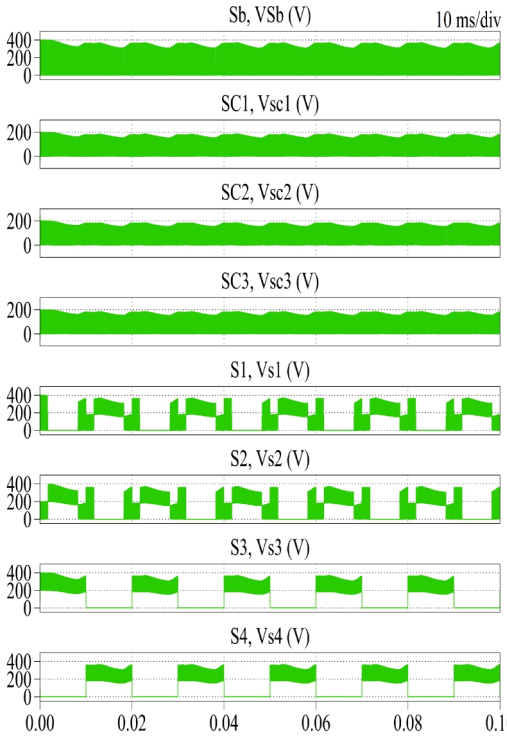

Fig. 5. Voltage across the power switches of the proposed 5-level inverter.

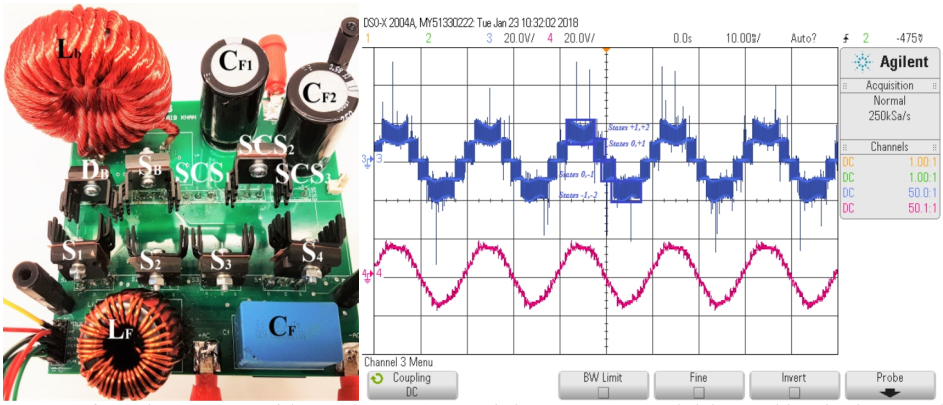

Fig. 6. Hardware setup for a 1 kW prototype of the new inverter (note: switches SCS1, SCS3 and eight gate drive circuits are on the bottom of the PCB), and the preliminary waveforms of the 5-level inverter (20 V/ div).

voltage. In the final version of the paper, more analysis and experimental results will be included with thermal modeling for calculating losses through semiconductor devices and efficiency evaluation.

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