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Model Predictive Observer Based Control for Single-Phase Asymmetrical T-type AC/DC Power Converter

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Abstract

This paper presents a robust control strategy for the control of single-phase five-level asymmetrical T-type (5L-T-AHB) ac/dc power converter. A cascaded control scheme consisting of finite control set model predictive control (FCS-MPC) with an extended state observer (ESO) is proposed to govern the converter. In this scheme, a proportional integral (PI) controller combined with an ESO-based disturbance observer is employed as an external control loop. This control loop dynamically modifies the active power reference to realize the desired operating point for the system state (converter output voltage). The proposed controller offers a high degree of disturbance rejection capability and robustness against the external disturbances to the converter. Whereas the conventional PI control performance suffers in the presence of these disturbances. Moreover, the inner current tracking loop is accomplished by an FCS-MPC algorithm. This algorithm is formulated to force the input currents to track the reference values while realizing a user-defined reactive power and maintaining balanced voltages in the series connected capacitors. Theoretical analysis and the design procedure of the proposed controller are discussed. Finally, experimental studies are conducted to verify the effectiveness of the proposed control scheme.

I. Introduction

In a residential power distribution system, a widely used converter architecture is the single-phase full-bridge two-level ac/dc converter. Contrary to the conventional two-level power converters, multilevel converters (MCs) present more advantages, including the higher quality of output waveforms, higher voltage-handling capability using medium-voltage switching devices, higher power density, and lower switching losses [1-5]. Single-phase MCs have gained popularity in the recent years due to their emerging applications, such as energy storage systems (ESSs), active power filters (APFs), vehicle-to-grid (V2G), grid-to-vehicle (G2V), uninterruptible power supplies (UPSs), and renewable energy conversion systems (RECSs). Consequently, various topologies and control methods have been proposed over the years with a pertinent focus on maintaining high power quality, improving the system dynamic performance and robustness.

Regarding the control of single-phase grid-connected multilevel ac/dc converters, the important control objectives are the reference grid current tracking with the lowest total harmonic distortion (THD), dc-link voltage regulation, and supply of a desired reactive power [6, 7]. The dc-link plays a significant role in the power flow between the utility grid side and the dc-side. Thus, the important control objective is to self-support the dc-link voltage due to the external disturbances and system parameter changes, while preserving the desired reactive power.

The available literature shows that numerous methods have been extensively studied to accomplish these control objectives, including the most conventional voltage oriented control (VOC) methods [8-12]. The dynamic performances of these control methods depend on the tuning of proportional-integral (PI) parameters. The other commonly used techniques are hysteresis controller, dq-axis current controller, and proportional resonant (PR) current controller [13-17]. The dynamic performances of these methods are related to the tuning of PI parameters. Since the ac/dc converters are highly non-linear, the controllers require the system parameters information during the different operating conditions. As the PI coefficients are required to be tuned during the different operation points, these control strategies cannot achieve the required control objectives under external disturbances [18].

Different from the conventional controllers, a widely used strategy is the direct power control (DPC) method [19-22]. This method uses hysteresis comparators and power switching lookup tables. Compared with the traditional control methods, the DPC can realize improved dynamic performances and robustness to achieve dc voltage regulation, and has been extensively applied in three-phase systems [13]. However, constructing an

accurate power switching lookup table is difficult, and hence, may produce high power ripples. As a result, this method affects the steady state performance of the system [23], which limits its application.

Recently, several advanced control methods have been proposed to improve the control performance of the DPC, which include model predictive DPC [24-35], deadbeat DPC [36], and fuzzy logic based DPC [37, 38]. Compared with the direct power and current control methods, predictive control methods provide faster demand tracking speed and generate lower power ripples [27, 28]. MPC based method has been extensively studied in recent years due to its simplicity, free of modulation, flexibility, and options to include nonlinearities and system constraints. However, in a conventional predictive control method, the outer dc-link voltage control is generally governed by a PI controller to generate the active and reactive power reference for the inner MPC-based power control loop. Consequently, the system performance still suffers in the presence of external disturbances due to the use of PI-based dc-link voltage controller. Recently, many nonlinear control approaches have been suggested for controlling three-phase ac/dc power converters, including sliding-mode control (SMC) [16, 39], nonlinear adaptive control [40], and passivity-based control [41]. To the best knowledge of the authors, these methods have been used as the inner current controller, and PI-controller has been used as the dc-link voltage controller. As a consequence, the control performance still suffers because of the uncertainties of external disturbances and system performance still suffers because of the uncertainties of external disturbances and system performance still suffers because of the uncertainties of external disturbances and system methods have been used as the control performance still suffers because of the uncertainties of external disturbances and system parameter variations.

Therefore, it is much desired to design a reliable and robust control strategy to rapidly regulate the dc-link voltage to the required value in the presence of disturbances, which is crucial for grid-connected ac/dc power converters. The available literature shows that the recent control concepts have been applied for the three-phase ac/dc power converter applications. However, as to the authors' knowledge, these controllers' implementation has not been validated for single-phase multilevel converters.

The focus of this work is the design, implementation, and evaluation of a robust control scheme for the fivelevel asymmetrical T-type (5L-T-AHB) ac/dc converter. The 5L-T-AHB converter topology has been proposed in [42, 43], where a new modulation strategy has been proposed to operate as a transformerless grid-connected inverter. Furthermore, a finite control set model predictive control (FCS-MPC) technique has been applied to an extended seven-level topology to operate as an active rectifier [44]. In this paper, an FCS-MPC with a disturbance observer based control technique is proposed to provide a high degree of disturbance rejection capability and robustness against the external disturbances to this converter. Moreover, the capacitor voltage balancing technique and reactive power compensation capability are also included in the proposed cost function formulation. In this scheme, an FCS-MPC is employed as the inner current tracking controller, and a PI controller combined with an ESO based disturbance observer is employed as the outer voltage control loop. This voltage control loop generates the active power reference for the inner FCS-MPC based current tracking controller.

The major novelty of this approach is the PI-ESO based controller design to reject external disturbances and realize a high performance to regulate the dc-link voltage. In this study, the dc-link load resistance of the converter, which influences the dynamics of the system, is considered as the external disturbance. Theoretical analysis is also provided to present the closed-loop behavior of the proposed control scheme. Moreover, an FCS-MPC algorithm is proposed to track the required current reference, while maintaining balanced voltages in the series connected capacitors and achieving a desired reactive power value.

The rest of this paper is organized in the following manner. Section II describes the single-phase grid-connected predictive model of the 5L-T-AHB converter. The FCS-MPC, a multi-objective cost function formulation, PI-ESO based voltage regulation technique, and an adaptive notch filter (ANF) based dc value estimation technique are described in Section III. Section IV presents the experimental results of the 5L-T-AHB converter tested while connected to the grid. Finally, concluding remarks are presented in Section V.

II. System Configuration and Mathematical Model

A. Dynamic model of 5L-T-AHB converter

The circuit configuration of the employed 5L-T-AHB converter is shown in Fig. 1. Based on the circuit configuration, this converter should be controlled to generate five distinct voltage levels in the ac-side to reduce the harmonic content of the grid current with small dv/dt stressing in the semiconductor devices. The following assumptions are made: a) neglecting both conduction and switching losses, b) capacitances C_1 and C_2 have equal values ($C_1 = C_2 = 2C$), and $L_1 = L_2$, ($L = L_1 + L_2$). Considering a charge balance condition, the continuous-

time dynamic model of the converter that defines the dynamical behavior of the converter can be obtained using Kirchhoff voltage law as follows:

$$v_{g} = v_{L_{1}} + v_{L_{2}} + v_{r} + \psi(t)v_{dc} = v_{L} + v_{r} + v_{c}(t)$$
(1)
(1)
$$i_{g} = i_{c} + i$$
(2)

where $v_c(t) = \psi(t)v_{dc}$, v_g is the grid voltage, v_L is the voltage across the filter inductors, v_r is the voltage across the equivalent series resistance of the filter inductors, v_c represents the converter voltage, i_g denotes the grid current, i_c denotes the grid-side capacitor current, and ψ is the control input which takes the values in the finite set from Table I.



Fig. 1. Topology of the 5L-T-AHB converter.

TABLE I

		Po	ossible	e state	es of t	he 5L	L-T-AF	HB conv	verter	
	<i>S1</i>	S2	<i>S3</i>	<i>S4</i>	<i>S5</i>	<i>S6</i>	i_{H1}	i_{H2}	ψ	Vc
•	0	0	0	0	0	0	i	i	1	$+\mathcal{V}DC$
~	0	0	0	0	1	0	0	i	1/2	+ <i>v_{DC}</i> /2
v_{g_g}	0	0	1	0	0	0	0	0	0	0
•	0	0	0	0	0	0	i	i	-1	$-v_{DC}$
\sim	0	0	0	0	0	1	i	0	-1/2	-v _{DC} /2
V_{g}	0	0	0	1	0	0	0	0	0	0

Substituting (2) into (1) yields

$$v_{g} = L\frac{di}{dt} + ri + v_{c}(t) = L\frac{di_{g}}{dt} - LC_{f}\frac{d^{2}v_{g}}{dt^{2}} + r(i_{g} - C_{f}\frac{dv_{g}}{dt}) + v_{c}(t)$$
(3)

where *L* is the grid side filter inductance, and *r* represents the equivalent series resistance of the filter inductor *L*. By using the forward Euler approximation method with a sampling period T_s , (3) can be rewritten as

$$v_{g}^{k} = \frac{L}{T_{s}} \left(i_{g}^{k+1} - i_{g}^{k} \right) - \frac{LC_{f}}{T_{s}^{2}} \left(v_{g}^{k+1} - 2v_{g}^{k} + v_{g}^{k-1} \right) + ri_{g}^{k} - \frac{rC_{f}}{T_{s}} \left(v_{g}^{k+1} - v_{g}^{k} \right) + v_{c}^{k}$$
(4)

where k is discretized t.

Rearranging (4), in terms of the predicted grid current, i_{g}^{k+1} can be expressed as

$$i_{g}^{k+1} = \left(1 - \frac{rT_{s}}{L}\right)i_{g}^{k} + \left(\frac{C_{f}}{T_{s}} + \frac{rC_{f}}{L}\right)v_{g}^{k+1} + \left(\frac{T_{s}}{L} - \frac{2C_{f}}{T_{s}} - \frac{rC_{f}}{L}\right)v_{g}^{k} + \frac{C_{f}}{T_{s}}v_{g}^{k-1} - \frac{T_{s}}{L_{f}}v_{c}^{k}$$
(5)

where v_g^{k+1} can be obtained as [45]

$$v_g^{k+1} = 3v_g^k - 3v_g^{k-1} + v_g^{k-2}$$
(6)

The 5L-T-AHB converter topology consists of a single dc-link in parallel with the series connected capacitors. Therefore, it is required to integrate the voltage balancing technique into the control method to ensure equal capacitor voltages (i.e. $v_{c_1} = v_{c_2} = \frac{v_{dc}}{2}$) to generate five distinct voltage levels in the ac-side. The dynamic equations for the capacitor voltages are expressed as follows

$$C_{1} \frac{dv_{C_{1}}}{dt} = i_{C_{1}} = i_{H_{1}} - i_{dc} = i_{H_{1}} - \frac{v_{C_{1}} + v_{C_{2}}}{R}$$

$$C_{2} \frac{dv_{C_{2}}}{dt} = i_{C_{2}} = i_{H_{2}} - i_{dc} = i_{H_{1}} - \frac{v_{C_{1}} + v_{C_{2}}}{R}$$

$$(8)$$

where i_{C_1} and i_{C_2} represent the currents through the capacitors C_1 and C_2 respectively, i_{H_1} and i_{H_2} represent the internal currents of the converter, R denotes the equivalent load resistance value, and i_{dc} denotes the dc-side current.

According to the MPC requirements, the present values of i_g , v_g , v_{c_1} , and v_{c_2} are required to predict the future behavior of i_g . The capacitor voltages balancing of the employed converter is also a control objective. The predictive values of the capacitor voltages of this converter can be presented in discrete-time form using the classical forward Euler method as follows

$$v_{C_1}^{k+1} = v_{C_1}^{k} + \frac{T_s}{C_1} i_{H_1}^{k} - \frac{T_s}{C_1} i_{dc}^{k}$$
(9)

$$v_{C_2}^{k+1} = v_{C_2}^{k} + \frac{T_s}{C_2} i_{H_2}^{k} - \frac{T_s}{C_2} i_{dc}^{k}$$

(10)

The measured values of i_{H_1} and i_{H_2} can be obtained from the individual switching functions as shown in Table I, and thus unnecessary measurements of i_{H_1} and i_{H_2} can be avoided. Therefore, to predict the future behavior of the grid-current and the capacitor voltage values, (5), (9), and (10) will be used by the proposed controller.

B. D-Q mathematical model

The grid voltage v_g , the inductor current *i*, and the converter voltage v_c of the employed converter are defined as follows

$$v_g = v_d \sin(\omega t) + v_q \cos(\omega t) \tag{11}$$

$$i = i_d \sin(\omega t) + i_a \cos(\omega t) \tag{12}$$

$$v_c = v_{cd}\sin(\omega t) + v_{cq}\cos(\omega t)$$
⁽¹³⁾

where v_d , i_d and v_{cd} are the *d*-axis components, and v_q , i_q and v_{cq} are the *q*-axis components of the grid voltage, the inductor current, and the converter voltage vectors v_g , *i*, and v_c respectively in *dq* rotating frame.

The equivalent circuit of the employed converter is shown in Fig. 2. The dynamic model of the employed converter in the dc-side is given by

$$C\frac{dv_{c}}{dt} = i_{c} = i_{s} - i_{load} - i_{R_{s}} = i_{s} - \frac{v_{dc}}{R_{load}} - \frac{v_{dc}}{R_{s}}$$
(14)

where R_S represents the switching loss of the converter and R_{load} denotes the equivalent load resistance value.

The inductor current *i* and grid voltage v_g can be decomposed in their *d* and *q* parts at the grid frequency. Thus, (1) and (14) will become

$$L\frac{di_d}{dt} = v_d - i_d r + i_q \omega L - v_{cd}$$
⁽¹⁵⁾

$$L\frac{di_q}{dt} = v_q - i_q r - i_d \omega L - v_{cq}$$
(16)

$$C\frac{dv_c}{dt} = i_s - i_{load} - i_{R_s} \tag{17}$$

Considering the system is in the steady state condition, according to the energy conservation law, the input power from the utility grid must be equal to the power consumed by the load, the semiconductor switching losses, and the capacitor charging power. The reference value of the output voltage is v_{dc} . Therefore i_s can be expressed as

$$i_s = \frac{v_d i_d + v_q i_q}{2v_{dc}} \tag{18}$$

From (17) and (18), we have

$$C\frac{dv_{c}}{dt} = \frac{v_{d}\dot{i}_{d} + v_{q}\dot{i}_{q}}{2v_{dc}} - \frac{v_{dc}}{R_{load}} - \frac{v_{dc}}{R_{s}} = \frac{1}{v_{dc}}(p^{*} - p_{load} - p_{R_{s}})$$
(19)
where $p_{load} = \frac{v_{dc}}{R_{load}}, p^{*} = \frac{1}{2}(v_{d}\dot{i}_{d} + v_{q}\dot{i}_{q}) = v_{dc}\dot{i}_{s}, p_{R_{s}} = \frac{v_{dc}^{2}}{R_{s}}$

Equations (16), (17) and (20) can be written in a state-space form as follows

$$\begin{bmatrix} \dot{i}_{d} \\ \dot{i}_{q} \\ \dot{v}_{c} \end{bmatrix} = \begin{bmatrix} -\frac{r}{L} & \omega & 0 \\ -\omega & -\frac{r}{L} & 0 \\ \frac{v_{d}}{2v_{dc}C} & \frac{v_{q}}{2v_{dc}C} & -\left(\frac{1}{CR_{load}} + \frac{1}{CR_{s}}\right) \end{bmatrix} \begin{bmatrix} \dot{i}_{d} \\ \dot{i}_{q} \\ v_{c} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{d} - v_{cd} \\ v_{q} - v_{cq} \end{bmatrix}$$
(20)



Fig. 2. Equivalent circuit of the 5L-T-AHB converter.

III. Proposed Control Scheme

This section covers the demonstration of the proposed control scheme. The block diagram of the proposed controller is illustrated in Fig. 3. The control objectives concerning the single-phase 5L-T-AHB converter are to regulate the dc-link voltage and provide the desired reactive power. The dc-link voltage of the power converter is determined by the active power. Therefore, in the dq rotating frame, the *d*-axis component (i_d^*) of the current *i* is computed dynamically to maintain the desired output voltage. Similarly, the instantaneous reactive power is determined by the *q*-axis component (i_q^*) of the current *i*. Hence, the converter currents (*d*-axis component (i_d) and *q*-axis component (i_q)) should follow the dynamically calculated references i_d^* and i_q^* respectively to realize the desired control objectives. Note that the dc-link voltage of the ac/dc converters is affected by the external load disturbances. To achieve the dynamic voltage regulation in the presence of active power reference for the MPC-based inner current control loop. For the employed converter, the MPC with finite control set (FCS-MPC) is used to define the state of this converter in each sampling period. The FCS-MPC offers several advantages, including the possibility to realize multiple control objectives, handling system constraints and the option to include nonlinearities.



Fig. 3. Block diagram of the proposed ESO-based ac/dc converter control system.

A. FCS-MPC for 5L-T-AHB power converter

The FCS-MPC algorithm has been derived for current control in 5L-T-AHB converter drives. The objectives of the controller are to track the current reference (i_g^*) , and to balance the series connected capacitor voltages. The current i_g^* is computed from the active power dynamic reference (u^*) obtained from PI-ESO controller and the desired reactive power (q^*) values. To accomplish this purpose, the FCS-MPC scheme operates in discrete time and uses the discrete model of the converter which is presented in Section II. The measured system states are used for the state predictions of the control variables for the employed converter model. The state predictions are then evaluated for each of the possible switching states to provide the best performance. It is based on an optimization criterion and uses a cost function which considers the design constraints. Among these switching states, the one which minimizes the cost function is applied to drive the employed converter.

B. Multi-objective cost function formulation

In the conventional MPC algorithm to control the single-phase two level converters, the predicted values of the grid current reference at the instant (k + 1) is calculated at each sampling instant by using (5) for each of the possible switching states. Among these switching states, the one which minimizes the cost function defined in (21) is selected and then applied to the power converter till the next sampling instant.

$$g_{conv} = \left| i_{g}^{*k+1} - i_{g}^{k+1} \right|$$
(21)

Only the grid-current variable is usually taken into account in the cost function defined in (21) to generate different voltage levels. Thus, the weighting factor selection and tuning process are not necessary. However, for the employed multilevel converter, the multilevel voltage synthesizing will be affected by this strategy due to voltage unbalancing problem that occurs in the series connected capacitors. Therefore, for this particular multilevel power converter, it is important to maintain balanced voltage across the series connected capacitors to generate five distinct voltage levels in the ac-side. The proposed cost function for the adopted 5L-T-AHB converter is defined as

$$g_{conv} = \lambda_i \left(i_g^{*k+1} - i_g^{k+1} \right)^2 + \lambda_v \left(v_{C_1}^{k+1} - v_{C_2}^{k+1} \right)^2$$
(22)

The trade-off between the capacitor voltage balancing and the grid-current waveform quality can be realized by adjusting the weighting factors λ_i and λ_v in (22). It can be observed that a large value of λ_v will take sides in the capacitor voltage balancing by paying the penalty of low THD of the line current, i.e., the line current THD will be affected by the capacitor voltage balancing. In this paper, the weighting factors are formulated as follows

$$\lambda_{v} = \frac{p^{*}}{V_{dc}^{2}}$$
(23)

$$\lambda_i = 1$$
(24)

where p^* is the active power reference calculated from the PI-ESO controller.

In (22), the grid-current reference i_g^{*k+1} computation is important to realize the required control objectives, which is explained in the following subsection.

C. Reference grid current calculation

In a single-phase system, a virtual two-phase system is usually generated to calculate the instantaneous active and reactive power. The second-order generalized integrator (SOGI) is a widely employed method to generate the orthogonal signal of the single-phase voltage and current signals. The transfer functions of SOGI in *s*domain are expressed as follows

$$x_{\alpha}(s) = \frac{k\omega s}{s^{2} + k\omega s + \omega^{2}} x(s)$$
(25)
$$x_{\beta}(s) = \frac{k\omega^{2}}{s^{2} + k\omega s + \omega^{2}} x(s)$$

(26)

where k represents the damping factor.

The performance of SOGI is related to the tunning of parameter k. Applying (25) and (26) to the grid voltage v_g and the current i_g , the orthogonal component of the voltage v_g and current i_g can be presented as follows

$$v_{g-\alpha} = V_g \sin(\omega t)$$
(27)
$$v_{g-\beta} = V_g \sin\left(\omega t + \frac{\pi}{2}\right)$$
(28)
$$i_{g-\alpha} = I_g \sin(\omega t + \phi)$$
(29)
$$i_{g-\beta} = I_g \sin\left(\omega t + \phi + \frac{\pi}{2}\right)$$
(30)

According to the instantaneous power theory, the active power p^k and the reactive power q^k of single-phase system are defined as

$$\begin{bmatrix} p^{k} \\ q^{k} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{g-\alpha} & v_{g-\beta} \\ k & v_{g-\beta} & -v_{g-\alpha} \end{bmatrix} \begin{bmatrix} i_{g-\alpha} \\ i_{g-\beta} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{g-d} & v_{g-q} \\ k & v_{g-q} & -v_{g-d} \end{bmatrix} \begin{bmatrix} i_{g-d} \\ i_{g-q} \end{bmatrix}$$
(31)

where $v_{g-\alpha}$, $v_{g-\beta}$, $i_{g-\alpha}$, $i_{g-\beta}$, are the α -axis and β -axis components of the grid voltage and the line current in the two-phase $\alpha - \beta$ stationary reference frame, respectively. v_{g-d} , v_{g-q} , i_{g-d} , and i_{g-q} are the *d*-axis and *q*-axis components of the grid voltage and the line current in the *dq* rotating frame, respectively.

The grid voltage is oriented to *d*-axis in synchronous reference frame. Thus, the grid-side instantaneous active power p^k and reactive power q^k are given by

$$p^{k} = \frac{1}{2} v_{g-d}^{k} i_{g-d}^{k}$$
(32)
$$q^{k} = -\frac{1}{2} v_{g-d}^{k} i_{g-q}^{k}$$
(33)

To calculate the reference grid current, the quantities in rotating reference frame in (32) and (33) are used. Therefore, the expression for reference grid current is given by [46]:

$$i_{g}^{k} = i_{g-q}^{k} \cos(\theta) + i_{g-d}^{k} \sin(\theta)$$
(34)

The quantities $sin(\theta)$ and $cos(\theta)$ in (34) can be obtained by using phase locked-loop (PLL). In this paper, a dc offset rejection capability based PLL [47] has been used. The block diagram of the employed PLL is illustrated in Fig. 4.



Fig. 4. DC- offset rejection based SOGI-PLL.

Finally, using (32) - (34), the grid-current references is obtained as

$$i_{g}^{k} = \frac{2p^{k}}{v_{g-d}^{k}}\sin(\theta) - \frac{2q^{k}}{v_{g-d}^{k}}\cos(\theta)$$
(35)

D. ESO-based disturbance observer design

The proposed control scheme includes an ESO as a disturbance observer in the dc-link voltage control loop. This observer has been used to compensate the total system disturbances f_t to the converter that consists of the external disturbance p_{load} and plant dynamic variation p_{R_s} . Finally, the observed value \hat{f}_t has been used to compensate the control output μ_{dc} . Therefore, the resulted control output $p^* = u$, can be written as

$$u = \mu_{dc} + \hat{f}_t$$

(36)

where \hat{f}_t is the observed value obtained from the ESO and μ_{dc} is the PI controller output defined as

$$\mu_{dc}(e_{dc}) = k_1 e_{dc} + k_2 \int e_{dc} dt$$
(37)

where the voltage regulation error $e_{dc} = z_1 - z_1^*$ with $z_1 = \frac{(v_{dc})^2}{2}$ and $z_1^* = \frac{(v_{dc}^*)^2}{2}$.

Using (19), the dynamic of z_1 can be expressed as

$$C\frac{dz_{1}}{dt} = (p^{*} - p_{load} - p_{R_{s}}) = p^{*} - f_{t}$$
(38)
where $f_{t=}p_{load} + p_{R_{s}}$.

Using (38), we have

$$C\frac{dz_1}{dt} = u - z_2$$
(39)
where $p^* = u$ and $f_t(t) = z_2$

The disturbance z_2 is treated as an extended state. Furthermore, the time derivative of z_2 is denoted *h*. Therefore, we have

$$\frac{dz_2}{dt} = h(t) \tag{40}$$

Hence, based on the above-mentioned analysis, the state-space model is derived as follows

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \end{bmatrix} = \begin{bmatrix} 0 & -1/C \\ 0 & 0 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \end{bmatrix} + \begin{bmatrix} 1/C \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h$$
(41)

Using (41), the ESO can be designed as follows

$$\begin{bmatrix} \dot{\hat{z}}_1 \\ \dot{\hat{z}}_2 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{z}_1 \\ \hat{z}_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{C} \\ 0 \end{bmatrix} u + \begin{bmatrix} \beta_1 \\ C \\ -\beta_2 \end{bmatrix} \begin{bmatrix} z_1 - \hat{z}_1 \end{bmatrix}$$
(42)

where \hat{z}_1 and \hat{z}_2 are the estimated values of z_1 and z_2 respectively, β_1 and β_2 are positive gains of ESO.

E. Parameter Tuning and Stability Analysis

By subtracting (42) from (41), the error dynamics can be expressed as

$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \end{bmatrix} = \begin{bmatrix} -\beta_1 / & -1 / C \\ \beta_2 & 0 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h$$
(43)

where $e_1 = z_1 - \hat{z}_1$ and $e_2 = z_2 - \hat{z}_2$

From (43), the gains β_1 and β_2 should be selected such that the roots of the characteristic polynomial of *A*, i.e., $\lambda(s) = s^2 + \frac{\beta_1}{c}s + \frac{\beta_2}{c}$ are in the left half-plane for Hurwitz stable.



Fig. 5. Equivalent transfer function of extended state observer.

Based on (38), we have

$$C\frac{dz_{1}}{dt} = p^{*} - p_{load} - \frac{2z_{1}}{R_{s}}$$
(44)

Using Laplace transformation, (44) can be expressed as

$$z_1(s) = \frac{R_s}{R_s C s + 2} p^*(s) - \frac{R_s}{R_s C s + 2} p_{load}(s)$$
(45)

After mathematical simplifications, the ESO can be expressed as follows

$$\begin{bmatrix} \dot{\hat{z}}_1 \\ \dot{\hat{z}}_2 \end{bmatrix} = \begin{bmatrix} -\beta_1 / c & -1 / c \\ \beta_2 & 0 \end{bmatrix} \begin{bmatrix} \hat{z}_1 \\ \hat{z}_2 \end{bmatrix} + \begin{bmatrix} 1 / c & \beta_1 / c \\ 0 & -\beta_2 \end{bmatrix} \begin{bmatrix} u \\ z_1 \end{bmatrix}$$
(46)

Based on Fig. 5 and (46), the expressions for G_{f_t-u} and $G_{f_t-z_1}$ are given as follows

$$G_{f_{t}-u} = \frac{f_{t}(s)}{u(s)} = \frac{\beta_{2}}{Cs^{2} + \beta_{1}s + \beta_{2}}$$
(47)
$$G_{f_{t}-z_{1}} = \frac{f_{t}(s)}{z_{1}(s)} = \frac{-\beta_{2}Cs}{Cs^{2} + \beta_{1}s + \beta_{2}}$$
(48)

Using (47) and (48), the transfer function of the observer can be expressed as follows

$$\hat{f}_{t}(s) = \frac{\beta_{2}}{Cs^{2} + \beta_{1}s + \beta_{2}}u(s) - \frac{\beta_{2}Cs}{Cs^{2} + \beta_{1}s + \beta_{2}}z_{1}(s)$$
(49)

Therefore, the revised model from the controller output u_0 to the $z_1(s)$ is given as follows

$$\overline{G}_{p}(s) = \frac{z_{1}(s)}{u_{o}(s)} = \frac{G_{p}}{1 - G_{u} - G_{Z_{1}}G_{p}}$$

$$= \frac{R_{s}}{(CsR_{s} + 2)\left(\left(\frac{\beta_{2}CsR_{s}}{(CsR_{s} + 2)(Cs^{2} + \beta_{1}s + \beta_{2})}\right) - \left(\frac{\beta_{2}}{(Cs^{2} + \beta_{1}s + \beta_{2})}\right) + 1\right)$$
where $G_{p} = \frac{R_{s}}{R_{s}Cs + 2}$ and u is the output of the controller. (50)

 R_sCs+2

The adopted controller performance and stability of the system are affected by the dc-side capacitance variations. To evaluate the robustness of the system, the closed loop poles of $\overline{G_P}$ have been studied for the dclink capacitance variations from 0.002 F to 0.004 F. The root loci of the system model $\overline{G_P}$ for this capacitance variation are illustrated in Fig. 6. According to the figure, it is observed that the pole moves in the direction of the imaginary axis as the capacitances vary from 0.002 F to 0.004 F. As a result, the system becomes oscillatory with a reduced damping when the capacitance increases. However, the system presents robustness against the capacitance variations, because the pole location is still far away from the imaginary axis.



Fig. 6. Root loci of the proposed system for the change of capacitance value.

F. ANF based dc value estimation of the dc-link voltage

In a single-phase system, the instantaneous grid voltage and current are given by

$$v_g(t) = V_g \sin(\omega t)$$
(51)

 $i_g(t) = I_g \sin(\omega t + \phi)$ (52)

Therefore, the instantaneous power can be expressed as [48]:

$$p_{g,inst} = \frac{1}{2} V_g I_g \cos(\phi) - \frac{1}{2} V_g I_g \cos(\phi) \cos(2\omega t) + \frac{1}{2} V_g I_g \sin(\phi) \sin(2\omega t)$$

$$= P - P\cos(2\omega t) + Q\sin(2\omega t)$$

(53)

where $P = \frac{1}{2}V_g I_g \cos(\phi)$, and $Q = \frac{1}{2}V_g I_g \sin(\phi)$.

The proposed control scheme feeds back the dc-link voltage signal to the controller. As the single-phase ac/dc converter has the double harmonic pulsating power ripple, the output voltage will have an intrinsic double line frequency ac ripple component superimposed on top of the dc-link. Therefore, the dc-bus voltage can be described as

$$v_{bus} = V_{dc} + V_{ripple} \sin(2\omega t)$$
(54)

This low frequency ripple signal propagates into the closed-loop control system. Therefore, it causes challenge to estimate the active power reference to track the reference dc-link voltage, which degrades the system dynamic performances and increases the current harmonics as well.

Conventionally, low-pass filter (LPF) is employed to filter out this ripple term. A very low cutoff frequency should be selected during the LPF design procedure to suppress the double-frequency ripple term completely, which causes a high phase delay in the control loop and hence, slows down the transient response. Therefore, extracting the dc value of the dc-link voltage signal with low-frequency ripple component is challenging. In this work, ANF is employed to estimate the dc-value and provide better dynamic performance. The characteristic equations of the employed ANF are given as follows [49]:

$$\ddot{x} + \theta^{2}x = 2\zeta \theta(y(t) - \dot{x})$$
(55)
$$\dot{\theta} = -\gamma x \theta(y(t) - \dot{x})$$
(56)
$$\gamma = \frac{\varepsilon}{(A^{2} + 1)(\theta^{2}\mu + 1)}$$
(57)

where y(t) represents the input signal, θ denotes the estimated second harmonic frequency, γ denotes the adaptation gain parameter, ζ represents the depth of the notch and γ represents the adaptation speed, μ and ε are variable positive parameters, and A denotes amplitude of the signal. For a single sinusoid input signal (n = 1), the ANF has a unique periodic orbit located at

$$o = \begin{pmatrix} x \\ \dot{x} \\ \theta \end{pmatrix} = \begin{pmatrix} -\frac{A_1}{\omega_1} \cos(\omega_1 t + \varphi_1) \\ A\sin(\omega_1 t + \varphi_1) \\ \omega_1 \end{pmatrix}$$

(58)

IV. Experimental Results

This section presents the experimental results obtained by using the proposed control scheme. To verify the performance of the proposed control technique, a prototype of the 5L-T-AHB converter was built and tested with the specifications listed in Table II. The experimental setup is shown in Fig. 7. The control algorithm is programmed in TMS320F28379D. The time required by the different control tasks of the proposed algorithm is presented in Table IV, which was measured by using the feature existing in the Code Composer Studio from Texas Instruments. A timer is programmed to acquire the voltage and current sensors data with a sampling frequency of 50 kHz. The experimental waveforms of the converter are illustrated in Fig. 8. As it can be seen that the maximum switching frequency of the converter is 25 kHz with the derived FCS-MPC control algorithm.



Fig. 7. Experimental setup.

The dc-value tracking performance of the dc-link voltage signal with the employed ANF is presented in Fig. 9. Clearly, the employed ANF can precisely estimate the dc-value and provides fast transient performance in estimating the dc-value during any change in the dc-link voltage.



Fig. 8. (a) Experimental results of the voltage produced by the 5L-T-AHB ac/dc converter, input current, and dc-link voltages for operation as an active rectifier, (b) magnified view of the voltage and current waveforms.



Fig. 9. ANF performance in estimating the dc value of the dc-link voltage.

The performance of the proposed control technique was evaluated under the different scenarios, including (a) capacitor voltages balancing performance, b) dc-link voltage tracking performance, (c) a load step at dc-link, and (d) reactive power compensation capability.

The performance of the proposed PI-ESO based control method is also compared with the PI-based control method with the same PI parameters and MPC-based inner current control loop, which is implemented to provide a base for comparison. For the PI-based method, the PI control parameters are adjusted through trial and error method to achieve better performance in terms of the speed of convergence and smaller overshoot. The parameters of the PI controller and ESO are presented in Table III.

To evaluate the capacitor voltage balancing performance of the derived FCS-MPC scheme, the reference dc-link voltage is set to 80 V. Therefore, each capacitor voltage should be divided into 40 V to generate five distinct voltage levels in the ac side. Fig. 10 shows the experimental results when the capacitor voltage balancing scheme is ignored in the cost function formulation. In this situation, the lower capacitor voltage level is decreased to around 10 V and the upper capacitor voltage is charged to around 70 V, as time goes by. Consequently, only three voltage levels are observed in the ac side. This is due to insufficient charging time to charge up the lower capacitor. Fig. 11 demonstrates the capacitor voltages with the formulated cost function in FCS-MPC, where each capacitor voltage is maintained at near $V_{ref}/2$, and consequently, five distinct voltage levels are observed in the ac-side.



Fig. 10. Experimental performances with the general FCS-MPC scheme, and the capacitor voltages unbalancing and its influence on the output voltage levels.



Fig. 11. Experimental performances with the proposed FCS-MPC scheme.

To assess the dynamic performance of the dc-link voltage tracking controller, a step variation in the reference dc-link voltage is introduced from 70 to 80 V, and after that the reference voltage is changed back to 70 V. The inner current tracking controller (FCS-MPC) remains the same. Figs. 12(a) and (b) show the results associated with the PI-ESO and PI methods, respectively for a step change in the reference dc-link voltage from 70 to 80 V. Both controllers can realize the dc-link voltage regulation. Comparing Fig. 12(a) with Fig. 12(b), a smaller overshoot is observed with the PI-based control method. Figs. 12(c) and (d) show the results for a step change in the reference dc-link voltage from 80 to 70 V with the PI-ESO and PI methods, respectively. Both controllers can reach the required dc-link voltage reference as desired. As it can be seen that, with the PI-based method the settling time is roughly double compared with the proposed method.





Fig. 12. Comparative study of the proposed PI-ESO-based control strategy, and PI control strategy when a step change in the dc-link voltage references is introduced; (a) PI-ESO (70 V to 80 V), (b) PI (70 V to 80 V), (c) PI-ESO (80 V to 70 V), (d) PI (80 V to 70 V).

To evaluate the dynamic behavior of dc-link voltage under external step load change, the dc-link voltage is set to 70 V and a step resistive load changes from 70 Ω to 50 Ω , and after that 50 Ω to 70 Ω is connected to the dc-link.

Figs. 13(a) and (b) show the results associated with the PI-ESO and PI methods, respectively, for a step resistive load changes from 70 Ω to 50 Ω . Clearly, the proposed PI-ESO demonstrates the best disturbance-rejection

performance to regulate the dc-link voltage with the less voltage drop and zero steady state error. Whereas for the PI controller, the settling time is roughly double compared to PI-ESO based control scheme, and steady-state error is also observed for this step load changes. Figs. 13(c) and (d) show the results for a step resistive load changes from 50 Ω to 70 Ω with the PI-ESO and PI methods, respectively. It can be observed that the PI-ESO method achieves a better transient response while the PI-based method shows steady state error, which points out that the ESO disturbance observer improves the dc-link voltage control performance.



(b)



Fig. 13. Comparative study of the proposed PI-ESO-based control strategy, and PI control strategy when a step change in the dc-link voltage references is introduced; (a) PI-ESO (70 Ω to 50 Ω), (b) PI (70 Ω to 50 Ω), (c) PI-ESO (50 Ω to 70 Ω), (d) PI (50 Ω to 70 Ω).

Fig. 14 shows the experimental results of the proposed controller when the employed converter is realizing the reactive power compensation operation, while keeping the dc-link voltage to its desired reference value.



Fig. 14. Experimental waveforms for reactive power compensation of the 5L-T-AHB ac/dc converter.

SPECIFICATIONS OF THE EXPERIMENTAL SETUP				
Parameters	Value	Unit		
Sampling frequency	50	kHz		
Maximum switching	25	kHz		
frequency				
dc-link capacitor	2.0	mF		
Filter capacitor	1.0	μF		
Filter inductor	3.0	mH		
Input ac voltage (V_m)	70	V		
Grid Frequency	50	Hz		
Controller	TMS320F28379D			
Voltage sensor	LV 25-P/SP5			
Current sensor	LA 25-NP			
Switch	SCT3022ALGC11			
Diode	HFA15PB60			

 TABLE II

 Specifications of the Experimental Setup

TAI	BLE III
CONTROLLER DE	ESIGN PARAMETERS
Parameters	Values
DI momomotore	k = 0.2 k = 5

PI parameters	$k_{\rm p} = 0.2, k_{\rm i} = 5$
ESO parameters	$\beta_1 = 0.4, \ \beta_2 = 20$

TABLE IV TIME REQUIRED BY DIFFERENT TASKS OF THE CONTROL ALGORITHM

Task	Value	Unit
PLL Synchronization	197	ns
Adaptive notch filter	78	ns
MPC	514	ns
PI-controller	26	ns
Current reference generation	29	ns
ESO	53	ns
ADCs reading	48	ns
Gate pulses	163	ns

V. Conclusion

A cascaded control scheme consisting of FCS-MPC with the PI-ESO to drive a single-phase 5L-T-AHB converter was proposed to improve the disturbance rejection capability. With the proposed control strategy, the current control loop was designed to track the reference currents by using the derived FCS-MPC algorithm, while maintaining the balanced capacitor voltages and reactive power reference. The key novelty of this approach is the active power reference design with the ESO-based disturbance observer to improve the dc-link voltage tracking performance in the presence of external disturbances. Compared with the traditional PI-based controller, this scheme presents a faster dynamic response in reducing settling time, and presents zero steady state error under an unexpected step load condition and a step variation in the dc-link voltage reference. The effectiveness of the proposed control scheme has been verified by experimental results.

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