Power Flow Control in Multi-Terminal HVDC Grids using a Serial-Parallel DC Power Flow Controller

Kumars Rouzbehi[1,3], *Senior Member, IEEE*, **Seyed Saeid Heidary Yazdi[2]**, *Member, IEEE* **and** Negin Shariati[3], *Member, IEEE*

1 University Loyola Andalucía, Seville, Spain
2 Amirkabir University of Technology, Tehran, Iran
3 University of Technology Sydney, Australia

Corresponding author: Kumars Rouzbehi (e-mail: krouzbehi@uloyola.es)

ABSTRACT Multi-Terminal HVDC (MT-HVDC) grids have no capability of power flow control in a self-sufficient manner. To address this important issue, utilization of DC-DC high power and high voltage converters is motivated. However, proposing suitable partial-rated DC-DC converters as well as their suitable modeling and control in both primary and secondary control layers as well as the stability analysis are the existing challenges that should be alleviated beforehand. This research addresses the control of power flow problem through application of a power converter with a different connection configuration, namely Serial Parallel DC Power Flow Controller (SPDC-PFC). The SPDC-PFC input is the transmission line voltage and its output is transmission line current. Therefore, employing a full-power DC-DC converter is avoided as a merit. Additionally, in this study, the common two-layer MT-HVDC grid control framework comprised of primary and secondary layers is efficiently modified in order to integrate the SPDC-PFC. A differential direct voltage versus active power droop control scheme is applied to the SPDC-PFC at the local control layer, guaranteeing dynamic stability, while, an extended DC Power-Flow (DC PF) routine – integrating the SPDC-PFC – is developed at the secondary control layer, to ensure the static stability of the entire MT-HVDC grid. The proposed control framework enables the SPDC-PFC to regulate the flow of current/power in the envisioned HVDC transmission line. From the static and dynamic simulation results conducted on the test CIGRE B4 MT-HVDC grid, successful operation of the proposed SPDC-PFC and control solutions are demonstrated by considering power flow control action. In more details, the SPDC-PFC successfully regulates the compensated lines power to the desired reference both in static and dynamic simulations by introducing suitable compensation voltages. In addition, good dynamic performance under both SPDC-PFC power reference and wind power-infeed change is observed.

INDEX TERMS Control of power flow, Hierarchical control framework, Serial-parallel DC power flow controller (SPDC-PFC), MT-HVDC grids, Voltage source converter.

I. INTRODUCTION

The development of Multi-Terminal HVDC (MT-HVDC) systems has provided promising solutions to overcome challenges posed by AC networks. These solutions include facilitation of future European offshore super-grid and transmission of harvested offshore wind energy to onshore AC power systems [1-5] more especially in Europe where there is a possibility of connecting wind, hydro, and solar potentials located in the North Sea, Scandinavia, and Mediterranean sea [6].

Secure and reliable operation of the future MT-HVDC grids should be ensured by establishing suitable flexible control infrastructures which is the research motivation of this paper. Therefore, power industry companies will be driven to develop bespoke devices and related control strategies that increase grid efficiency, reliability, and security to successfully satisfy the requirements of the modern grids.

In order to control an MT-HVDC grid, a multi-layer (usually two) hierarchical control framework is commonly utilized [7-12]. In this context, the local control layer of an MT-HVDC grid (power converter level) is realized through the vector current control technique applied to the Voltage Source Converter (VSC)s which is typically accompanied with suitable direct voltage/active power sharing control philosophy with sample realizations [10, 13, 14]. It is while grid monitoring and (optimal) power-flow calculations are addressed at the global control layer (e.g., the grid control level) located at the dispatch center [15, 16].

The HVDC lines flowing power/current is dedicated by a "voltage difference" imposed to its both endings and the "line resistance". In this context, there is a chance that under certain operating conditions, some of the power lines might be overloaded while other lines remain under-utilized due to the limited flexibility of power flow control of the line [17]. In addition, the possible increased power losses in the future's complex MT-HVDC grids due to the loop power flows is another main concern that must be addressed. These potential issues and transmission bottlenecks could get alleviated by employing power flow control devices which bring the ability to redistribute the direct currents within the MT-HVDC grid [18, 19]. Accordingly, an economic solution can be achieved to relieve transmission congestion compared to the costly solution of constructing new HVDC lines. Aside from being technically justified, there are significant energy market benefits too: the transmitted power can be distributed between

two zones on particular lines, depending on the signals received that convey economic demand to perform a congestion management maneuver. This also provides the flexibility required to contribute towards a loss-reduction strategy in MT-HVDC grids [10].

For all these reasons, "control of power flow" in MT-HVDC grids has inspired research interest and attracted widespread attention from researchers [17, 20, 21]. Also, [22] has proposed a sensitivity analysis based approach to optimize the location and control variable setting of several types of PFCs within the MT-HVDC grid to enhance the grid static security. The importance of this topic has even motivated CIGRE to initiate a working group to investigate the feasibility and develop methods, and devices to address power flow control issues within MT-HVDC grids [23]. Nevertheless, there are similar efforts within the HVAC grids to improve the grid operating conditions, e.g. energy loss, voltage profile, and reliability, by appropriate coordination and control reference settings for controllable grid elements [24, 25].

Although several remarkable studies have been conducted over proposing of power electronic devices to enhance MT-HVDC grid control flexibility [17, 23, 26-29], they are mainly focused on "topology level" and have not deeply analyzed the impact of the converter on MT-HVDC grid studies. For instance, there are several papers [27, 30, 31] devoted to proposing and analyzing various cascaded PFCs along with their modeling and local control. Despite excellent regulation capability and DC fault blocking capability, their full-rated nature introduces considerable losses and reduced reliability. In this regard, there are emerging proposals [32-35] for interline PFCs which have partial-rated nature that should withstand a limited portion of system rated voltage as they are floated in each pole. However, their performance depends on the MT-HVDC grid loading and their flowing currents [22] which can be problematic under low flowing currents. Apart from the need for proposing a suitable high power/voltage DC-DC power converter topology, it is also essential to develop a suitable related primary-level control approach to address the power flow control objectives and to define a grid-level control strategy, at the higher layer, to bring the capability of performing power flow control in the MT-HVDC grid.

This paper firstly contributes to the field by proposing a DC-DC converter topology with special connection configuration and it's complete local control strategy to control MT-HVDC grid power flow regarding a specific HVDC line. The proposed topology improves dynamic stability during AC network side transients. Secondly, this study extends the secondary control layer of the MT-HVDC grid by integrating the action of the proposed power flow controller, which regulates the current/power flowing through the intended HVDC line.

The analysis approach followed by this study is summarized as follows:
• A converter topology is proposed with a special connection configuration to the transmission line named Serial Parallel DC Power Flow Controller (SPDC-PFC). The SPDC-PFC functionality as a DC power flow controller is evaluated in turn.
• An average model is proposed for the SPDC-PFC, suitable for the grid level static and dynamic studies.

• Primary (local-level) control system is designed for the SPDC-PFC, including a novel differential voltage-droop scheme to improve MT-HVDC grid control flexibility in terms of power flow control.
• The stability of the SPDC-PFC is studied by developing an appropriate linearized model.
• The MT-HVDC grid secondary control layer is extended by incorporating the local control structure of the SPDC-PFC, which constitutes the entire control structure.

The remainder of this paper is organized as follows. The proposed topology and control structure of the SPDC-PFC is discussed in Section II. Section III illustrates and describes how the incorporation of the SPDC-PFC in the DC power flow program and MT-HVDC grid overall control framework can be accomplished. Static analysis and dynamic simulation results are presented in Sections VI and V, respectively to demonstrate the successful operation of the SPC-PFC considering test CIGRE B4 MT-HVDC grid. Finally, the Conclusion section summarizes the achieved key findings.

II. FLEXIBLE CONTROL OF MT-HVDC GRIDS

To regulate power flow and power quality in the MT-HVDC grid, solid-state devices would be needed. This is comparable to FACTS devices in AC grids, as they enhance the grid functionality and controllability in turn. Considering the rapid progress in power electronics technology, it is feasible to utilize DC-DC high-power/current converters to control the power flow within MT-HVDC grids and hence, improve the grid functionality and controllability [20]. In this regard, one extra degree of freedom can be achieved by adjusting the power converter transformation ratio; which resemble the effect of the FACTS devices in AC power systems [36, 37]. This means that the converter flowing power can be regulated through fine adjusting the terminal voltage of the converter.

A. Serial -Parallel DC Power Flow Controller

The SPDC-PFC is installed through a parallel/series connection configuration (i.e., shunt input– series output) on the associated transmission line, Fig. 1. Therefore, this device imposes a compensating series voltage source to the corresponding line and hence, it has the potential of regulating its flowing current/power.
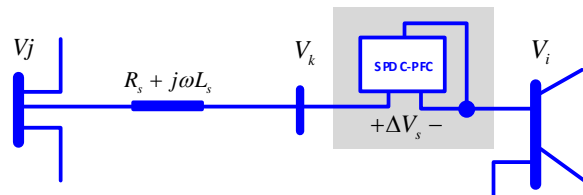
Fig. 1. The SPDC-PFC connection configuration (positive pole single-line).

The proposed SPDC-PFC topology is presented in Fig. 2. A dual active bridge power converter with magnetic isolation between the High-Voltage (HV) and the Medium-Voltage (MV) sides is the core of the SPDC-PFC. The SPDC-PFC is composed of a HVDC shunt-connected series-formed multi-modular converter to exchange current with the HVDC link, an isolation stage formed by transformers to couple the HV and the MV sides, and an MVDC series-connected parallel-formed multi-modular converter to insert voltage to the HVDC lines.

The SPDC-PFC of Fig. 2 has a single-phase topology for the sake of simplifying the presentation. However, this single-phase structure results in pulsating power flow through the magnetic isolation stage, which complicates regulation of the DC magnitudes. Such pulsating power would not exist in case of using a three-phase structure, which facilitates regulation of the DC magnitudes. In Fig. 2, the single-phase shunt-connected stage has a leg that has an MMC structure with n series-connected modules and an inductor. Here, the MMC modules employ a half-bridge structure, although other module topologies can be also used to improve controllability in case of faults. The isolation stage is composed of $2 \times m$ transformers with series-connected primary windings. The series-connected stage in Fig. 2 is composed of $2 \times m$ full-bridges, where m of

them share a common DC bus which is connected in series with the HVDC link's positive pole. It is while the other m ones do the same for the negative pole. The number of sub-modules and full-bridges can easily be rated according to the HVDC line voltage and its current level, respectively. The SPDC-PFC controls power flow by inserting a "controllable series voltage" to the compensated HVDC line. As shown in Figs. 1 and 2, the SPDC-PFC controls the power flow between the connecting buses i and j through regulating its "transformation ratio, n_H" defined as:

$$n_H = \left(\frac{\Delta V_s}{V_i} \right) \qquad (1)$$
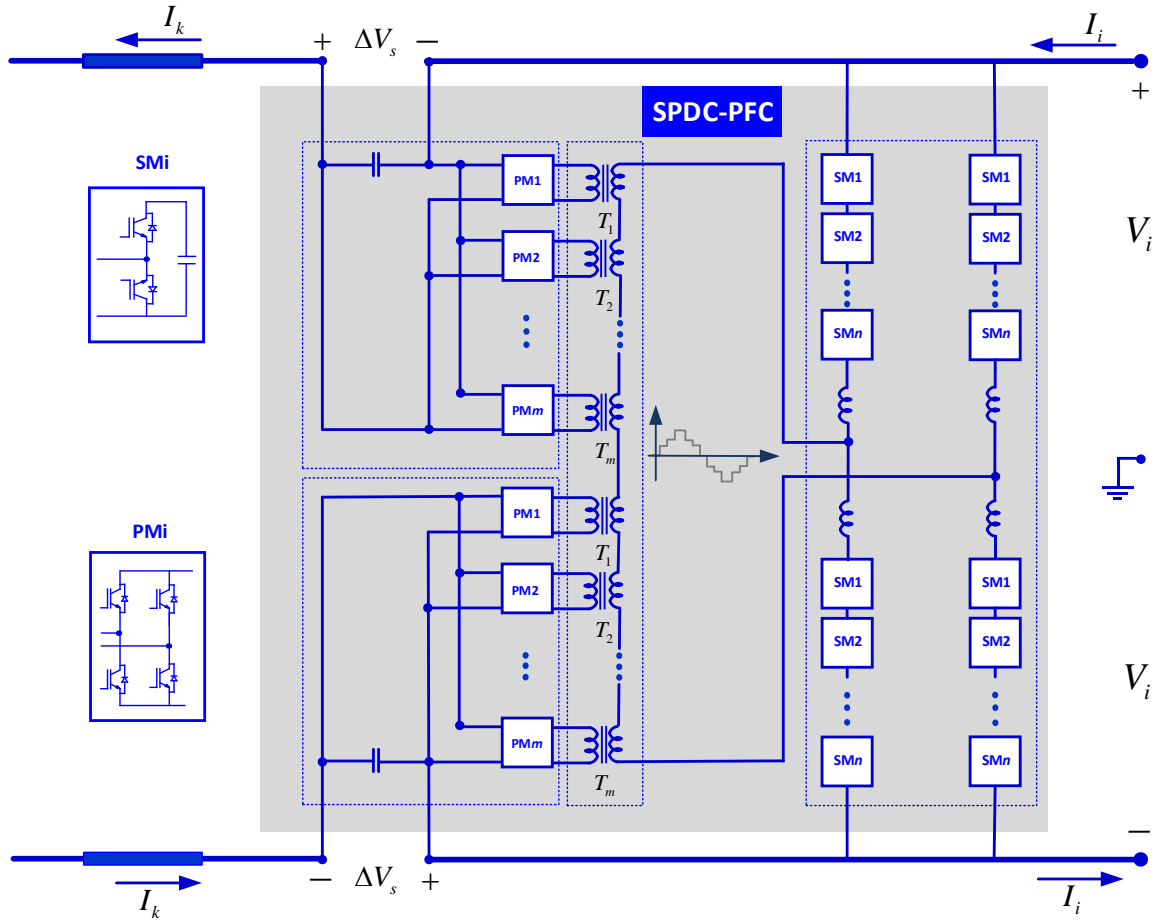
Fig. 2. Proposed topology for the SPDC-PFC.

where ΔV_s and V_i represent the steady-state voltages on the output and input of the SPDC-PFC, respectively. It can be easily concluded that the SPDC-PFC works at a fractional power level, since the intended HVDC line's full-rated current flow through it, but only a fractional series voltage in comparison with the corresponding HVDC bus voltage is outputted (see Figs. 1 and 2). However, a proper model is required to conduct dynamic and static investigations on the system level rather than a detailed switching model. This model is explained in the following sub-section.

B. Modeling of the SPDC-PFC

As mentioned before, appropriate modeling of the SPDC-PFC is vital for the static and dynamic analyses. In this study, a two-port average model for the SPDC-PFC is developed and illustrated in Fig. 3, consisting of a "controlled current source" and a "controlled voltage source", with losses omitted. The aim is to establish a two-port model for the SPDC-PFC which is a common modeling approach in power electronic studies [38].

For steady-state analysis, one can neglect the effects of storage elements and the following model is derived as the result:

$$\begin{bmatrix} V_k \\ I_i \end{bmatrix} = \begin{bmatrix} (1+n_H) & 0 \\ 0 & (1+n_H) \end{bmatrix} \begin{bmatrix} V_i \\ I_k \end{bmatrix} \quad (2)$$

However, the following frequency-domain model can be used for dynamic studies:

$$\begin{bmatrix} V_k(s) \\ I_i(s) \end{bmatrix} = \begin{bmatrix} (1+n_H) & 0 \\ sC & (1+n_H) \end{bmatrix} \begin{bmatrix} V_i(s) \\ I_k(s) \end{bmatrix} \quad (3)$$

C. Local Control of the SPDC-PFC

Fig. 3 shows a proposal for the local control system of the SPDC-PFC, whose main objective is to obtain the target flowing power in a particular HVDC line through using an appropriate PFC transformation ratio. For the SPDC-PFC, two control modes are considered; block mode, corresponding to n_H of zero, and therefore not providing power flow regulation, and the power flow control mode. Modes could get selected by dispatching control center located at the secondary control layer through communicating a signal, S_m, defined to be mode selection signal. In addition, the reference power $P_{PFC,ref}$ is provided by a differential direct voltage versus active power droop controller with droop slope of m_{PFC}.

Fig. 3. Proposed control structure for the SPDC-PFC.

The planned local control system in Fig. 3 consists of power and droop control loops. The differential voltage-droop control loop is used to improve system stability during grid contingencies and disturbances and provides the reference power for the SPDC-PFC. An inner power controller, which is realized by a PI structure, tracks the specified power reference by generating an appropriate reference compensation voltage. From the power flow routine output, a feed-forward transformation ratio, $n_{H,ff}$, is specified and dispatched by the grid-level control layer to improve the dynamic performance of the SPDC-PFC local control system.

To evaluate the SPDC-PFC stability, the related closed-loop linearized model is developed as shown in Fig. 4. Here, m_{PFC} specifies the slope of the direct voltage versus active power droop characteristic. A second-order Padé approximation is employed to model the switching delay of PWM generator block within the SPDC-PFC (see Fig. 4).

Considering high power application of the SPDC-PFC, the PI controller's parameters are adjusted to achieve a 200 ms settling time with 2% overshoot. From the open-loop system Bode diagram (Fig. 5), the robust and stable status of the system is found with a gain margin of 26 dB and phase margin of 77°.

III. INTEGRATION OF THE SPDC-PFC INTO THE MT-HVDC CONTROL FRAMEWORK

Proposed control framework for an MT-HVDC grid, composed of N DC terminals (or DC buses) is illustrated in Fig. 6. In this control framework, there are n VSC-HVDC stations in the grid and a SPDC-PFC.

At the local (or primary) control layer, the vector current control approach controls the VSC-DC stations in the rotary reference frame in which the current references, for voltage-controlling VSCs, are commonly specified by a direct voltage droop control philosophy [10]. It is while suitable reference control is dispatched to the local controllers by the secondary control layer acting as process supervisor. These signals are generated by a DC load-flow program, executed in the supervisory layer, in a periodic manner based on the current requirements of the MT-HVDC grid.

The program is initiated at discrete intervals, which are in sync with the pre-determined secondary control sample time. A proposal for this hierarchical control structure is shown in Fig. 6, which also considers the delay in sending and receiving signals between the secondary and primary layers.

In order to accurately capture the DC power-flow impacts on MT-HVDC grid power flow, the power-flow routine should be extended to incorporate SPDC-PFC at the grid-level control layer.
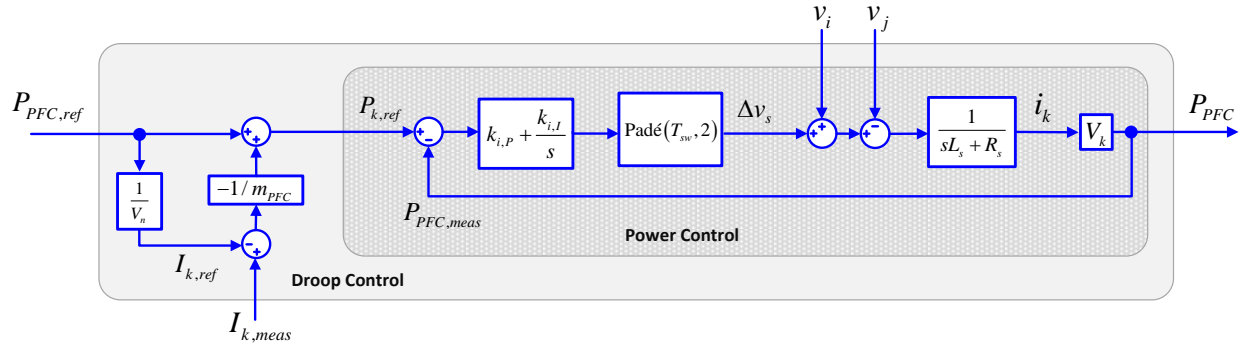
Fig. 4. The SPDC-PFC small-signal model comprised of differential droop and power control loops.
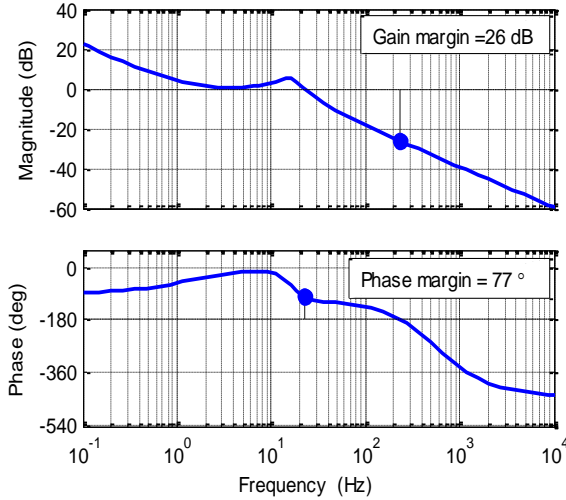

Fig. 5. HPFC open-loop Bode diagram.

To integrate the SPDC-PFC into the grid supervisory control system, some DC load-flow aspects should get altered through reformulating in presence of newly added SPDC-PFC.

A. MT-HVDC Power-Flow Formulation

The load-flow formulations for a sample N-terminal MT-HVDC grid are presented and the subsequent constraints are imposed [39]:

$$P_i = (P_{Gi} - P_{Li}) = V_i \cdot I_i \quad for \quad i = 1, \ldots, N \quad (4)$$

here, P_i, P_{Gi}, and P_{Li} are the net power injected, generated, and consumed, respectively. V_i is the bus voltage; and I_i denotes the bus i total injected direct current.

Afterward, the MT-HVDC grid conductance matrix $[G_{ij}]_{i,j=1,\ldots,N}$ is used to relate the buses total injected current to the bus voltages:

$$[I_1 \ I_2 \ldots I_N]^T = [G_{ij}] \cdot [V_1 \ V_2 \ldots V_N]^T \quad (5)$$

The conductance matrix elements could be readily specified as:

$$\begin{cases} \sum_{j=1}^{N} (g_{ij} + g_{si}) & for \quad i = j \\ -g_{ij} & for \quad i \neq j \end{cases} \quad (6)$$
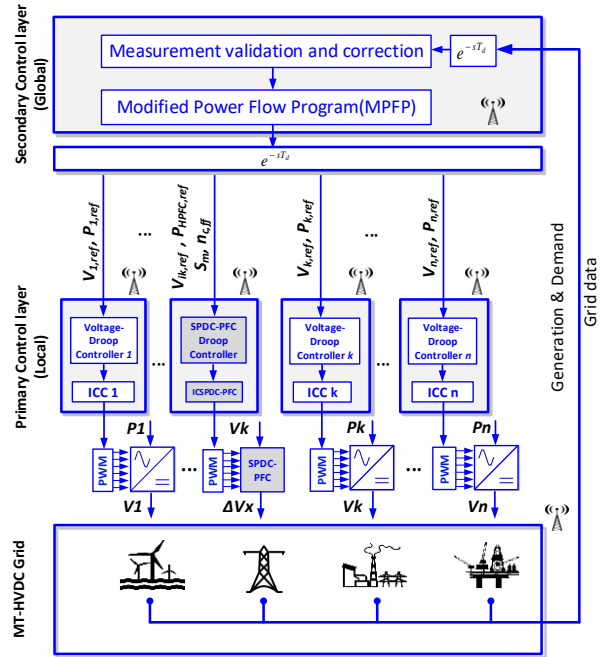

Fig. 6. Hierarchical two-layer (primary and secondary) control framework for MT-HVDC grid.

where the first line of (6) refers to the total conductance seen between DC buses i and j, and i to ground, respectively. The first line value is named driving-point conductance of bus i and for the second line is called transfer conductance between buses i and j.

The MT-HVDC grid buses power could be formulated as by the following:

$$P_i = V_i \cdot \left[\sum_{j=1}^{N} (G_{ij} \cdot V_j) \right] \quad for \quad i = 1, \ldots, N \quad (7)$$

As it is clear in (7), each HVDC bus adds two unknowns, P_i and V_i, hence there exist $2N$ total unknowns. Therefore, one variable per HVDC bus should get pre-determined in order to solve DC load-flow equations. Generally, two types of HVDC buses can be recognized in the MT-HVDC grids namely P-bus, with pre-selected total injected DC power and V-bus, with pre-selected direct voltage.

A 'slack bus' should be also integrated into the MT-HVDC grid load-flow routine to preserve the power balance. Considering the pre-selected slack bus's direct voltage, the

related equation is omitted from the DC load-flow routine and thereby power flow equations number is reduced.

The Newton–Raphson (NR) method is a successful approach to solve the AC power systems power-flow problem [40, 41]. Accordingly, the NR method is adapted to HVDC systems in this study which has a lower degree of complexity, number of equations, and constraints in comparison to HVAC counterparts. Hence, satisfactory performance is expected. The usual mathematical framework of the NR method can be easily found in the standard literature [42].

As the first HVDC bus is considered to be the slack bus (single V-bus) while keeping the generality, the state variables become:

$$\mathbf{V} = [V_2 \ldots V_N]^T \qquad (8)$$

and the following represents the vector of mismatch:

$$\mathbf{\Delta P} = [\Delta P_2 \; \Delta P_3 \ldots \Delta P_N]^T \qquad (9)$$

Note that the $\mathbf{\Delta P}$ elements can be calculated:

$$\Delta P_i = P_i^* - V_i \cdot \left[\sum_{j=1}^{N} G_j \cdot V_j \right] \quad for \quad i = 2, \ldots, N \qquad (10)$$

The DC power flow state variables can be updated by the following equations at iteration k and employing Jacobian matrix $\mathbf{J} = [J_{ij}]$:

$$[\mathbf{V}]^{k+1} = [\mathbf{V}]^k + [\mathbf{\Delta V}]^k \qquad (11)$$

$$[\mathbf{\Delta V}]^k = ([\mathbf{J}]^k)^{-1} \cdot [\mathbf{\Delta P}]^k \qquad (12)$$

The $\mathbf{J}$ matrix can get related to MT-HVDC grid load flow equations and computed in turn as:

$$J_{ij} = -\partial P_i / \partial V_j \quad i, j = 2, \ldots, N \qquad (13)$$

Finally, J_{ij} elements can be calculated:

$$J_{ij} = \begin{cases} -\sum_{\substack{j=1 \\ j \neq i}}^{N} (G_{ij} \cdot V_j) - 2G_{ii} \cdot V_i & for \quad i = j \\ -G_{ij} \cdot V_i & for \quad i \neq j \end{cases} \qquad (14)$$

B. Inclusion of the SPDC-PFC

The SPDC-PFC is intended to retain an electrical extent, y (here, the flowing power in the HVDC line connected between buses i and j, P_{ij}) at a pre-specified reference, y^*, through fine-adjusting the control variable u. Hence, DC load-flow equations should be extended to incorporate the SPDC-PFC. In this regard, the vectors of state and mismatch should be updated with adding of SPDC-PFC imposed equality constraints as follows:

$$\left[\begin{array}{c|c} \mathbf{J} & -\partial \mathbf{P} / \partial \mathbf{u} \\ \hline -\partial \mathbf{y} / \partial \mathbf{V} & -\partial \mathbf{y} / \partial \mathbf{u} \end{array} \right]^k \cdot \left[\begin{array}{c} \mathbf{\Delta V} \\ \mathbf{\Delta u} \end{array} \right]^k = \left[\begin{array}{c} \mathbf{\Delta P} \\ \mathbf{\Delta y} \end{array} \right]^k \qquad (15)$$

$$\Delta y = (y^* - y) \qquad (16)$$

where, $\mathbf{u}$ denotes the corresponding control variables vector and $\Delta \mathbf{y}$ refer to the new mismatch vector elements. The extra added row and column are related to the incorporation of SPDC-PFC which add the SPDC-PFC transformation ratio as a new unknown variable to the power flow equations.

For a lossless (ideal) SPDC-PFC, the following equations could be deduced:

$$P_{ik} = P_{ij} \qquad (17)$$

$$\Delta V_s = n_H \cdot V_i \qquad (18)$$

On inclusion of the SPDC-PFC, one extra degree of freedom will be obtained that enables the direct voltage adjustment on SPDC-PFC (both) terminals or related flowing power. Therefore, n_H will become the only control variable:

$$\Delta u = \Delta n_H \qquad (19)$$

If it is intended to control the power flow, i.e., P_{ij} to P_{ij}^*, Δy becomes:

$$\Delta y = \Delta P_{ij} = P_{ij} - P_{ij}^* \qquad (20)$$

and the following elements can be used to update the Jacobian matrix:

$$\frac{\partial P_{ij}}{\partial V_k} = \left(\frac{\partial P_{ij}}{\partial V_i} \cdot \frac{\partial V_i}{\partial V_k} \right) = \left(\frac{1}{1 + n_H} \right) \cdot \frac{\partial P_{ij}}{\partial V_i} \qquad (21)$$

$$\frac{\partial P_{ij}}{\partial n_H} = \left(\frac{\partial P_{ij}}{\partial V_i} \cdot \frac{\partial V_i}{\partial n_H} \right) = \frac{-V_k}{(1 + n_H)^2} \cdot \frac{\partial P_{ij}}{\partial V_i} \qquad (22)$$

$$P_{ij} = \left(\frac{V_k}{1 + n_H} \right) \left(V_j - \frac{V_k}{1 + n_H} \right) (-G_{ij}) \qquad (23)$$

Therefore, the augmented Jacobian matrix, (15), are expressed:

$$\left[\begin{array}{c|c} \mathbf{J} & -\partial \mathbf{P} / \partial n_H \\ \hline -\partial P_{ij} / \partial \mathbf{V} & -\partial P_{ij} / \partial n_H \end{array} \right]^k \left[\begin{array}{c} \mathbf{\Delta V} \\ \Delta n_H \end{array} \right]^k = \left[\begin{array}{c} \mathbf{\Delta P} \\ \Delta P_{ij} \end{array} \right]^k \qquad (24)$$

By employing this formulation, now, the SPDC-PFC is included into the MT-HVDC power-flow equations. Nevertheless, the $\partial P_{ij} / \partial V_i$, $\partial P_{ij} / \partial V_k$, and $\partial V_i / \partial n_H$ derivatives present in (21) and (22) can be easily calculated considering (18) and (23).

IV. STATIC SIMULATION RESULTS

A. Test MT-HVDC Grid

In this study, steady-state simulations are exercised considering the test eight-terminal CIGRE B4 MT-HVDC grid [43] to demonstrate how the SPDC-PFC can enhance the MT-HVDC grid control flexibility by power flow control. The schematic diagram of the test, bipolar (±400 kV), and symmetric CIGRE B4 DCS3 MT-HVDC grid is presented in Fig. 7. The offshore WFs nominal power is set to be 800 MW and 1600 MW for C2 and D1 respectively.
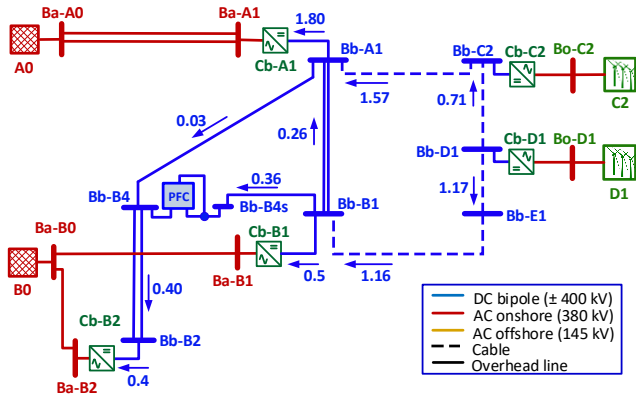
Fig. 7.   CIGRE DCS3 MT-HVDC grid including SPDC-PFC.

The onshore network side VSCs nominal powers are considered to be 2400 MW for Cb-A1, Cb-B1, and Cb-B2. Moreover, the HVDC transmission lines current capacity is taken to be 2265 A for HVDC cables and 3500 A for HVDC overhead lines (for more details refer to [43]). Base direct voltage and power are selected to be 800 kV and 500 MW while expressing per-unit results. Hence, the power production of some wind farms might exceed 1 pu. A MATLAB platform is utilized to perform static simulations by preparing valid m-files considering the relevant equations expressed in the per-unit system.

In the test grid, the SPDC-PFC is installed between buses Bb-B4s and Bb-B4 to regulate the flowing power of the HVDC line(s) between Bb-B1 and Bb-B4 buses as a PFC. The power-flow assumptions are presented in Table I for the slack bus (Bb-A1) and P-buses (Bb-B1, Bb-B2, Bb-C2, and Bb-D1) which have pre-specified direct voltage and generation/consumption values. Also, intermediary buses (Bb-B4, Bb-B4s, and Bb-E1) are considered as P-buses without generation/consumption. The objective is to show that the proposed SDC-PFC can regulate the flowing power of the intended HVDC line in steady-state by inserting suitable compensation voltage identified by the proposed modified power flow program. Accordingly, a base case power flow program is solved in section IV.B to obtain the MT-HVDC grid operating conditions before SDC-PFC placement. Accordingly, the proposed SDC-PFC is inserted to regulate the flowing power and the obtained results are compared with the base case in section IV.C.

TABLE I
POWER-FLOW DATA

DC bus	Bus type	DC voltage	Net power (pu)
Bb-A1	Slack	1	Unknown
Bb-B1	P	Unknown	-0.5
Bb-B2	P	Unknown	-0.4
Bb-B4	Intermediate	Unknown	0
Bb-B4s	Intermediate	Unknown	0
Bb-C2	P	Unknown	0.9
Bb-D1	P	Unknown	1.9
Bb-E1	Intermediate	Unknown	0

B.   Base Case

In the base case, n_H is kept at zero and the PFC does not make control action to control the flowing power. By applying the modified NR method to MT-HVDC grid load flow problem,

the following power-flow results are obtained, as presented in Table II with more details in Fig. 7. The obtained results include values of buses direct voltage and net injected power.

TABLE II
POWER-FLOW RESULTS (BASE CASE: FOR $N_H = 0$)

DC bus/DC Line	Bus type	DC voltage (pu)	Net power (pu)
Bb-A1	Slack	1.00000	-1.80299
Bb-B1	P	1.00102	-0.50000
Bb-B2	P	0.99864	-0.40000
Bb-B4	Intermediate	0.99971	0
Bb-B4s	Intermediate	0.99971	0
Bb-C2	P	1.00475	0.90000
Bb-D1	P	1.00792	1.90000
Bb-E1	Intermediate	1.00446	0
Bb-B1 to Bb-B4s[*]	-	-	0.36871

[*]Line powers are reported at the receiving end.

C. Effect of SPDC-PFC

In the first case, the SPDC-PFC is utilized to control the power transmitted through the transmission line connecting Bb-B1 and Bb-B4. The flowing power of this HVDC transmission line is scheduled at 0.5 pu (compared to the related base case value of 0.36871 pu) while preserving all power flow assumption (e.g., magnitudes of slack bus direct voltage and P-buses generation/consumption). Note that, without installation of the SPDC-PFC, the power flow on the mentioned HVDC line cannot be simultaneously controlled by the action controllable VSCs, under assumed operational modes, due to limited control flexibility.

Based on the static simulation (load-flow) results, the SDC-PFC transformation ratio n_H must be re-scheduled to $n_H = -0.00201$ to reach the reference power flow. The power-flow results are presented in Table III for this case. From Tables II and III it is clear that all the buses direct voltage has been changed due to the SPDC-PFC regulatory action.

While the controlled line's flowing power is regulated to 0.5 pu, the buses total injected power, except the slack bus, is equal to the relevant value of the base case. The change in slack bus power can be justified by the fact that the flowing power regulation in the compensated HVDC line will likely change MT-HVDC grid losses, which should be compromised by the slack bus to ensure power balance.

In Fig. 8, the detailed power-flow results and HVDC line power flows (for all DC lines) are presented. From the comparison of Fig. 8 and Fig. 9, the power flow change in all HVDC lines are clearly observed.

Fig. 8. Static simulation (load- flow) results for case 1 (ideal SPDC-PFC is assumed).

The cumulative amount of input and output powers at all

Fig. 9. Step change in the power of the line between Bb-B1 and Bb-B4.

buses deviate from zero in Fig. 8. This is due to calculating each power at the receiving side of each HVDC line; therefore, the sum of the power at the sending side of HVDC lines might not be zero as for transmission losses.

TABLE III
POWER-FLOW RESULTS (CASE 1: FOR N_H = -0.00201)

DC bus/DC Line	Bus type	DC voltage (pu)	Net power (pu)
Bb-A1	Slack	1.00000	-1.78273
Bb-B1	P	1.00065	-0.5000
Bb-B2	P	0.99981	-0.4000
Bb-B4	Intermediate	1.00088	0
Bb-B4s	Intermediate	0.99887	0
Bb-C2	P	1.00466	0.9000
Bb-D1	P	1.00771	1.9000
Bb-E1	Intermediate	1.00417	0
Bb-B1 to Bb-B4s[*]	-	-	0.5

[*]Line powers are reported at the receiving end.

V. DYNAMIC PERFORMANCE EVALUATION

The conducted static analyses demonstrate the SPDC-PFC ability of power flow control in the MT-HVDC grid. Dynamic evaluations would be also necessary to validate the SPDC-PFC regulatory action and its performance. In this study, the averaged models of the VSC-HVDC stations and SPDC-PFC are used and implemented in a MATLAB/Simulink platform. In this study, the grid-side VSC-HVDC stations are operating in voltage droop mode for distributed direct voltage control and sharing of active power. The wind farm-side VSC-HVDC stations control the AC voltage amplitude, frequency, and phase angle of their corresponding AC systems by operating in the grid forming mode. All VSC's controllers are designed using well-known classical approaches.

The objective is to evaluate dynamic performance of the proposed SDC-PFC under both power reference and wind power-infeed change scenarios. The action of proposed local control structure for the SDC-PFC and periodic update of control references by the proposed secondary control layer are highlighted.

A. Dynamic Evaluation of the SPDC-PFC

The dynamic evaluation is initialized with the power-flow results, refer to the base steady-state in Table II. Accordingly, the references of the direct voltage versus active power droop controllers of the grid-side VSC-HVDC stations are adjusted from the results of the DC load-flow.

The flowing power in the controlled HVDC line is kept at 0.5 pu before $t = 5$ sec by SPDC-PFC with $n_H = 0.00201$. Fig. 9 and Fig.10 present the power flow profiles of the line and the grid-side VSC-HVDC stations respectively. At $t = 5$ sec, the secondary control runs power-flow again to re-schedule the power transmitted by the controlled line to 0.4 pu. Considering the DC power flow results, calculated at the secondary control layer, the SPDC-PFC transformation ratio must be re-adjusted to $n_H = 0.00058$. Nevertheless, the direct voltage- active power droop settings are also updated regarding onshore VSCs. From Fig. 9, it is visible that the flowing power in the compensated HVDC line has tracked the new set-point of 0.4 pu within the specified settling time and demonstrating a good dynamic performance.

Considering the power profile of the onshore VSC-HVDC stations (Fig. 10), it is evident that the direct voltage versus active power droop controller of the VSC-HVDC stations has a satisfactory performance in keeping the VSC-HVDC stations power at their pre-specified value, thereby indicating the favorable performance of the presented control strategy for both the primary and secondary control layers.

B. Response to Grid Disturbances

The following scenario is considered to evaluate the robustness of the introduced control strategy under grid disturbances. The flowing power of the compensated HVDC transmission line is scheduled at 0.5 pu initially.

Then, a -0.9 pu decrease is applied to the generation of the offshore grid Bo-D1 (at $t = 3$ secs). Accordingly, MT-HVDC grid status fluctuation is inevitable, however, it should not lead to grid instability. The power profile of the compensated HVDC line is presented in Fig. 11 in the period of this contingency. From Fig. 11, it can be seen that the power is flowing by the SPDC-PFC and hence compensated HVDC line is reduced during the disturbance. This implies a high reduction in the total generated power, as for the action of the employed direct voltage versus active power droop controller.

At $t = 5$ secs, the secondary control layer, dispatching center, computes and sends new control references for the direct voltage versus active power droop controller of the onshore VSC-HVDC stations, and the SPDC-PFC. In this regard, the DC load-flow routine is executed again considering the current MT-HVDC grid status in terms of generated powers, demand requirements, etc. Thanks to new control references sent by the dispatching center, the flowing power of the compensated

HVDC line is recovered to 0.5 pu which is evident from Fig.

11. Moreover, tracking of prescribed power references for Cb-B1 (0.5 pu) and Cb-B2 (0.4 pu) onshore VSC-HVDC stations,
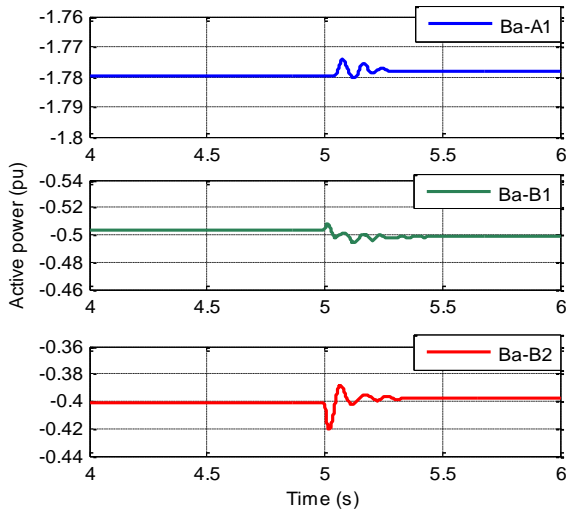

Fig. 10.   Power profile of the grid-side VSC-HVDC stations during a step change for SPDC-PFC.
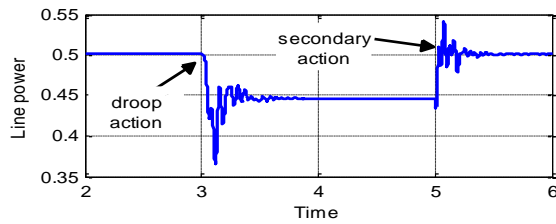

Fig. 11.   Controlled power flow of the line between Bb-B1 and Bb-E1 VCSs during grid disturbance.
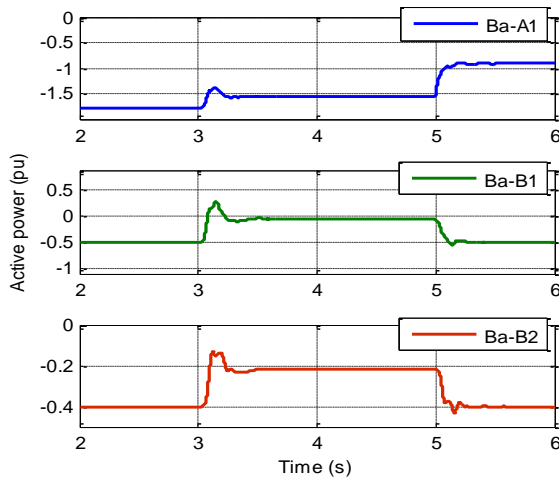

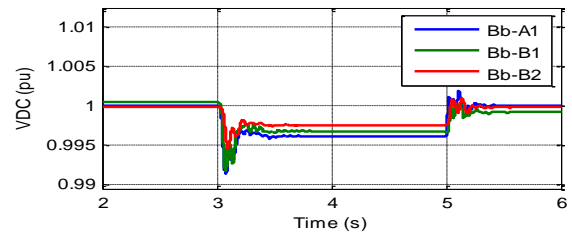Fig. 12. Power profiles of VSC-HVDC stations during grid disturbance.

Fig. 13. Direct voltage profiles of grid-side VCS stations.

as *P*-buses, is successfully attained (see Fig. 12). Finally, Fig. 13 depicts the direct voltage profiles of the onshore VSC-HVDC stations during simulations.

VI. CONCLUSION

A Serial-Parallel DC Power Flow Controller (SPDC-PFC) is demonstrated in this research and its complete control strategy is integrated with the grid control framework. The aim was to control the intended HVDC line flowing current/power and hence enhance MT-HVDC grid control flexibility. To do so, a two-layer hierarchical control framework taking into account of VSC-HVDC stations and the SPDC-PFC station was proposed and investigated. In more details, a direct voltage versus active power droop control approach was implemented at the local control layer of power converters, while the modified DC power-flow routine is employed at the global control to integrate the SPDC-PFC for power flow purpose.

Static and dynamic simulations conducted on test CIGRE DCS3 MT-HVDC grid exhibited its capability in power flow control and thereby enhancing MT-HVDC grid control flexibility and HVDC line utilization. In more details, it is found that the proposed SPDC-PFC can regulate the compensated HVDC lines flowing power to the desired reference by injection of suitable compensation voltages, which also proves successful functionality of the proposed secondary control layer. Further, the successful dynamic performance of the proposed SPDC-PFC accompanied with the related primary control level controllers are validated by applying both SPDC-PFC power reference and wind power-infeed change. The simulation results indicate successful dynamic power reference tracking and stable operation under wind power-infeed changes. Future PFC installation objectives might aim to increase grid efficiency and manage grid congestion.

REFERENCES

[1]   S. Taraft, D. Rekioua, D. Aouzellag, and S. Bacha, "A proposed strategy for power optimization of a wind energy conversion system connected to the grid," *Energy Conversion and Management,* vol. 101, pp. 489-502, 2015.

[2]   C. Dierckxsens, K. Srivastava, M. Reza, S. Cole, J. Beerten, and R. Belmans, "A distributed DC voltage control method for VSC MTDC systems," *Electric Power Systems Research,* vol. 82, pp. 54-58, 2012.

[3]   D. Van Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles,"

Renewable and Sustainable Energy Reviews, vol. 14, pp. 3156-3163, 2010.

[4] L. Xu, B. W. Williams, and L. Yao, "Multi-terminal DC transmission systems for connecting large offshore wind farms," in *2008 IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, 2008, pp. 1-7.

[5] Y. Liu, A. Raza, K. Rouzbehi, B. Li, D. Xu, and B. W. Williams, "Dynamic Resonance Analysis and Oscillation Damping of Multiterminal DC Grids," *IEEE Access,* vol. 5, pp. 16974-16984, 2017.

[6] J. Blau, "Europe plans a North Sea grid," *IEEE Spectrum,* vol. 47, pp. 12-13, Mar. 2010.

[7] N. R. Chaudhuri and B. Chaudhuri, "Adaptive Droop Control for Effective Power Sharing in Multi-Terminal DC (MTDC) Grids," *IEEE Transactions on Power Systems,* vol. 28, pp. 21-29, 2013.

[8] A. S. Abdel-Khalik, A. M. Massoud, A. A. Elserougi, and S. Ahmed, "Optimum Power Transmission-Based Droop Control Design for Multi-Terminal HVDC of Offshore Wind Farms," *IEEE Transactions on Power Systems,* vol. 28, pp. 3401-3409, 2013.

[9] K. Rouzbehi, J. I. Candela, A. Luna, G. B. Gharehpetian, and P. Rodriguez, "Flexible Control of Power Flow in Multiterminal DC Grids Using DC-DC Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 4, pp. 1135-1144, 2016.

[10] K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna, and P. Rodriguez, "A Generalized Voltage Droop Strategy for Control of Multiterminal DC Grids," *IEEE Transactions on Industry Applications,* vol. 51, pp. 607-618, 2015.

[11] K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna, and P. Rodriguez, "A hierarchical control structure for multi-terminal VSC-based HVDC grids with GVD characteristics," in *2013 International Conference on Renewable Energy Research and Applications (ICRERA)*, 2013, pp. 996-1001.

[12] A. Raza, Y. Liu, K. Rouzbehi, M. Jamil, S. O. Gilani, X. Dianguo*, et al.*, "Power Dispatch and Voltage Control in Multiterminal HVDC Systems: A Flexible Approach," *IEEE Access,* vol. 5, pp. 24608-24616, 2017.

[13] K. Rouzbehi, A. Miranian, A. Luna, and P. Rodriguez, "A generalized voltage droop strategy for control of multi-terminal DC grids," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 59-64.

[14] E. Prieto-Araujo, F. D. Bianchi, A. Junyent-Ferre, and O. Gomis-Bellmunt, "Methodology for Droop Control Dynamic Analysis of Multiterminal VSC-HVDC Grids for Offshore Wind Farms," *IEEE Transactions on Power Delivery,* vol. 26, pp. 2476-2485, 2011.

[15] K. Rouzbehi, A. Miranian, A. Luna, and P. Rodriguez, "DC Voltage Control and Power Sharing in Multiterminal DC Grids Based on Optimal DC Power Flow and Voltage-Droop Strategy," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 2, pp. 1171-1180, 2014.

[16] S. S. H. Yazdi, K. Rouzbehi, J. I. Candela, J. Milimonfared, and P. Rodriguez, "Analysis on impacts of the shunt conductances in multi-terminal HVDC grids optimal power-flow," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 121-125.

[17] D. Jovcic, M. Hajian, H. Zhang, and G. Asplund, "Power flow control in DC transmission grids using mechanical and semiconductor based DC/DC devices," in *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, 2012, pp. 1-6.

[18] K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna, and P. Rodriguez, "Proposals for flexible operation of multi-terminal DC grids: Introducing flexible DC transmission system (FDCTS)," in *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, 2014, pp. 180-184.

[19] S. S. H. Yazdi, K. Rouzbehi, J. I. Candela, J. Milimonfared, and P. Rodriguez, "Flexible HVDC transmission systems small signal modelling: A case study on CIGRE Test MT-HVDC grid," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 256-262.

[20] A. Parastar, Y. C. Kang, and J. K. Seok, "Multilevel Modular DC/DC Power Converter for High-Voltage DC-Connected Offshore Wind Energy Applications," *IEEE Transactions on Industrial Electronics,* vol. 62, pp. 2879-2890, 2015.

[21] E. Veilleux and B. T. Ooi, "Multiterminal HVDC With Thyristor Power-Flow Controller," *IEEE Transactions on Power Delivery,* vol. 27, pp. 1205-1212, 2012.

[22] S. S. Heidary Yazdi, J. Milimonfared, S. H. Fathi, and K. Rouzbehi, "Optimal placement and control variable setting of power flow controllers in multi-terminal HVDC grids for enhancing static security," *International Journal of Electrical Power & Energy Systems,* vol. 102, pp. 272-286, 2018.

[23] CIGRE WG B4-58: Devices for load flow control and methodologies for direct voltage control in a meshed HVDC grid [Online]. Available: http://b4.cigre.org/

[24] M. Aryanezhad, "Management and coordination of LTC, SVR, shunt capacitor and energy storage with high PV penetration in power distribution system for voltage regulation and power loss minimization," *International Journal of Electrical Power & Energy Systems,* vol. 100, pp. 178-192, 2018/09/01/ 2018.

[25] M. Aryanezhad, E. Ostadaghaee, and M. Joorabian, "Management and coordination charging of smart park and V2G strategy based on Monte Carlo algorithm," in *2014 Smart Grid Conference (SGC)*, 2014, pp. 1-8.

[26] Q. Mu, J. Liang, Y. Li, and X. Zhou, "Power flow control devices in DC grids," in *2012 IEEE Power and Energy Society General Meeting*, 2012, pp. 1-7.

[27] D. Jovcic, "Bidirectional, High-Power DC Transformer," *IEEE Transactions on Power Delivery,* vol. 24, pp. 2276-2283, 2009.

[28] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday, and B. W. Williams, "Review of dc-dc converters for multi-terminal HVDC transmission networks," *IET Power Electronics,* vol. 9, pp. 281-296, 2016.

[29] B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "Modular Multilevel High-Frequency-Link DC Transformer Based on Dual Active Phase-Shift Principle for Medium-Voltage DC Power Distribution Application," *IEEE Transactions on Power Electronics,* vol. 32, pp. 1779-1791, 2017.

[30] D. Jovcic and B. T. Ooi, "Developing DC Transmission Networks Using DC Transformers," *IEEE Transactions on Power Delivery,* vol. 25, pp. 2535-2543, 2010.

[31] T. Lüth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-Frequency Operation of a DC/AC/DC System for HVDC Applications," *IEEE Transactions on Power Electronics,* vol. 29, pp. 4107-4115, 2014.

[32] J. Sau-Bassols, E. Prieto-Araujo, and O. Gomis-Bellmunt, "Modelling and Control of an Interline Current Flow Controller for Meshed HVDC Grids," *IEEE Transactions on Power Delivery,* vol. 32, pp. 11-22, 2017.

[33] N. Deng, P. Wang, X. P. Zhang, G. Tang, and J. Cao, "A DC current flow controller for meshed modular multilevel converter multiterminal HVDC grids," *CSEE Journal of Power and Energy Systems,* vol. 1, pp. 43-51, 2015.

[34] W. Chen, X. Zhu, L. Yao, G. Ning, Y. Li, Z. Wang, *et al.*, "A Novel Interline DC Power-Flow Controller (IDCPFC) for Meshed HVDC Grids," *IEEE Transactions on Power Delivery,* vol. 31, pp. 1719-1727, 2016.

[35] J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt, and F. Hassan, "Series interline DC/DC Current Flow Controller for meshed HVDC grids," *IEEE Transactions on Power Delivery,* vol. PP, pp. 1-1, 2017.

[36] K. Rouzbehi, J. I. Candela, G. B. Gharehpetian, L. Harnefors, A. Luna, and P. Rodriguez, "Multiterminal DC grids: Operating analogies to AC power systems," *Renewable and Sustainable Energy Reviews,* vol. 70, pp. 886-895, 2017.

[37] B. Chong, X. P. Zhang, L. Yao, K. R. Godfrey, and M. Bazargan, "Congestion Management of Electricity Markets Using FACTS Controllers," in *2007 IEEE Power Engineering Society General Meeting*, 2007, pp. 1-6.

[38] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2 ed.: Springer US, 2001.

[39] K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna, and P. Rodriguez, "A hybrid power flow controller for flexible operation of multi-terminal DC grids," in *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, 2014, pp. 550-555.

[40] A. Gomez-Exposito, A. J. Conejo, and C. Canizares, *Electric Energy Systems: Analysis and Operation*: CRC Press 2008.

[41] N. M. Peterson and W. S. Meyer, "Automatic Adjustment of Transformer and Phase-Shifter Taps in the Newton Power Flow," *IEEE Transactions on Power Apparatus and Systems,* vol. PAS-90, pp. 103-108, 1971.

[42] J. D. Glover, M. S. Sarma, and T. Overbye, *Power System Analysis and Design*, 5 ed.: Cengage Learning, 2011.

[43] T. K. Vrana, Y. Yang, D. Jovcic, S. Dennetière, J. Jardini, and H. Saad, "The CIGRE B4 DC Grid Test System," 2016.