Sequential Phase-Shifted Model Predictive Control for Multicell Power Converters

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Abstract—This paper proposes a sequential Phase-Shifted Model Predictive Control (PS-MPC) strategy for multicell power converters. The key novelty of this proposal lies in the way the predictive control strategy is formulated to fully exploit a phase-shifted pulse width modulation (PS-PWM) stage. Normally, when using a linear controller along with a standard PS-PWM stage, the modulator receives the same duty cycle for all the internal carriers. In contrast, by means of an appropriate choice of synchronized models for each carrier, the proposed predictive controller obtains independent optimal duty cycles for each carrier in a sequential manner. This allows one to formulate the optimal control problem to govern not only the output current but also the internal floating capacitor voltages, similarly to the finite-control-set MPC (FCS-MPC) case. As a result, the proposed sequential PS-MPC can attain a faster floating voltage balancing dynamic when compared to a standard PS-PWM implementation. Moreover, it generates a fixed-spectrum in the steady state with a constant commutation rate, which outperforms a standard FCS-MPC strategy. Simulation results of the proposed sequential PS-MPC strategy governing a single-phase four-level flying capacitor converter are presented to verify its dynamic and steady-state performance.

Index Terms—Predictive control, predictive models, control design, sequential analysis, flying capacitor, multilevel converters, pulsewidth modulation (PWM), phase-shifted, power conversion.

I. INTRODUCTION

Multilevel converters (MCs) are an interesting technology for medium/high-voltage and high power applications, such as high-power ac motor drives, active power filters, and integration of renewable energy sources to the grid [1], [2].

Several multilevel topologies have been proposed in the literature, which offer different features [1], [3]. Among them the most important, and in continuous development, are the Neutral Point Clamped (NPC), Flying Capacitor, Cascaded H-bridge (CHB), and Modular Multilevel Converter (MMC) [1]. This work is particularly focused on the flying capacitor converter, which is an interesting multilevel topology from the power electronics and control point of view. This topology requires a single dc-link to feed a three-phase load (unlike CHB), is not difficult to scale to a higher number of levels (unlike NPC), and the flying capacitor voltages can reach a stable operation under not too demanding conditions. On the other side, from a control perspective, when an active control of the capacitor voltage balance is required, the converter model results in a non-linear system due to the interaction of the states (capacitor voltages) and inputs (semiconductor gate

signals). In general, a standard approach in power electronics to address this issue is to decouple this problem by means of a pulsewidth modulation (PWM) technique [4]. For example, in [5]–[7], it has been shown that in steady-state operation and using phase-shifted PWM (PS-PWM), the floating capacitors tend to stabilize their voltages to a, so-called, balanced value without requiring an active control. This, is referred to as natural balancing. Therefore, in a flying capacitor converter, the PS-PWM stage takes care of the internal capacitor voltages while an external controller governs the output current [8]. However, this natural balance mechanism presents a poor capacitor voltage dynamic (slow with large oscillations), which only depends on the system parameters. In [9], it was shown how the natural balancing process can be significantly accelerated by actively controlling the capacitor voltages using finite-control-set model predictive control (FCS-MPC). Moreover, in [10], FCS-MPC has been used to impose a capacitor voltage ratio different to the balanced case in order to increase the number of levels in the output voltage, improving the output current Total Harmonic Distortion (THD). As in other MPC algorithms (see, e.g., [11]–[15]), in [9], the actuation signal is chosen to minimize a cost function, which quantifies a tracking error. A key aspect of FCS-MPC, as used in [9], [10], is that it explicitly takes into account the fact that power converters can only generate a finite number of actuations. Thus, the optimal switching combination, i.e., the one which minimizes the cost function, can be found by searching over a finite set. An advantage of FCS-MPC methods is that the cost function can merge in a single-expression electrical and nonelectrical variables, e.g., tracking of currents; the balancing of capacitor voltages and the total number of commutation events [16], [17]. However, a clear disadvantage when compared to PWM-based control strategies is a variable switching frequency, an uneven distribution of semiconductor losses, and a spread spectrum in the electrical variables are obtained.

To address the above issues, this work proposes a sequential Phase-Shifted MPC (PS-MPC) for multicell power converters. This predictive control strategy takes advantage of the PS-PWM working principle to optimally obtain independent duty cycles for each carrier in a sequential manner. As a result, the proposed sequential PS-MPC can attain a faster floating voltage balancing dynamic when compared to a standard PS-PWM implementation while achieving a fixed-spectrum in the

steady state with a constant switching rate which therefore outperforms a standard FCS-MPC strategy.

II. FLYING CAPACITOR CONVERTER

In this section, we describe the flying capacitor converter topology in more detail and develop a model for the system. Figure 1 shows a schematic of a single-phase four-level flying capacitor converter. This converter is electrically fed by a dc-voltage source V_{dc}. Internally, this converter has three-pairs of power switches that work in a complementary manner to avoid open- and short-circuits. Therefore, the state of each pair of switches can be represented only by the state of one of them, i.e.:

$$S_j(t) = \begin{cases} 0 & \text{if } S_j = 0 \text{ and } \bar{S}_j = 1 \\ 1 & \text{if } S_j = 1 \text{ and } \bar{S}_j = 0 \end{cases} \quad (1)$$

for all $j \in \{1, 2, 3\}$.

A distinguishing feature of this converter is that it has two internal capacitors that are electrically floating. They are required to generate intermediate voltage levels in the total output voltage. Thus, a staircase waveform of four-levels can be achieved when floating capacitor voltages are balanced, i.e., $V_{dc} : v_{C2} : v_{C1} = 1 : 2/3 : 1/3$. It is important to note that the load is connected between the output terminal a and the middle point of the dc-link n in order to generate a returning path for the alternating output current.

A. Continuous-Time Model

To derive a continuous-time model of the flying capacitor converter, we firstly denote:

$$u(t) = \begin{bmatrix} u_1(t) \\ u_2(t) \\ u_3(t) \end{bmatrix} = \begin{bmatrix} S_1(t) \\ S_2(t) \\ S_3(t) \end{bmatrix}, \quad (2)$$

as the system input. Then, considering the electrical topology in Fig. 1, by using simple circuit analysis, the following continuous-time dynamic model for each capacitor voltage and output current can be obtained:

$$\frac{dv_{C1}(t)}{dt} = -\frac{1}{C_1} i_L(t)(u_1(t) - u_2(t)) \quad (3)$$

$$\frac{dv_{C2}(t)}{dt} = -\frac{1}{C_2} i_L(t)(u_2(t) - u_3(t)) \quad (4)$$

$$\frac{di_L(t)}{dt} = -\frac{R}{L} i_L(t) + \frac{1}{L} v_{an}(t), \quad (5)$$

where $v_{an}(t)$ is the converter output voltage, which is given by:

$$v_{an}(t) = (u_1(t) - u_2(t))v_{C1}(t) + (u_2(t) - u_3(t))v_{C2}(t) + (u_3(t) - 1/2)V_{dc}. \quad (6)$$

B. Discrete-Time Model

The continuous-time model in (3)–(5) can be transformed into discrete-time by using a zero order hold approximation, by considering that the output voltage, $v_{an}(t)$, remains constant
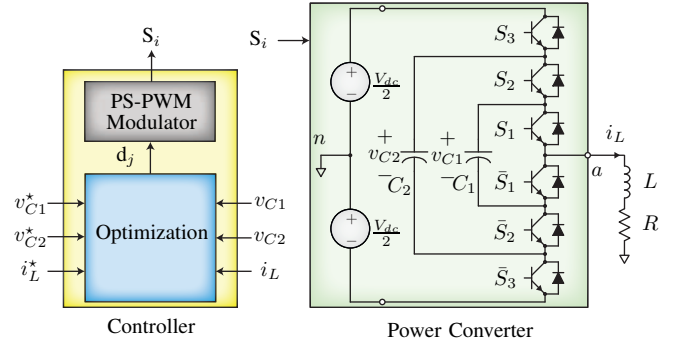

Fig. 1. Single-phase four-level flying capacitor topology and proposed sequential PS-MPC strategy.

during the sampling period T_s. This results in the following discrete-time dynamic model of the flying capacitor converter:

$$v_{C1}(k+1) = v_{C1}(k) - \gamma_{c1} i_L(k)(u_1(k) - u_2(k))$$
$$v_{C2}(k+1) = v_{C2}(k) - \gamma_{c2} i_L(k)(u_2(k) - u_3(k)) \quad (7)$$
$$i_L(k+1) = \gamma_a i_L(k) + \gamma_b v_{an}(k)$$

where

$$\gamma_a = e^{-T_s R/L},$$
$$\gamma_b = (1 - \gamma_a)/R, \quad (8)$$
$$\gamma_{cj} = T_s/C_j.$$

Finally, considering

$$x(k) = \begin{bmatrix} v_{C1}(k) \\ v_{C2}(k) \\ i_L(k) \end{bmatrix} \quad (9)$$

as the system state, a discrete-time state-space model of the flying capacitor converter can be represented via:

$$x(k+1) = Ax(k) + B(x(k))u(k) + g \quad (10)$$

where

$$A = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & \gamma_a \end{bmatrix}, \quad g = \begin{bmatrix} 0 \\ 0 \\ -\gamma_b V_{dc}/2 \end{bmatrix},$$

$$B(x) = \begin{bmatrix} -\gamma_{c1} i_L & \gamma_{c1} i_L & 0 \\ 0 & -\gamma_{c2} i_L & \gamma_{c2} i_L \\ \underbrace{\gamma_b v_{C1}}_{b_1(x)} & \underbrace{\gamma_b(v_{C2} - v_{C1})}_{b_2(x)} & \underbrace{\gamma_b(V_{dc} - v_{C2})}_{b_3(x)} \end{bmatrix}. \quad (11)$$

Notice from matrix $B(x)$ in the state-space model (10)–(11) that the flying capacitor converter is a non-linear system, since the system state, $x(k)$, multiplies the control input, $u(k)$. Therefore, from a control viewpoint, this is a challenging topology.

C. Control Target

For the flying capacitor converter, it is desired to control not only the output current, $i_L(t)$, but also the internal floating capacitor voltages.

In general, a flying capacitor converter can be subdivided in *cells*. Each cell is composed by a dc-voltage source (or floating capacitor) and a pair of complementary power switches. For a η-cell flying capacitor converter, the voltage that each switch, S_j, has to block is given by the difference between the two adjacent capacitor voltages. To ensure that this voltage is the same for every switch, each capacitor C_j must be charged with a voltage of

$$v_{Cj}^\star = \frac{j}{\eta} V_{dc}, \quad \forall j \in \{1, \cdots, \eta\}. \tag{12}$$

As a result of this, a blocking voltage of V_{dc}/η will be obtained for every power switch. Moreover, as mentioned before, if these balanced voltages are achieved, a four-level output voltage waveform will be obtained for a 3-cell converter, as the one shown in Fig. 1. Therefore, the control target for this converter can be represented by:

$$x^\star(k) = \begin{bmatrix} V_{dc}/3 \\ 2V_{dc}/3 \\ i_L^\star(k) \end{bmatrix} \tag{13}$$

where the output current reference is given by:

$$i_L^\star(t) = I^\star \sin(\omega t). \tag{14}$$

III. STANDARD FCS-MPC

In order to achieve the desired balanced voltage condition, a multi-variable closed-loop controller for a flying capacitor converter should not only govern the output current but also the internal floating voltages, as per (13).

To obtain predictions of the system state, the non-linear system (10) can be directly evaluated for the 8 different combinations of $u(k)$, namely,

$$\mathbb{U} \triangleq \left\{ \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}, \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}, \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix}, \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix}, \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix}, \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \right\}. \tag{15}$$

Then, each system state prediction is evaluated in the following quadratic cost function:

$$J(k) = e(k+1)^T Q e(k+1) \tag{16}$$

where

$$e(k+1) = x(k+1) - x^\star(k+1) \tag{17}$$

is the next-step system state tracking error and

$$Q = \text{diag}(\lambda_1, \lambda_2, 1) \tag{18}$$

is the system state weighing matrix. Here, λ_1 and λ_2 are weighting factors which allow one to trade current tracking error versus capacitor voltage tracking errors and, thus, achieve the proposed control target.

Finally, the optimal switch combination is the one that minimizes the cost function in (16), i.e.,

$$S^{\text{opt}}(k) = \arg \left\{ \min_{S(k) \in \mathbb{U}} J(k) \right\}. \tag{19}$$

For further details on stability of FCS-MPC for power converters, the reader is referred to [18], [19].

IV. PROPOSED SEQUENTIAL PS-MPC

In general, when controlling power converters, a modulation stage is normally used to synthesize the required output voltage. Particularly for flying capacitor converters, it is also required that this modulation technique can balance the floating capacitor voltages. In this context, one of the most popular modulation techniques for flying capacitor converters is PS-PWM. This modulation technique provides a natural balancing of the floating capacitor voltages with an easy implementation. However, since it is not an active control method, the resulting dynamic is in general slow and with large oscillations, which depends only on the system parameters.

To formulate the proposed sequential PS-MPC strategy, we take advantage of the PS-PWM working principle; cf. [20]. In Fig. 2, a three-carrier PS-PWM working in a double update mode is depicted. Here, one can see that each duty cycle, d_j, is only updated whenever the value of its associated carrier T_j is at one of its edges. After that, d_j remains constant until the next update (i.e., during half of the carrier period, $T_c/2$). This results in a sequential duty cycle update process (as shown in Fig. 2), with the advantage that only one of them needs to be obtained at each sampling instant. This behavior is the key to derive an average model that will be used to sequentially forecast the future system behavior every $T_c/(2\eta)$-time intervals, but considering predictions for each half of the carrier period, i.e., $T_s = T_c/2$ in (8).

A. Sequential Average Model

Based on the above analysis, a sequential average model of the flying capacitor converter can be derived. Firstly, we notice that each power switch, $S_j(k)$, commutes only once during its updating period, $T_c/2$. Thus, we now substitute them by their average values (or duty cycles), $d_j(k)$ in (10), i.e.,

$$u(k) = \boldsymbol{d}(k) = \begin{bmatrix} d_1(k) \\ d_2(k) \\ d_3(k) \end{bmatrix}. \tag{20}$$

Then, since only one active duty cycle, $d_j(k)$, needs to be calculated, the inactive ones are considered to be constant. Thus, the inactive duty cycles are represented by $\bar{d}_\ell(k)$ with $\ell \neq j$. Consequently, the resulting sequential average model of the flying capacitor converter is represented via:

$$x(k+1) = Ax(k) + b_j(x(k))d_j(k) + h_j(x(k)) \tag{21}$$

where

$$h_j(x(k)) = g + \sum_{\substack{\ell=1 \\ \ell \neq j}}^{3} b_\ell(x(k))\bar{d}_\ell. \tag{22}$$

Notice that $b_j(x)$ and $b_\ell(x)$ are vectors that belong to the original system matrix $B(x)$ in (11).

B. Reference Design

As described in [19], when formulating an MPC strategy, it is convenient to include in the cost function a term to penalize
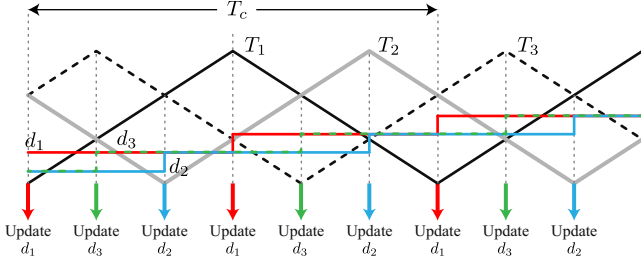
Fig. 2. Standard PS-PWM working in a double update mode.

the control effort. This allows one to regulate the controller bandwidth. To do this, based on $x^\star(k)$ in (13), it is necessary to find the system equilibrium point $(x^\star(k), u^\star(k))$. When the system achieves the desired steady-state, i.e., $x(k) = x^\star(k)$, the controller has to apply $u^\star(k)$ so the system can remain in this steady-state, i.e.,

$$x^\star(k+1) = Ax^\star(k) + B(x^\star(k))u^\star(k) + g. \quad (23)$$

The steady-state input, $u^\star(k)$, can be easily obtained by analyzing the continuous-time model in (3)–(5). Firstly, since a constant reference is desired for each floating capacitor voltage, in the steady-state their derivatives become zero, i.e.,

$$\frac{dv_{C1}^\star}{dt} = \frac{dv_{C2}^\star}{dt} = 0. \quad (24)$$

Thus, from (3) and (4), this condition is achieved whenever the control inputs are equal, i.e.,

$$u_1^\star(t) = u_2^\star(t) = u_3^\star(t) = d^\star(t). \quad (25)$$

Now, a similar approach can be applied to the output current reference. By taking into account (5), (14), and (25), it follows that

$$\frac{di_L^\star(t)}{dt} = -\frac{R}{L}i_L^\star(t) + \frac{V_{dc}}{L}(d^\star(t) - 1/2). \quad (26)$$

Therefore, the steady-state duty cycle to keep the desired system reference in the steady-state is give by:

$$d^\star(t) = \frac{I^\star}{V_{dc}}\big(R\sin(\omega t) + X_L\cos(\omega t)\big) + \frac{1}{2} \quad (27)$$

where $X_L = \omega L$.

Finally, the equilibrium point for the flying capacitor converter can be expressed via:

$$(x^\star(k), u^\star(k)) = \left(\begin{bmatrix} V_{dc}/3 \\ 2V_{dc}/3 \\ i_L^\star(k) \end{bmatrix}, \begin{bmatrix} d^\star(k) \\ d^\star(k) \\ d^\star(k) \end{bmatrix} \right). \quad (28)$$

C. Sequential Optimal Control Problem

To obtain the optimal duty-cycles, the following cost function is introduced

$$J_j(k) = e(k+1)^T Qe(k+1) + \lambda_d\left(\delta_j(k)\right)^2 \quad (29)$$

where

$$\delta_j(k) = d_j(k) - d^\star(k) \quad (30)$$

and $e(k+1)$ and Q are as per (17) and (18) respectively. Moreover, λ_d is the control weighting factor that allows one to trade system state tracking errors versus a control input effort. Finally, the optimal duty cycle is the one that minimizes this cost function, i.e.,

$$d_j^{\text{opt}}(k) = \arg\left\{ \min_{d_j(k)} J_j(k) \right\}. \quad (31)$$

Since at each sampling instant, the cost function only depends on one active input, each optimal duty cycle, d_j^{opt}, can be easily obtained by solving the standard derivative

$$\frac{dJ_j(k)}{dd_j(k)} = 0. \quad (32)$$

This leads to the following explicit optimal solution:

$$d_j^{\text{opt}}(k) = -(W_j(k))^{-1} F_j(k) \quad (33)$$

where

$$\begin{aligned} W_j(k) &= b_j(x)^T Q b_j(x) + \lambda_d, \\ F_j(k) &= b_j(x)^T Q(Ax + h_j(x) - x^\star(k+1)) - \lambda_d d^\star(k) \end{aligned} \quad (34)$$

with $x = x(k)$.

Notice that if λ_d is too large, then the second term in (29) becomes predominant. For this case, the optimal solution becomes $u^{\text{opt}}(k) = u^\star(k)$. This will result in an open-loop slow dynamic given by the natural dynamic of the system. On the other hand, if λ_d is too small ($\lambda_d \approx 0$), then the controller will become in a multi-variable deadbeat controller [21], which can be too aggressive. Therefore, λ_d can be used to regulate the closed-loop bandwidth of the controller.

It is important to emphasize that the proposed sequential PS-MPC strategy can be easily extended to govern flying capacitor converters with a large number of cells. This comes from the fact at each sampling instant only one optimal duty-cycle has to be calculated by evaluating (33), irrespective of the number of cells in the converter.

V. SIMULATION RESULTS

The effectiveness of the capacitor cell voltage balancing for the start-up condition is analyzed by comparing the results of the proposed sequential PS-MPC strategy with those obtained for a standard PS-PWM and standard FCS-MPC. Simulations are carried out on the single-phase four-level flying capacitor converter using the system parameters in Table I.

A. Standard PS-PWM

For this case, each carrier is set to have a frequency of $f_c = 1.5$ [kHz]. Since $\eta = 3$ carriers are required, they are phase shifted by $120°$ with respect to the previous one. This results in an apparent output switching frequency of 4.5[kHz] in the output voltage v_{an}. Figure 3 shows the start-up condition for the standard PS-PWM. In this worst case scenario, the floating voltages raise from 0 to their references in about 150 [ms]. This represents a very slow dynamic. During this period, the power switches are exposed to a blocking voltage larger that $V_{dc}/3$. Notice that the voltage levels are clearly identified only after the capacitor cell voltage balancing is achieved. At this
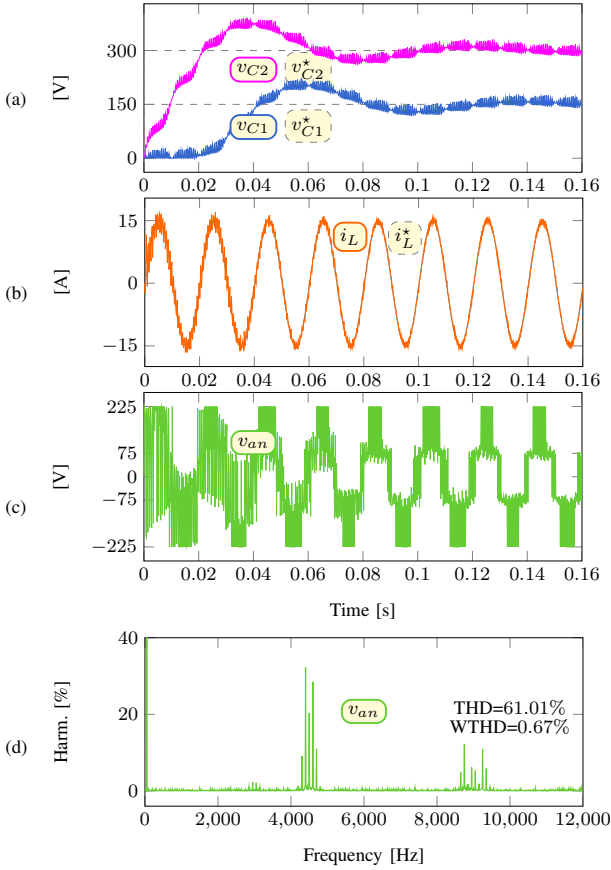
Fig. 3. Standard PS-PWM results: (a) Capacitor voltages and their references, (b) load current, (c) load voltage, and (d) its corresponding steady state spectrum.

Table I
MAIN CONVERTER AND CONTROLLER PARAMETERS.

Parameter	Value
V_{dc}	450 V
R	10 Ω
L	5 mH
$C_1=C_2$	66 μF
$\lambda_1 = \lambda_2$	0.01
λ_d	100
f_c	1.5 [kHz]

time, the output current presents a high quality, while the output voltage is characterized by a fixed spectrum, with the main harmonics centered at $f_{SW} = 4.5$ [kHz] ($f_{SW} = \eta f_c$).

B. Standard FCS-MPC

For this case, the standard FCS-MPC runs with a sampling frequency f_s equal to 9 [kHz]. This limits the maximum switch commutations to $f_{SW} \leq 4.5$ [kHz]. Moreover, the system predictions are obtained by evaluating the system model in (11) with $T_s = T_c/6$. For the same start-up condition, the
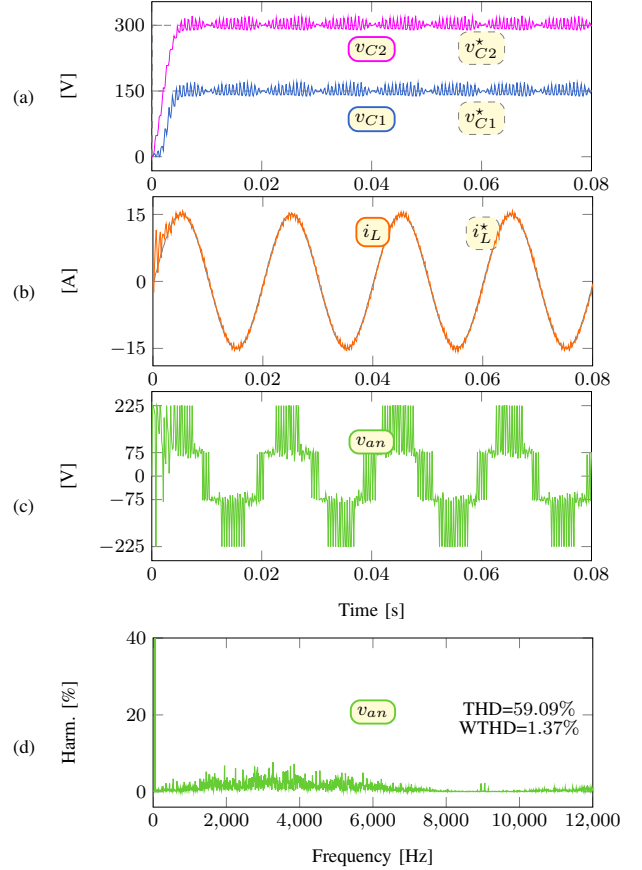

Fig. 4. Standard FCS-MPC results: (a) Capacitor voltages and their references, (b) load current, (c) load voltage, and (d) its corresponding steady state spectrum.

controller governs not only the output current, but also the internal capacitor voltages as shown in Fig 4. Notice that the dynamic of the capacitor cell voltage balancing is improved with respect to the standard PS-PWM. A faster response is achieved, about 5 [ms]. However, a spread spectrum and higher WTHD is obtained. This is due to the fact that more lower order harmonics are generated in v_{an} when compared to using PS-PWM.

C. Proposed Sequential PS-MPC

Due to the double update mode of the PS-PWM, the proposed sequential PS-MPC strategy works with a sampling frequency of 9 [kHz] ($f_s = 2\eta f_c$). Nevertheless, since each optimal duty-cycle, d_j^{opt}, remains constant for half of the carrier period, the system predictions in (21) are evaluated using a sampling period of $T_s = T_c/2$. As with the FCS-MPC case, the resulting voltage dynamics are fast. However, in this case, the output voltage spectrum is fixed (similar to PS-PWM) as shown in Fig 5. Moreover, the same WTHD is obtained between the standard PS-PWM and the proposed sequential PS-MPC strategy, which implies that the small difference in THD is mainly given by high order harmonics, which can be easily filtered out by the load.
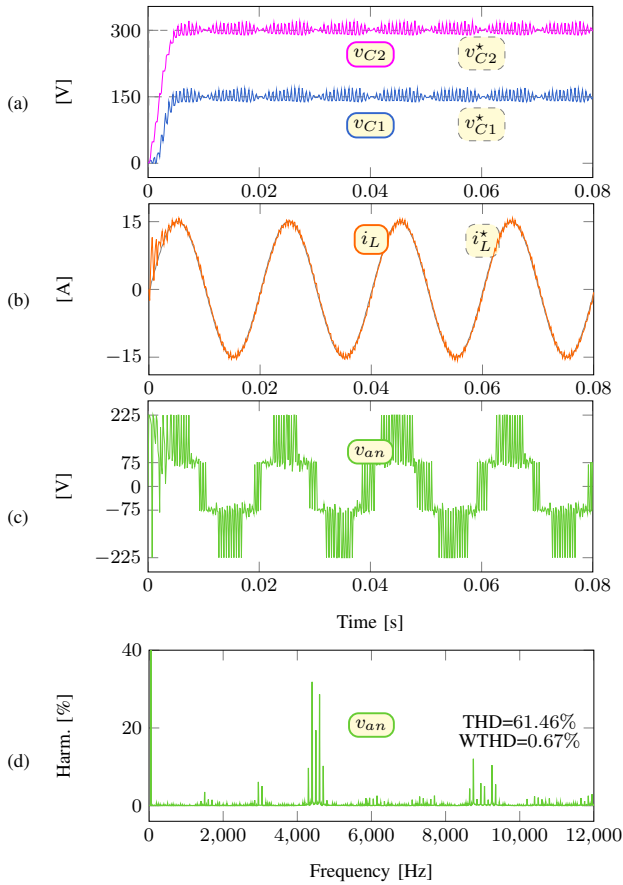
Fig. 5. Proposed Sequential PS-MPC results: (a) Capacitor voltages and their references, (b) load current, (c) load voltage, and (d) its corresponding steady state spectrum.

VI. CONCLUSION

This paper proposed a sequential PS-MPC strategy for multicell power converters. A case study using a single-phase four-level flying capacitor converter has been analyzed. The major benefits of the proposed sequential PS-MPC strategy are: the explicit consideration for the capacitor cell voltage balancing in a sequential manner, which allows one to speed-up the voltage balancing dynamic; and the fixed-spectrum and constant switch commutations obtained in the steady-state. Therefore, the proposed sequential PS-MPC strategy has the potential to outperform both standard PS-PWM and FCS-MPC strategies. Additionally, since only one optimal duty cycle has to be calculated at each sampling instant, the proposed sequential PS-MPC strategy can be easily extend to govern flying capacitor converters with a larger number of cells. Moreover, it can be also applied to other multilevel topologies.

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REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodríguez, M. A. Pérez, and J. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *Industrial Electronics, IEEE Transactions on*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] H. Abu-Rub, J. Holtz, J. Rodríguez, and G. Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *Industrial Electronics, IEEE Transactions on*, vol. 57, no. 8, pp. 2581–2596, 2010.

[3] T. A. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 3, pp. 356–364, Jun 1997.

[4] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodríguez, and B. Wu, "The Essential Role and the Continuous Evolution of Modulation Techniques for Voltage-Source Inverters in the Past, Present, and Future Power Electronics," *Industrial Electronics, IEEE Transactions on*, vol. 63, no. 5, pp. 2688–2701, 2016.

[5] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural Balance of Multicell Converters: The General Case," *Power Electronics, IEEE Transactions on*, vol. 21, no. 6, pp. 1658–1666, 2006.

[6] B. McGrath and D. Holmes, "Analytical Modelling of Voltage Balance Dynamics for a Flying Capacitor Multilevel Converter," *Power Electronics, IEEE Transactions on*, vol. 23, no. 2, pp. 543–550, 2008.

[7] B. McGrath and D. Holmes, "Natural Capacitor Voltage Balancing for a Flying Capacitor Converter Induction Motor Drive," *Power Electronics, IEEE Transactions on*, vol. 24, no. 6, pp. 1554–1561, 2009.

[8] A. M. Y. M. Ghias, J. Pou, G. J. Capella, P. Acuna, and V. G. Agelidis, "On improving phase-shifted pwm for flying capacitor multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5384–5388, Aug 2016.

[9] E. Silva, B. McGrath, D. E. Quevedo, and G. C. Goodwin, "Predictive Control of a Flying Capacitor Converter," in *American Control Conference, 2007. ACC '07*, 2007, pp. 3763–3768.

[10] P. Lezana, R. P. Aguilera, and D. E. Quevedo, "Model Predictive Control of an Asymmetric Flying Capacitor Converter," *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 6, pp. 1839–1846, Jun. 2009.

[11] S. Vazquez, J. Rodríguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model Predictive Control for Power Converters and Drives: Advances and Trends," *Industrial Electronics, IEEE Transactions on*, vol. 64, no. 2, pp. 935–947, 2017.

[12] P. Acuna, R. P. Aguilera, A. M. Y. M. Ghias, M. Rivera, C. R. Baier, and V. G. Agelidis, "Cascade-free model predictive control for single-phase grid-connected power converters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 285–294, Jan 2017.

[13] R. P. Aguilera, P. Acuna, Y. Yu, G. Konstantinou, C. D. Townsend, B. Wu, and V. G. Agelidis, "Predictive control of cascaded h-bridge converters under unbalanced power generation," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 4–13, Jan 2017.

[14] P. Lezana, R. Aguilera, and D. Quevedo, "Steady-state issues with finite control set model predictive control," in *35th Annual Conference of the IEEE Industrial Electronics Society, IECON 2009*, 2009, pp. 1776–1781.

[15] R. P. Aguilera, P. Lezana, and D. E. Quevedo, "Finite-Control-Set Model Predictive Control With Improved Steady-State Performance," *Industrial Informatics, IEEE Transactions on*, vol. 9, no. 2, pp. 658–667, May 2013.

[16] R. Vargas, U. Ammann, and J. Rodríguez, "Predictive Approach to Increase Efficiency and Reduce Switching Losses on Matrix Converters," *Power Electronics, IEEE Transactions on*, vol. 24, pp. 894–902, 2009.

[17] V. Yaramasu, M. Rivera, M. Narimani, B. Wu, and J. Rodríguez, "Model Predictive Approach for a Simple and Effective Load Voltage Control of Four-Leg Inverter With an Output *LC* Filter," *Industrial Electronics, IEEE Transactions on*, vol. 61, no. 10, pp. 5259–5270, 2014.

[18] R. P. Aguilera and D. E. Quevedo, "On stability and performance of finite control set MPC for power converters," in *PRECEDE 2011 - Workshop on Predictive Control of Electrical Drives and Power Electronics*, Munich, Germany, Oct. 2011, pp. 55–62.

[19] R. P. Aguilera and D. E. Quevedo, "Predictive Control of Power Converters: Designs With Guaranteed Performance," *IEEE Transactions on Industrial Informatics*, vol. 11, no. 1, pp. 53–63, 2015.

[20] R. P. Aguilera, P. Acuna, P. Lezana, G. Konstantinou, B. Wu, S. Bernet, and V. G. Agelidis, "Selective Harmonic Elimination Model Predictive Control for Multilevel Power Converters," *Power Electronics, IEEE Transactions on*, vol. 32, no. 3, pp. 2416–2426, Mar. 2017.

[21] D. E. Quevedo, R. P. Aguilera, and T. Geyer, "Predictive Control in Power Electronics and Drives: Basic Concepts, Theory, and Methods," in *Advanced and Intelligent Control in Power Electronics and Drives*. New York, NY, USA: Springer, 2014, pp. 181–226.