

Dual polarity DC–DC converter integrated grid-tied single-phase transformer less inverter for solar application

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Abstract: This study proposes a novel single-phase transformer-less inverter, using the principle of combined Ćuk SEPIC (CCS) converter for grid-connected photovoltaic (PV) systems. The new inverter has a common ground between the grid and the PV source, which helps to eliminate the leakage current for the grid-connected PV application. Unlike common ground-type charge-pump-based transformer-less inverter, this topology eliminates inrush current and hence reduces the current stress on the components. The CCS allows voltage control with both step-up and step-down abilities, along with more robustness against solar panel side fault. Further, application of wide band-gap devices, such as SiC MOSFETs allows higher switching frequency to be achieved, and thus reduction of the passive components. A novel switching strategy, proposed here allows current in both directions, positive and negative (to the load/grid or from the load/grid, for reactive loads), making the converter suitable for grid connection (unity power factor), as well as stand-alone operation. The proposed concept has been discussed in detail, along with simulation results. Finally, a prototype hardware has been fabricated and the experimental results are reported.

1 Introduction

Grid-connected photovoltaic systems (PVs), particularly low power single-phase systems (up to 5 kW) are becoming more common worldwide, due to declining PV price, government incentives and advancement in power electronics and technology [1]. To date, the PFC boost converter, coupled with H-bridge and transformer has been the most popular topology for PV systems. Besides providing the additional capability to adjusting voltage level, the inherent galvanic isolation blocks common mode (CM) current and limits the fault current. However, due to weight and volume of the line frequency transformer, different topologies [2, 3] have been proposed to avoid them without losing the main benefit of blocking CM current. It has been previously reported, by using a virtual DC bus [4], the common ground connection can be achieved, which diverts CM current.

In this paper, a novel converter topology has been proposed based on dual polarity DC–DC converter, which creates separate positive and negative virtual DC bus; thus allowing the common ground connection of the solar panel with the grid. The dual polarity DC–DC converter allows more flexibilities for voltage control with both step-up and step-down abilities, along with more robustness against solar panel side fault.

The next section details the converter topology and operating principles, along with pulse width modulation (PWM) strategy of different switches in the converter. The proposed converter has been investigated with simulation studies, using MATLAB-Simulink and PLECS, and the results are reported. Finally, a laboratory prototype has been developed and experimental results are presented to validate the concept.

2 Converter topology and operation

The circuit schematic of the converter is shown in Fig. 1. The converter can be analysed as a two-part system, consisting of a combined Ćuk SEPIC (CCS) converter [5] along with a bipolar DC to single phase AC converter. The CCS converter generates a bipolar DC output, which is referred as virtual DC bus. The switching node of the Ćuk and SEPIC converter is unified by the switch S_1 . The Ćuk converter generates a negative voltage with respect to the common ground node G , at node N . Similarly the SEPIC converter creates the positive voltage output at node P with

respect to the ground. The output of the Ćuk and the SEPIC converter is related to input.

DC voltage as

$$V_{\text{Cuk}} = -V_{\text{in}} \frac{d}{1-d} \quad (1)$$

$$V_{\text{SEPIC}} = V_{\text{in}} \frac{d}{1-d} \quad (2)$$

where V_{in} is the input DC voltage, and d is the duty ratio of the switch. The dual polarity output generated by this CCS converter, between nodes P , N and G , is fed to the bipolar DC to single phase AC converter consisting four switches S_p , S_n , S_{zp} , and S_{zn} , which produces an AC output. It can be observed, the load neutral point, node G is common to the source ground, thus allowing a common ground connection which eliminates the CM leakage current.

Switch S_p of the bipolar DC–AC converter is switched in sine PWM during the positive half cycle. During switch-on period – positive –active, the circuit path is shown in Fig. 2 – positive voltage active. The anti-parallel diode with the MOSFET allows the current path for both the directions. When the switch S_p is turned off, the zero state switches – S_{zp} and S_{zn} , need to be turned on, to allow the current path for the load. Depending on the direction of the current, it can take either of the two paths. For the current to the load (positive direction) the path is completed by the

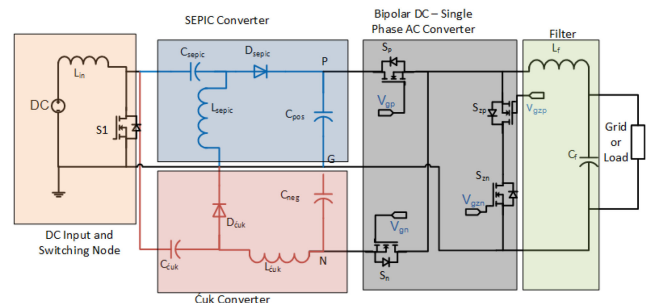


Fig. 1 Converter topology

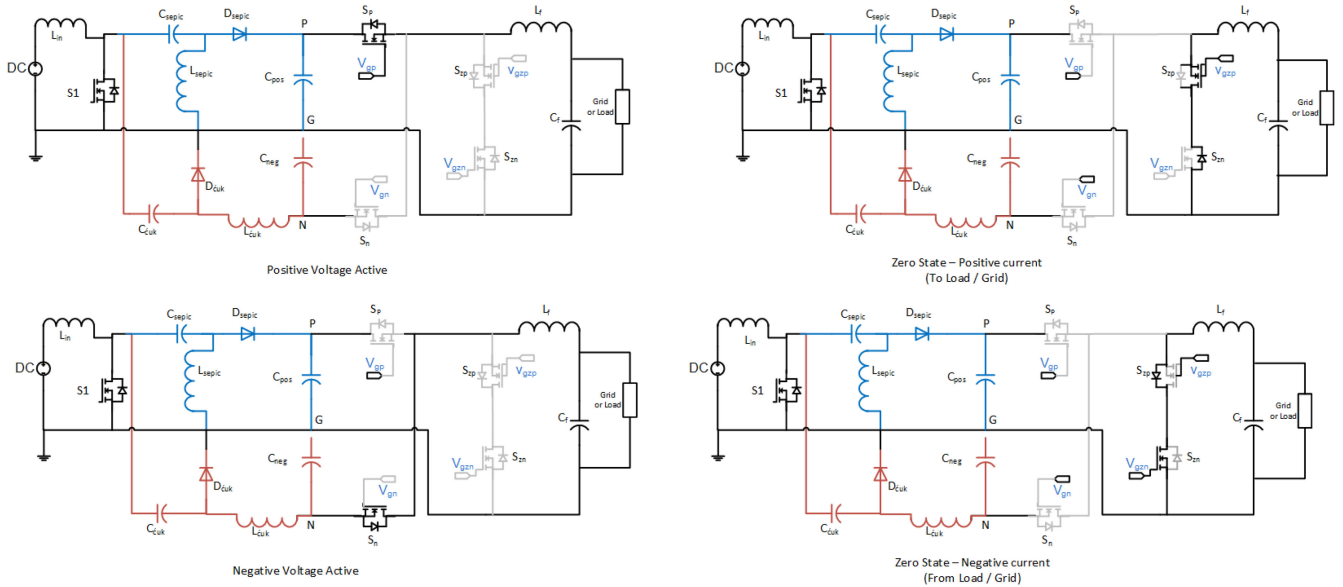


Fig. 2 Converter operation modes

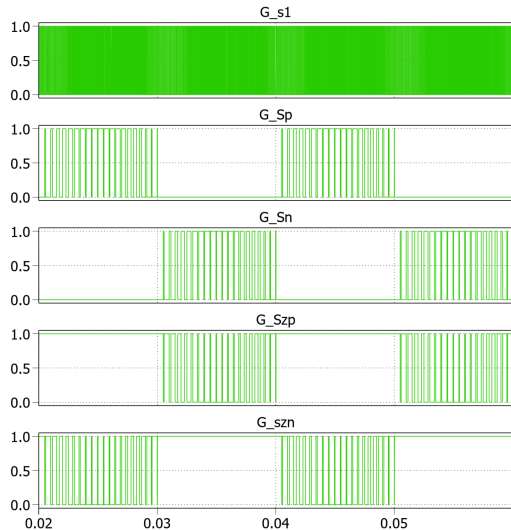


Fig. 3 PWM pulses of different switches

anti-parallel diode of the switch S_{zn} and the MOSFET S_{zp} as shown in Fig. 2. For negative current, current from the load or grid side, the path is completed by the S_{zn} and the anti-parallel diode of S_{zp} , also shown in Fig. 2. It should be noted, while the switch S_{zp} can be kept on during the positive half cycle of voltage, as the anti-parallel diode of S_{zn} blocks the path for current. However, during the switch-on period of S_p , S_{zn} must remain turned off, otherwise, it will lead to short circuiting across the nodes P and G . This will require switching only S_p and S_{zn} in a complementary fashion, during positive half cycle. This strategy will reduce switching loss of the converter, as S_{zp} is not switched, although it provides current path as necessary. However, to ensure there is no short circuit, a dead time has to be inserted between the gate pulses of S_p and S_{zn} . During this dead time period, when neither of the switches is on, in case of positive current, the path is completed by S_{zp} and anti-parallel diode of S_{zn} . However, if the load/grid current is negative during a particular switching, the path is completed by anti-parallel diode of S_p and feeding back to the positive DC bus (node P) capacitor C_{pos} .

Similarly, during the negative half cycle of voltage, the negative bus switch S_n is switched in sine – PWM fashion, shown in Fig. 2 – negative active. To provide the circulating current path, during off period, similar to the positive half cycle, S_{zp} and S_{zn} are switched, and the operation modes are same as before. During this negative

Table 1 Converter and component size and rating

Component	Size
converter	1 kW
input (nominal)	360 V
input range	290 to 400 V
output	240 V (RMS), 50 Hz
L_{in}	546 μ H
L_{SEPIC} , L_{Cuk}	890 μ H
C_{SEPIC}	1 : 19 μ F
L_{Cuk}	0 : 47 μ F
C_{pos} , C_{neg}	500 μ F
L_f	330 μ H
C_f	1 μ F

half-cycle period, S_{zn} can be kept on, while S_{zp} being switched complementarily with S_n . Similar to the positive half cycle, here too, dead time should be inserted between the pulses of S_n and S_{zp} . Finally, the output of the bipolar-DC to single-phase AC converter is fed to an LC filter, before connecting to the load (in case of stand-alone operation) or grid.

The PWM pulses for the switches in the converter, S_1 , S_p , S_n , S_{zp} , and S_{zn} are shown in Fig. 3. The x -axis (time) is not to scale, to show the sine – PWM pattern of the switches of the AC converter. S_1 is switched at high frequency, 100 kHz to keep the size of the passive components of the CCS small. Further, increasing the switching frequency of S_p , S_n , S_{zp} , and S_{zn} will allow redirection in size of the filter components L_f and C_f .

3 Simulation results

Having discussed the topology of the converter, and operation principle, a MATLAB-Simulink and PLECS-based simulation model has been developed to study the converter in details. The specification of the simulated converter specification along with the component size is given in Table 1.

The converter has been simulated with nominal 360 V as well as the limit input voltages (290 and 400 V). \hat{C}_{uk} converter generates a negative voltage between nodes N and G . The duty ratio of S_1 has been controlled in a closed loop to maintain the desired voltage across capacitor C_{pos} and C_{neg} , as the load of both the \hat{C}_{uk} and the SEPIC converter changes from zero to peak in each negative half cycle and positive half cycle, respectively. Further, the closed-loop operation takes care of no-load operation of the \hat{C}_{uk} converter during the positive half cycle, otherwise

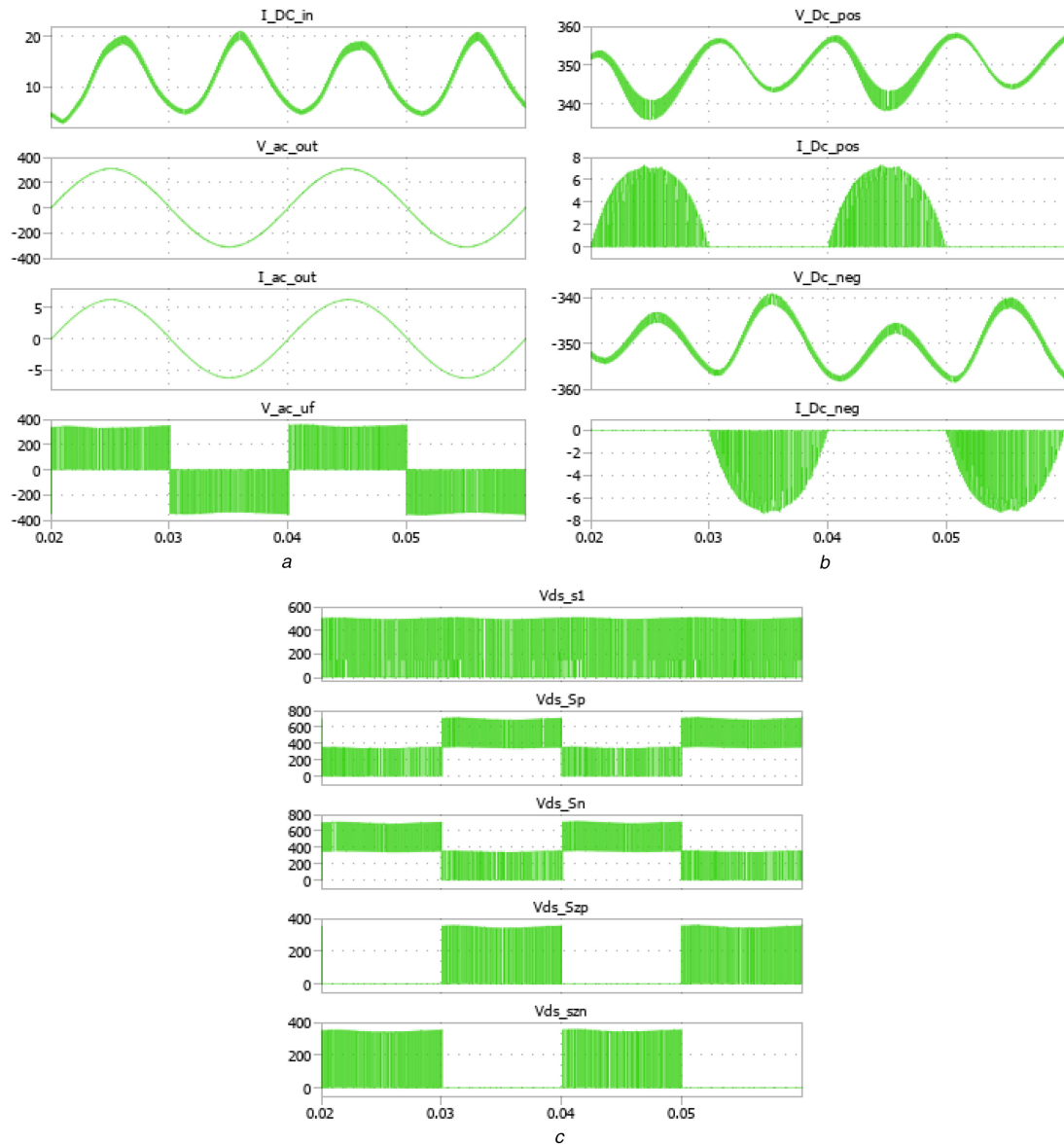


Fig. 4 Simulation results

which can lead to voltage buildup across C_{neg} . Further, the bipolar DC-AC converter also takes feedback of DC bus voltage level, to generate a 240 V RMS, 50 Hz output.

The simulation results for input voltage 290 V, where input current will be maximum, are presented in Fig. 4. It can be observed that the closed-loop controller is working to maintain the DC bus voltage at ± 350 V. However, due to the variation of load in 50 Hz sinusoidal fashion, there is a voltage ripple of 50 Hz frequency, on top of smaller variation at switching frequency of S_1 . However, the net peak-to-peak variation is kept $< 5\%$ of the rated bus voltage for both Čuk and SEPIC converter.

It can be further observed that the higher switching frequency of the bipolar DC-AC converter, along with the filter, generates a sinusoidal voltage output, with very less THD content. THD was measured to be 0.8%. The drain-source voltage of different switches was measured too. The maximum voltage across switches S_p and S_n goes up to 700 V, which is the total voltage across positive and negative DC nodes P and N respectively. However, the novel switching strategy discussed in the previous section results in lesser voltage stress across switches S_{zp} and S_{zn} as only two of the four switches of the bipolar DC-AC converter is switched at the PWM frequency. The maximum voltage stress across these two switches are same as individual virtual DC bus voltage levels, not the total.

4 Experimental validation

A prototype has been developed for experimental validation of the proposed converter. To achieve a high switching frequency, particularly for the switch S_1 a Sic MOSFET (CREE C3M0075120K) has been used, as this offers capability to switch at frequency up to 500 kHz and voltage rating up to 1.2 kV. For rated operation of the converter (240 V RMS output), the voltage stress across the switches S_p and S_n is shown to be 700 V for ± 350 V virtual DC bus level. Further, as discussed in the previous section, ability to switch the bipolar DC-AC converter at a higher frequency, allows the lower size of the filter. Hence the same MOSFET has been used there too. Silicon carbide Schottky diodes (STPSC20H12) has been used for the CCS converter. A TI 28069M launchpad digital signal processor controller has been used as the PWM sources.

To maintain modularity, and easy debugging and probing during prototype building, the converter was also made as two-part system. The first part consists CCS converter and generates a bipolar DC output from the unipolar DC input. The other converter is designed to take in the bipolar output of the previous converter as its input, and generate single phase AC, which can be connected to grid or operated in standalone mode. Fig. 5a shows the laboratory prototype of CCS converter. Figs. 5b and c shows the developed bipolar DC-AC converter. Further, the inductors for CCS converter too were built in the laboratory, using nanocrystalline core, as shown in Fig. 5d

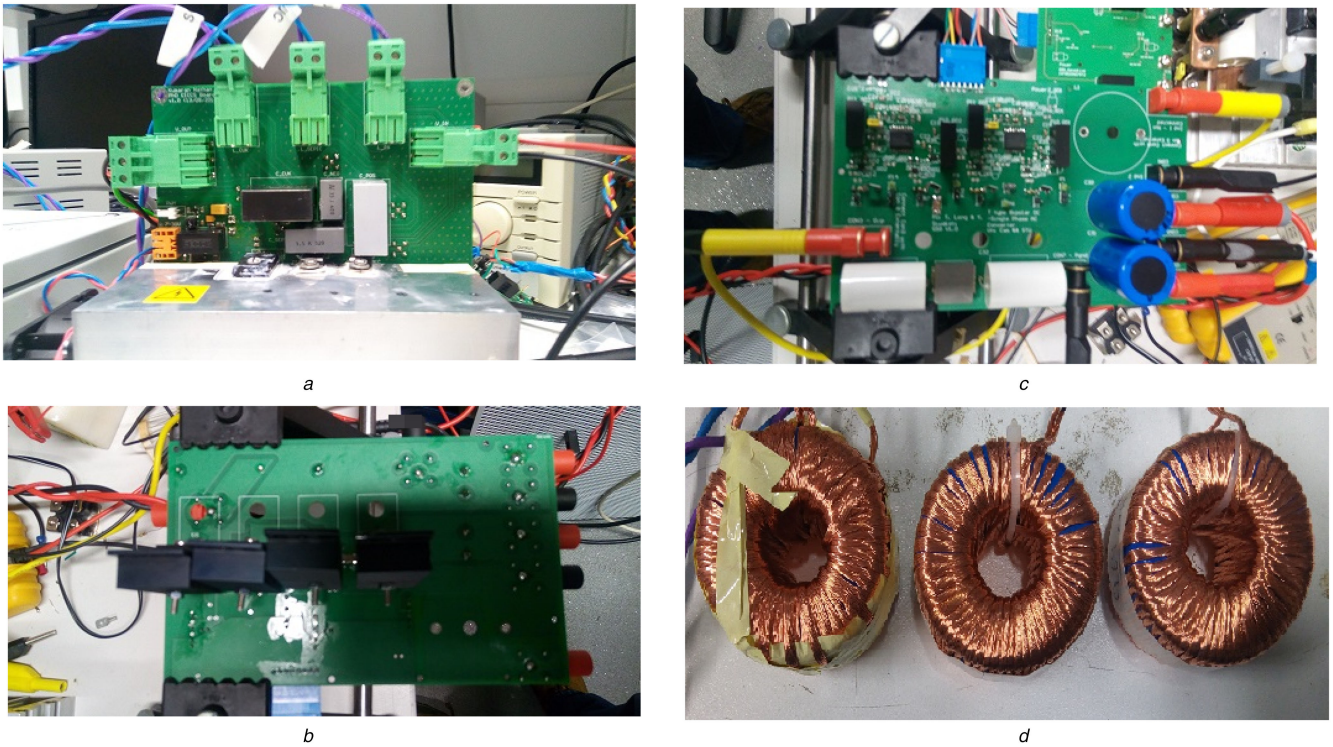


Fig. 5 Fabricated converter
 (a) Combined Ćuk Sepic converter, (b) Bipolar DC-single phase AC converter – gate drive side, (c) Bipolar DC-single phase AC converter – power switches, (d) Used inductors

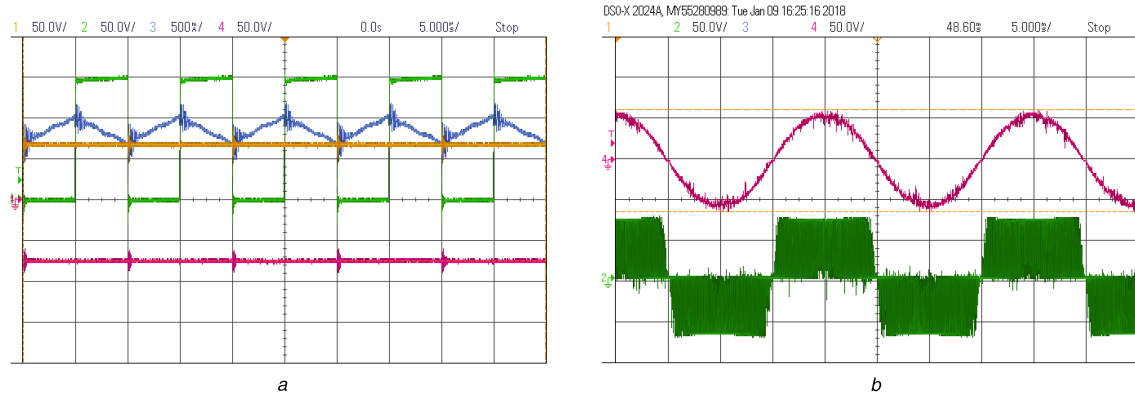


Fig. 6 Experimental results:
 (a) CCS converter: Ch1: V_{DC+} ; Ch2: V_{DS} across S_1 ; Ch3: input current; Ch4: V_{DC-} , (b) Output: Ch4: output AC, Ch2: output before filter

Experimental results were taken at input DC voltage of 75 V and a 47 Ω resistive load. Switching frequency of S_1 was kept at 100 kHz. The bipolar DC-AC converter switches S_p , S_n , S_{zp} , and S_{zn} were switched at 20 kHz. The experimental results of the CCS converter is shown in Fig. 6a. The duty ratio of the switch S_1 is set to 0.5. For a 75 V input, Fig. 6a shows ± 75 V across positive and negative DC bus in channels 1 and 4, respectively. Fig. 6b shows the output of the bipolar DC-AC converter before and after the filter. It can be observed that similar to simulation result the THD present in the output AC is very less. Further, the drain-to-source voltages across different switches of the bipolar DC-AC converter was measured, and shown in Fig. 7. In line with the simulation result, for a ± 75 V virtual DC bus, V_{DS} across the switches S_p and S_n go to 150 V, whereas, the voltage across the switches S_{zp} and S_{zn} remain 75 V.

5 Conclusions

In this paper, a novel converter topology, based on CCS converter for solar application, has been presented. The CCS converter creates virtual bipolar DC bus, and a bipolar DCAC converter feeds to AC. Further, a novel PWM strategy for the bipolar DC-AC converter has been reported, which requires only two switches

to be switched at high frequency in either of the positive or negative half cycles. Moreover, the converter allows common ground connection between the input DC source and AC. This feature is particularly helpful for blocking CM current in the grid-connected solar converters. The proposed converter topology along with PWM strategy has been discussed in detail. Further, both simulation and experimental results of the fabricated hardware laboratory prototype has been reported in detail to validate the concept. In this paper, only open-loop experimental results are presented. Closed-loop control of the converter, along with the grid connection of the AC output of the converter will be presented in future work.

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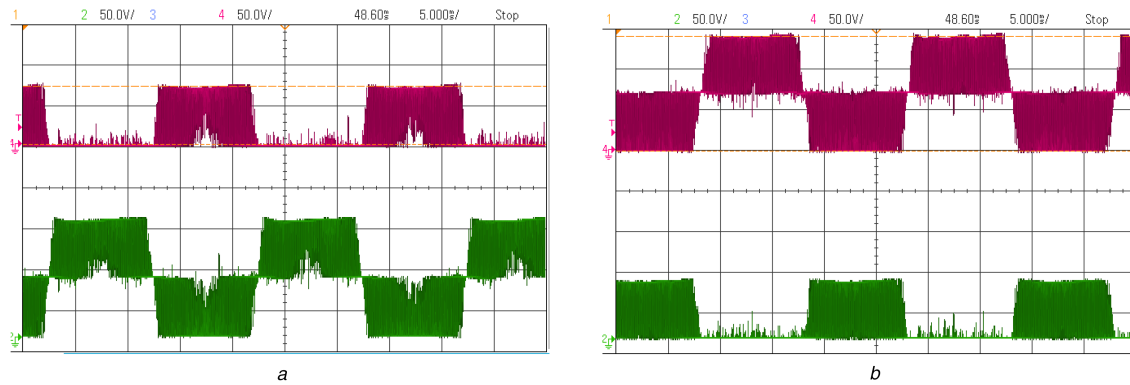


Fig. 7 V_{DS} across switches of bipolar DC-AC converter
 (a) V_{DS} across S_p [ch4] and S_{zp} [ch2], (b) V_{DS} across S_{np} [ch4] and S_n [ch2]

7 References

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