A Least Mean Square Algorithm Based Single-Phase Grid Voltage Parameters Estimation Method

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***Abstract*—Grid-synchronization may be the most significant task in order to integrate renewable energy sources (RESs) and electric vehicles (EVs) into the power grid. The popular technique for grid synchronization is the power based phase locked loop (PLL). The major challenges that one encounters to design a robust power based PLL is the filter design inside the power based PLL control loop, and estimating the grid voltage parameters under frequency drift conditions. A wide bandwidth should be considered during filter design if a wide range of frequency variations are predicted in the grid voltage. The traditional filters cause a large phase delay if a wide bandwidth is considered during filter design. As a result, it degrades the transient performance of the power based PLL. In order to improve the transient performance of the PLL, this paper adopted a Fourier linear combiner (FLC) filter inside the PLL control loop. Moreover, a feedback loop is used to make the FLC frequency adaptive in order to estimate the grid voltage parameter when grid frequency drift occurs. Simulation and experimental results are provided to verify the proposed technique.**

Keywords—FLC algorithm, notch filter, grid synchronization, LMS algorithm, transient performance.

I. INTRODUCTION

Grid-connected converters are the key component used to integrate renewable energy sources (RESs) and Electric vehicles (EVs) into the grid. The high penetration of DESs such as PV energy, wind energy (WE), energy storages (ESs), and fuel cells requires a robust controller design for these converters [1]. The estimation of the grid voltage parameters is required in order to design a controller for the converters. Moreover, the control of the real and reactive power for grid-tied microgeneration systems requires accurate grid voltage parameters (e.g. frequency and phase) information. A robust controller design requires a faster estimation of the power-grid voltage parameters [2]-[3]. The popular method for grid voltage parameters estimation is the phase-locked-loop (PLL). A basic phase locked loop block diagram is shown in Fig. 1.

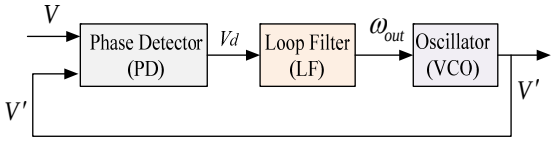

Fig. 1. Basic PLL structure.

The reported attractive PLL methods in the recent literature may be classified into two main categories: power-based PLL methods (pPLLs) and quadrature signal-based PLL methods (QSG-PLLs). For the power based PLLs, the main difference in their configurations is the type of phase detector (PD) used in their structures. In the power based PLL configurations, a product type phase detector is used to generate the phase-error information. The output of phase detector consists of a double-grid frequency (*2f*) component that varies at twice of the grid frequency. This *2f* component should be removed from the output of the phase detector to get the phase error information [1]-[3].

The disadvantage of the power based PLL is that it does not give information about the grid voltage amplitude [4]-[5]. In recent years, numerous power based PLL methods have been proposed in the literature like LPF-pPLL, NF-pPLLs, MAF-pPLL, DFAC-pPLL and, MMPD-pPLL. In order to make these PLLs frequency adaptive for a wide frequency variation, the filter used in the PLL control loop should be designed with a high bandwidth. As a result, it generates a significant phase delay in the control loop. Consequently, these PLL approaches present slow dynamic performances under distorted grid conditions. Furthermore, some of the power based PLL techniques require an accurate amplitude normalization of the grid voltage signal. Consequently, the implementation of these PLL techniques is a difficult task [6]-[7].

In order to suppress the double-frequency ripple component from the output of the product type phase detector, a notch filter (NF) based approaches are suitable. A basic power based NF-PLL structure is shown in Fig. 2.

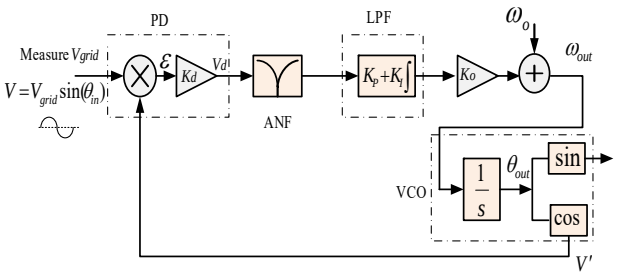

Fig. 2. Conventional notch filter based PLL structure.

The notch filter based approaches present less distortion of the input signal compared to other approaches. However, this PLL technique can not estimate the grid parameters accurately under off-nominal frequencies. Therefore, NF based PLL is not suitable where a large frequency variation occurs. In order to design the PLL frequency adaptive, several adaptive notch filter based PLLs are presented in the recent literature. However, these approaches are sensitive to grid disturbances to estimate the frequency, particularly when grid voltage sag and phase step occurs. Some filtering approaches like finite impulse response (FIR) based notch filter (FIR-NF) and non-adaptive infinite impulse response based filter (IIR) are used inside the PLL control loop to suppress the *2f* ripple part [4]-[7]. These filtering approaches present satisfactory result in removing the *2f* term even when a large frequency variation occurs in the grid voltage. However, the major problem associated with these methods is that the large bandwidth selection causes a high phase delay, and therefore, degrades the PLL transient performance under distorted grid conditions. Recently, several other power based PLL approaches such as double frequency and amplitude compensation based PLL, modified mixer PD Based PLL have been introduced to improve the PLL performance under distorted grid voltage conditions. However, these techniques are complex and difficult to implement and require long computation time. The use of traditional filters in the PLL control loop causes filtering delay and suffer from sensitivity in the presence of frequency fluctuation of the utility voltage. To address the limitation of the traditional filters, this paper adopted a Fourier Linear Combiner (FLC) filter inside the power based PLL to improve the transient performances under distorted grid conditions. Moreover, a feedback loop is used to make the FLC frequency adaptive in order to estimate the grid voltage parameters under grid frequency variations in the proposed PLL structure. The block diagram of the proposed approach is shown in Fig. 3.

II. Proposed Method

The major problem regarding the single phase power based PLL methods is to calculate the power-grid voltage parameters during the frequency variations and slow transient performance under distorted grid conditions. To overcome this challenge, a modified Least Mean Square (LMS) algorithm, i.e. (Fourier Linear Combiner (FLC) [8] filter is adopted inside the proposed PLL method to remove the *2f* component from the output of the phase detector. Furthermore, to make the PLL frequency adaptive under power grid-frequency changes, the frequency estimated by the PLL is utilized to make the adopted FLC filter frequency adaptive.

In the proposed structure, the FLC algorithm is used as an adaptive frequency estimator and removes the double grid frequency component which is a by-product of the phase detector in the power based PLL structure.

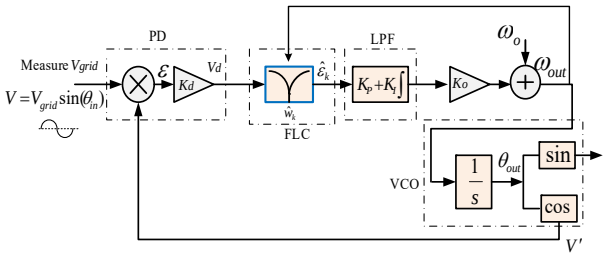

Fig. 3. Proposed PLL block diagram.

The FLC algorithm is given by [8]

$$x_{r_k} = \begin{cases} \sin\left(r\sum_{t=1}^{k} w_{0_t}\right), & 1 \le r \le M \\ \cos\left((r-M)\sum_{t=1}^{k} w_{0_t}\right), & M+1 \le r \le 2M \end{cases} \quad (1)$$

$$\varepsilon_k = s_k - w_k^T x_k \quad (2)$$

$$w_{k+1} = w_k + 2\mu x_k \varepsilon_k \quad (3)$$

$$x_k = \left[x_{1_k} \ldots\ldots x_{2M_k}\right]^T \quad (4)$$

where x_k denotes the vector of the Fourier harmonic components, w_{0_k} represents the adaptive weight which is corresponding to the grid voltage fundamental frequency component w, s_k represents the input signal component, and ε_k is the modelling error.

$$w_k = \left[w_{1_k} \ldots\ldots w_{2M_k}\right]^T \quad (5)$$

where μ_o denotes the adaptive gain that governs the adaptation of frequency, w_k represents the weight vector, and this vector quantity approximates the input signal amplitude information and phase information, *M* represents the total number of harmonic components in the model, μ denotes the adaptive gain that governs the adaptation of the signal amplitude.

III. Performance Analysis

This section presents the performance of the proposed phase locked loop method. Simulation studies have been conducted by using MATALB/Simulink environment and compared with the traditional notch filter based PLL method under distorted grid conditions. In this work, the sampling

frequency is selected as 50 kHz. The power grid frequency is set to 50 Hz in the simulation studies.

A. Phase Jump (90^0)

Figs. 4, and 5 illustrate the simulation results of the conventional phase locked loop method, and the proposed method, respectively, for a grid voltage phase jump of 90^0. It can be observed that the phase error decreases to zero in about 70 ms (3.5 cycles) for the conventional PLL approach and 40 ms (2 cycles) for the proposed approach.

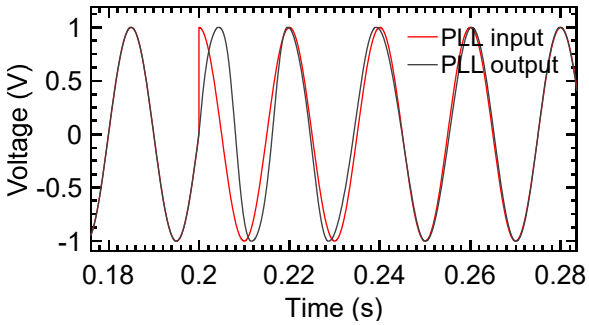

Fig. 4. Conventional PLL response (90° phase Jump)

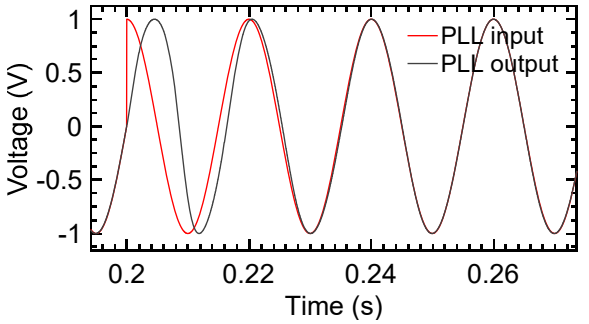

Fig. 5. Proposed PLL response (90° phase Jump)

B. Frequency Shift (5 Hz)

Figs. 6 and 7 illustrate the simulation results of the conventional and the proposed methods, when the power grid voltage experiences a frequency drift of 5 Hz. It can be seen that the proposed PLL output frequency is locked to the input voltage in about 20 ms with the proposed PLL method, while the NF-PLL cannot lock to the input voltage in the case of frequency drift condition.

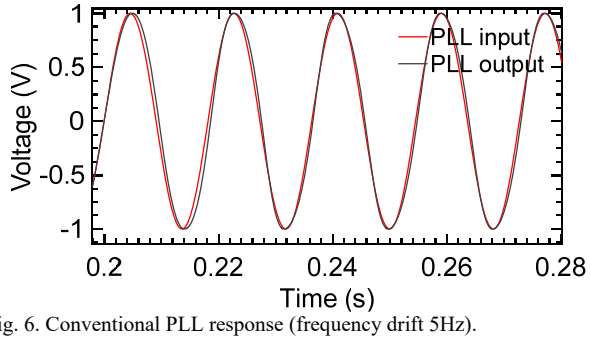

Fig. 6. Conventional PLL response (frequency drift 5Hz).

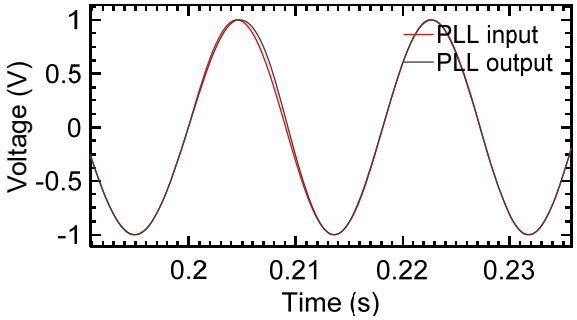

Fig. 7. Proposed PLL response.

C. Voltage Sag (20%)

Figs. 8 and 9 illustrate the performance analysis of the traditional power-based approach and the proposed grid-synchronization approach, respectively, when the power grid voltage experiences a voltage sag of 20%. As it can be observed that, both methods present a fast transient performance in estimating the grid voltage information.

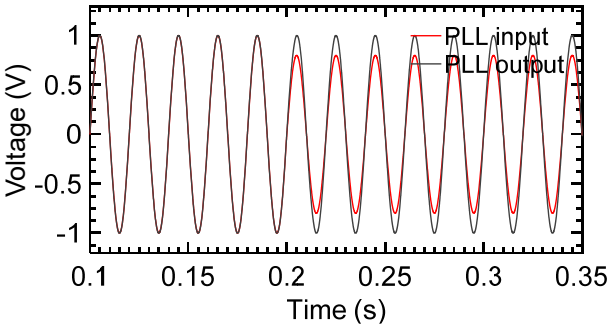

Fig. 8. Conventional PLL response (voltage sag 20%)

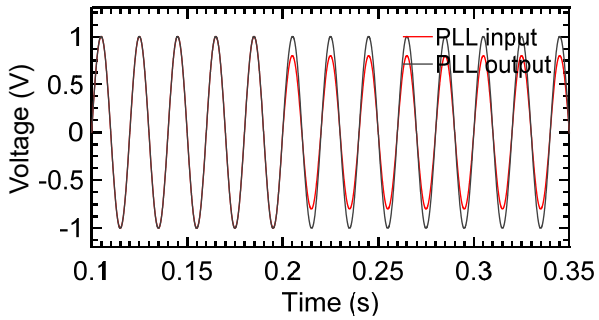

Fig. 9. Proposed PLL response (voltage sag 20%)

D. Harmonic Distortion (5^{th} harmonic injection)

Figs. 10, and 11 illustrate the performance analysis of the conventional PLL approach, and the proposed approach, respectively when 10% fifth-harmonic component is injected into the grid voltage signal. It can be observed that the harmonic elimination performance is similar for the conventional and the proposed approaches. Fig. 12 shows the FFT analysis of the output signal of the proposed PLL approach.

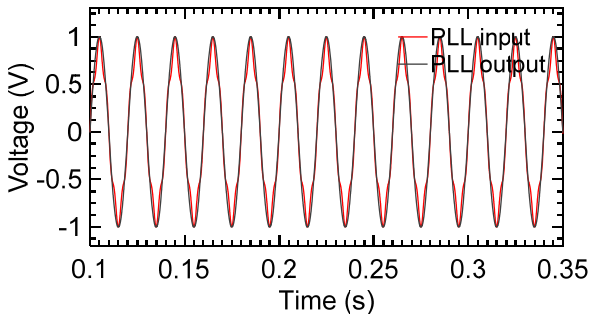

Fig. 10. Conventional PLL response (5th harmonic distortion)

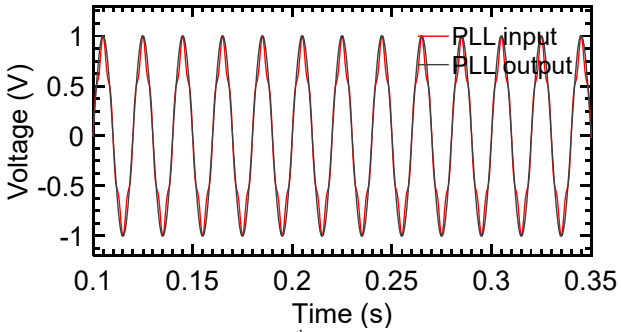

Fig. 11. Proposed PLL response (5th harmonic distortion)

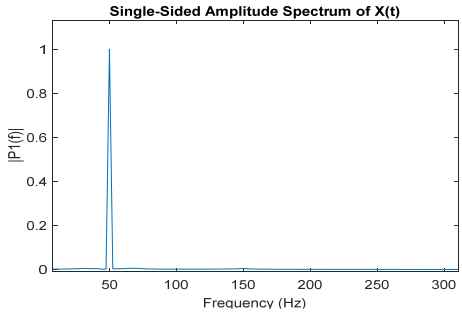

Fig. 12. FFT analysis of the PLL output signal.

IV. Experimental Results

To verify the proposed method, four different grid fault conditions have been generated by using a TMS320F28379D floating-point digital signal controller (DSC) from Texas Instruments as an alternative of the programmable ac voltage source. The performance of the proposed PLL method is verified with the generated grid fault conditions. Experimental studies are conducted considering a 20 kHz sampling frequency. To evaluate the proposed approach in estimating the grid frequency under grid frequency variation, a frequency jump from 50 Hz to 55 Hz is introduced in the input signal. Fig. 13 shows the experimental result. Clearly, the proposed method presents a fast transient performance in estimating the grid frequency for frequency drift condition, and the transient lasted less than 40 ms. Fig. 14 shows the experimental results for 90° phase shift of the input signal. It is worth noting that the proposed approach provides fast transient performance to estimate the grid information. The observed settling time was around than 50 ms. Fig. 15 shows the performance of the PLL for 50% voltage sag in the input voltage. The proposed PLL confirms a quicker dynamic response. The settling time of the proposed method is less than 40 ms. Finally, considering the grid voltage with 10% 3rd harmonic and 5% 5th harmonic, the proposed PLL provides robust harmonic elimination property of the grid voltage as presented in Fig. 16.

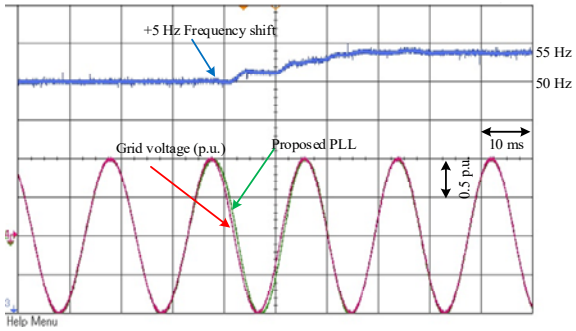

Fig. 13. Experimental results for frequency jump of the grid voltage.

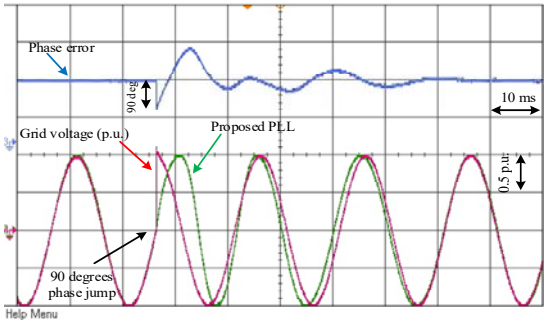

Fig. 14. Experimental results phase shift of the grid voltage.

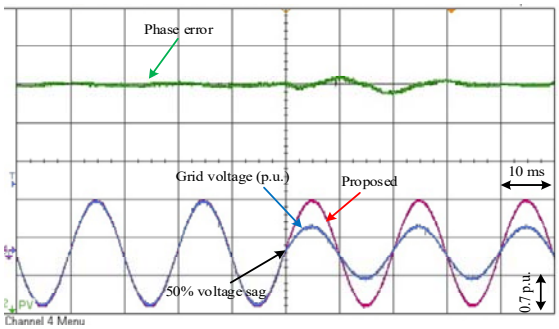

Fig. 15. Experimental results for amplitude variation of the grid voltage.

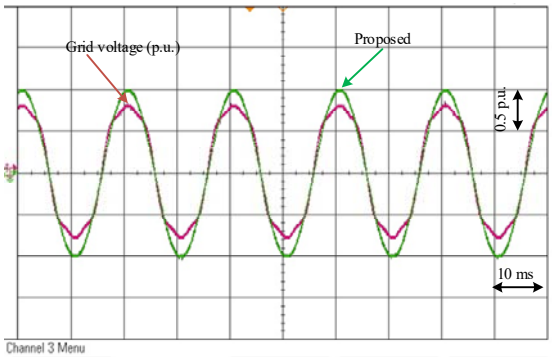

Fig. 16. Experimental results in the existence of grid voltage harmonics.

V. Conclusion

In this paper, a modified power based PLL structure is introduced. The proposed method adopted an FLC filter to suppress the double grid frequency term from the output of the phase detector. The proposed approach provides a fast transient performance in estimating the grid voltage parameters under distorted grid conditions. Moreover, it can also estimate the grid frequency under off-nominal frequencies. Simulation and experimental studies are conducted to confirm the performance of the proposed approach.

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