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Controllable reactor based hybrid HVDC breaker

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Abstract: Short circuit fault occurrence in high-voltage DC (HVDC) systems causes extremely high currents in a fast raising time that does not experience current zero-crossing. To protect HVDC systems/grids against fault current, fast HVDC breaker is an essential equipment. This study presents the design procedure of a novel HVDC breaker based on solid-state controllable reactor which is able to reduce the fault current's rate of rise and fault current amplitude to less than grid nominal current in the breaking process. The main achievement of the proposed HVDC breaker is that not only breaker does not encounter fault current, but also none of the series HVDC equipment is influenced by the fault. The designed breaker performance is studied by PSCAD/EMTPS, and then the simulation results are validated by the developed laboratory experimental setup.

1 Introduction

The development of renewable energy market through the so-called supergrids would be a promising solution by launching of high-voltage DC (HVDC) grids [1]. On the other hand, HVDC grids are very much vulnerable to DC faults. When a DC fault takes place, the relatively low impedance of HVDC system/grid is a tremendous challenge as fault penetration is much faster and deeper than in the case of AC systems [2]. In recent years, several ideas for HVDC breaker have been introduced, but performance of the presented solutions has been always debated [3–6].

Generally, main characteristics of HVDC circuit breakers are [4]:

- Rapid breaking capability
- Minimum conduction losses
- Reliable and efficient protection
- Repetition possibility of switching operation
- Prevention of excessive overvoltages
- Minimum arc after separation of the mechanical contactors

Active and passive resonant breakers as slow breakers were solutions for old DC systems [4–6]. Recently, the hybrid breaker technology as a fast breaker for HVDC grids applications has introduced [7–11]. Conductive power losses of hybrid breaker are fairly low because of using solid-state load commutation switch (LCS) [9]. Multiline breaker and active mechanical breaker are two recent ideas to improve hybrid breaker technology [10, 11].

On the other hand, fault current limiters are types of protection devices, which have recently introduced to improve HVDC systems protection [12, 13]. A design procedure of superconductive FCLs is presented in [14]. In [15], superconductor technology based FCL is studied to improve hybrid HVDC breaker. In [16], a DC reactor solid-state FCL is presented that uses a superconductive technology with high capability of DC fault current limiting. At the present day, hybrid HVDC breaker that consists of a current-limiter reactor is commercialised [9, 17].

In [18], a new LC type DC breaker is presented. In [19–22], a limiter reactor is used to improve operation of breaker. To upgrade technical operation of DC circuit breaker, novel topologies are presented in [23–25].

In this paper, a controllable reactor based HVDC breaker (HCR-B) is proposed. Prior to the fault occurrence, HCR-B works under negligible resistance and inductance. Following the fault occurrence, fault current will be broken into three stages as follows: limiting fault current's rate of rise, decreasing magnitude of the fault current and fault current breaking. This topology significantly improves the operational time and decreases the dissipated energy.

The rest of the paper is organised as follows. Section 2 presents HCR-B configuration. In Section 3, analytical studies are given in all of HCR-B operation modes. In Section 4, operational and control strategy are discussed. Simulation results are reported in Section 5, and in Section 6 an experimental prototype is developed to validate the conducted simulations. HCR-B performance and comparison study are presented in Section 7. In the last section, conclusions are summarised.

2 HCR-B configuration

In this section, configuration of the proposed HCR-B is presented. As shown in Fig. 1*a*, L_1 is a series DC reactor that is controlled by the coupled inductor L_2. IGBTs S_1 and S_2 are used to control DC reactor inductance in two-level which in this paper is called controllable reactor switch (CRS).

In addition, R_1 and R_2 are used to damp the stored energy of the reactor in the transient state. D_1–D_4 operate as a full-bridge, and S_3 behaves as a LCS which passes line current as a bidirectional switch. An ultra-fast disconnector (UFD) is connected in series with LCS to isolate the switch while LCS opens. On the other hand, switches S_5, S_6 and diodes D_5, D_6 are used to make the main breaker (MB) that is made by series connection of modular high voltage switches. A surge arrester is used to provide counter DC voltage under the DC load/fault current at the instant of interruption. Moreover, a residual breaker is placed to interrupt the surge arrester leakage current after the fault breakage.

The proposed HCR-B that is connected in series with HVDC line which is depicted in Fig. 1*b*.

In Fig. 1*b*, a point-to-point HVDC transmission system is depicted where two HCR-Bs are installed in the sending and receiving ends of the line.

The HCR-B operates in two operation modes. The first one is normal operation mode and the second one is the fault mode. In each mode, HCR-B circuit is modelled by its equivalent circuit.

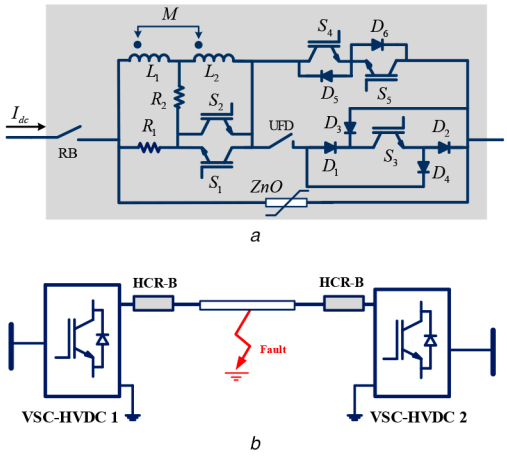

Fig. 1 *HCR-B configuration and placement*
(a) Proposed HCR-B,
(b) HCR-B placed in the HVDC line

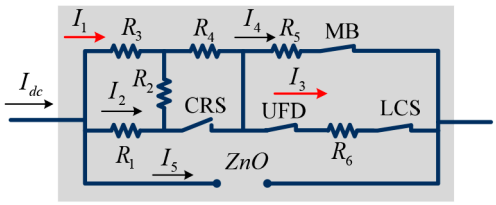

Fig. 2 *Equivalent circuit of HCR-B in the steady state*

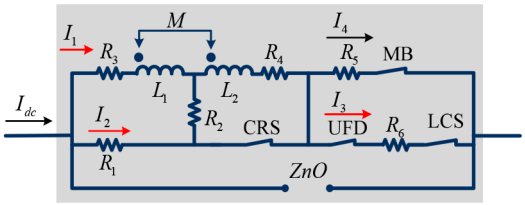

Fig. 3 *HCR-B equivalent circuit in DC system dynamic mode*

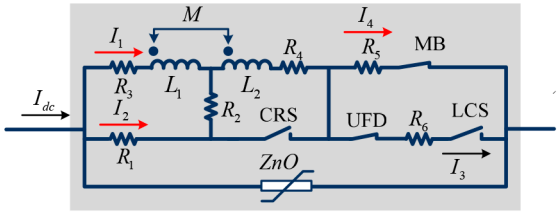

Fig. 4 *HCR-B equivalent circuit in the breaking state*

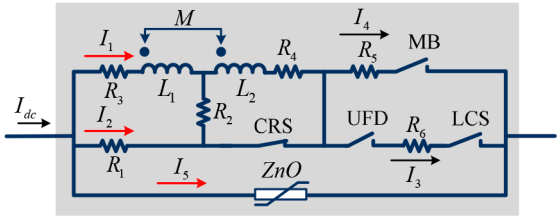

Fig. 5 *Equivalent circuit of HCR-B in the breaking state*

2.1 Normal operation (steady-state)

In the normal operation mode (steady-state), inductors L_1 and L_2 have no inductive effect and behave as just very low resistances. On the other hand, the main current path is determined by on-state resistances of the switches. Equivalent circuit of the breaker is presented in Fig. 2. Values of parallel resistors can be compared as follows:

$$R_1 + R_2 \gg R_3 \text{ and } R_5 \gg R_6$$

Accordingly, most of the line current is conducted by the first and second inductors, L_1 and L_2, UFD and LCS. In addition, controlling switch CRS is turned off.

2.2 Normal operation mode (system dynamic)

In the dynamic mode, inductors L_1 and L_2 effect appears in consequence of the current variations. To bypass the controlled reactor, CRS closes L_1 and current passing through R_2 results in a reverse flux in the controlled reactor core. Therefore, its inductance considerably decreases. Consequently, voltage drop of the controlled reactor in dynamic state is very low and similar to the steady-state condition line current passes through the coupled reactor L_1 and L_2, UFD and LCS. Equivalent circuit of HCR-B is given in Fig. 3.

2.3 Fault mode (pre-breaking state)

In this operation mode, fault took placed. In the first stage, to limit the line fault current, CRS is turned-off to open circuit of L_2 as a controlling coupled inductor. Due to this operation, fault current is limited through L_1 inductance. In the second stage, by turning-off LCS faulty current conducts through the MB. Therefore, limited fault current passes through R_1, coupled limiter reactor $L_1 + L_2$ and the MB. Equivalent circuit of this operation mode is shown in Fig. 4.

2.4 Fault mode (fault current breaking state)

In the third mode, LCS disconnects from the DC line by operation of UFD. This operation mode provides LCS safety by insolating this switch from line voltage. In this time, MB opens the line current and CRS closes circuit of L_2 to bypass the controllable reactor at the same time. This operation decreases the dissipated energy of the MB. On the other hand, R_1 dissipates remaining stored energy of the controllable reactor. Moreover, increasing MB voltage stress causes surge arrester to suppress over voltage and dissipate the DC system stored energy.

3 Analytical studies

In this section, analytical studies of HCR-B are carried out in the steady-state, dynamic operation and fault mode (Fig. 5).

In the normal operation mode, breaker power loss is analysed. In addition, value of dissipated energy in the MB operation is presented.

3.1 Steady-state operation mode

In this operation mode, inductors have not impact in the circuit. Therefore, all the equations are resistive and the circuit model can

Table 1 HCR-B switches control logic

	LCS	UFD	CRS	MB
Normal operation (steady-state)	1	1	0	1
Normal operation (dynamics)	1	1	1	1
Fault condition stage 1	0	1	0	1
Fault condition stage 2	0	0	0	1
Fault condition stage 3	0	0	1	0

be presented as Fig. 2. Equation (1) presents circuit breaker voltage drop in the steady-state condition, and (2) introduces breaker power loss

$$V_{\mathrm{HCR-B}} = (R_3 + R_4)I_1 + R_6 I_3 + V_{\mathrm{LCS}} \tag{1}$$

$$P_{\mathrm{loss}} = (R_3 + R_4)I_1^2 + R_6 I_3^2 + I_3 V_{\mathrm{LCS}} \tag{2}$$

$$I_{\mathrm{dc}} = I_1 = I_3 \tag{3}$$

Here, R_3 and R_4 are resistances of the controllable reactor, R_6 is the equivalent resistance of LCS. V_{LCS} is voltage of LCS semiconductor.

3.2 System dynamics

In the dynamic state, CRS does short circuit L_2 and generated reverse flux in the controllable reactor decreases series inductance value. HCR-B voltage drop and power loss are given in (4) and (5), respectively

$$\begin{aligned} v_{\mathrm{HCR-B}}(t) = {} & (N_1 + N_2)\frac{\mathrm{d}(\varphi_1(t) - \varphi_2(t))}{\mathrm{d}t} \\ & + R_3 i_1(t) + R_4(i_3(t) - i_r(t)) + R_6 i_3(t) + V_{\mathrm{LCS}} \end{aligned} \tag{4}$$

$$\begin{aligned} p_{\mathrm{loss}}(t) = {} & R_3 i_1^2(t) + R_4(i_1(t) - i_r(t))^2 \\ & + R_2 i_r^2(t) + R_6 I_3^2 + I_3 V_{\mathrm{LCS}} \end{aligned} \tag{5}$$

Here, φ_1 is the flux of controllable reactor, and φ_2 is the reverse flux generated by the operation of CRS and i_r is CRS current.

3.3 Per-breaking state

In the per-breaking state, CRS is open and limiter reactor is connected in series with the DC line. In addition, LCS is open. Equivalent circuit is shown in Fig. 4. In this state, there are two current paths as presented in (6). Therefore, two equivalent resistances and inductances can be calculated as (8), (9), (11) and (12)

$$i_{\mathrm{dc}}(t) = i_1(t) + i_2(t) = i_4(t) \tag{6}$$

$$i_1(t) = I_{\mathrm{dc}}(t_0) + \frac{V_{\mathrm{dc}}}{R_{\mathrm{eq1}}}\left(1 - \mathrm{e}^{-(R_{\mathrm{eq1}}/L_{\mathrm{eq1}})t}\right) \tag{7}$$

$$R_{\mathrm{eq1}} = R_{\mathrm{sys}} + R_3 + R_4 + R_5 \tag{8}$$

$$L_{\mathrm{eq1}} = L_{\mathrm{sys}} + L_1 + R_2 + 2M \tag{9}$$

$$i_1(t) = I_{\mathrm{dc}}(t_0) + \frac{V_{\mathrm{dc}}}{R_{\mathrm{eq2}}}\left(1 - e^{-(R_{\mathrm{eq2}}/L_{\mathrm{eq2}})t}\right) \tag{10}$$

$$R_{\mathrm{eq1}} = R_{\mathrm{sys}} + R_1 + R_2 + R_5 \tag{11}$$

$$L_{\mathrm{eq1}} = L_{\mathrm{sys}} + L_2 + M \tag{12}$$

Here, $I_{\mathrm{dc}}(t_0)$ is the initial line current in the fault inception. V_{dc} is the nominal value of DC line voltage. R_{sys} is equivalent resistance of the DC system. M is the mutual inductance between L_1 and L_2.

3.4 Breaking mode

In this state, the MB opens the line fault current and system stored energy dissipates by the surge arrester. Current of the surge arrester is calculated by (13) assuming its non-linear behaviour that is depending on its voltage. Dissipated energy in the surge arrester can be calculated by (14)

$$i_5 = \frac{v_{\mathrm{HCR-B}}(t)}{R_{(V)}} \tag{13}$$

$$P_D = \int_{t3}^{t4} \frac{(v_{\mathrm{HCR-B}}(t))^2}{R_{(V)}}\mathrm{d}t \tag{14}$$

Here, i_5 is the arrester current, $R_{(V)}$ is arrester resistance which is a function of the HCR-B voltage drop and P_D is the arrester dissipated energy. Arrester time period of operation is from t_3 to t_4.

4 Operational and control strategy

In each HCR-B operation mode, a fixed controlling pattern is used. In the normal operation mode (steady-state) all the switches except CRS are closed. In the dynamic state, by turning-on the CRS, impact of series reactor inductance decreases. After fault occurrence at t_0, current and voltage sensors measure DC line signals to prepare a command for HCR-B operation, and after a delay at t_1, LCS and CRS turns off. After 2 ms at t_2, UFD isolates LCS and the MB will be ready to cut the line current. In t_4, again CRS closes to bypass again the series reactor. Summary of the switches control logic is presented in Table 1

5 Simulations of the proposed HCR-B

In this section, operation of the proposed HCR-B is simulated to evaluate its performance. In this simulation, two HCR-Bs are installed in the HVDC line sending and receiving end. Line-to-ground fault is occurred in the HVDC line. Simulated system is shown in Fig. 1*b*. Data of circuit breaker and configured system is presented in Table 2.

In the simulated system, fault is occurred at $t_1 = 2$ ms. Fig. 6*a* shows the line current considering the normal operation and fault condition by applying the proposed HCR-B. At $t_2 = 2.3$ ms, system experiences the peak of fault current that its magnitude reaches ~2.4 kA. In this time, by opening of CRS and LCS, limiter reactor limits the fault current and line current conducted by the MB, respectively.

Therefore, line current experiences its minimum 0.9 kA at $t_2 =$ 3 ms and again increases to a small peak 1.2 kA at $t_3 = 4$ ms. At the same time, MB operates to open line fault current. Line current reaches zero with steady falling from $t_3 = 4$ ms till $t_4 = 7$ ms.

Fig. 6*b* presents the MB voltage while at $t_3 = 4$ ms by opening the MB its voltage decreases to ~450 kV and after 4 ms its voltage reaches the grid nominal voltage.

Fig. 6*d* shows voltage stress of CRS. At $t_1 = 2.3$ ms, CRS experiences its maximum voltage that is close to 48 kV and after the MB operation voltage of CRS falls to −20 kV and finally by turning-on the CRS its voltage fixes in zero.

6 Experimental laboratory results

In this section, to validate the simulation results, a scaled-down experimental prototype is developed and tested. The measurements

Table 2 Simulated DC system and HCR-B parameters

Parameter	Description	Value
L_1	reactor primary inductance	0.2 H
L_2	reactor secondary inductance	0.02 H
R_1	reactor damping resistor	100 Ω
R_2	reactor bypassing resistor	0.1 Ω
R_3	reactor primary resistance	0.04 Ω
R_4	reactor secondary resistance	0.01 Ω
R_5	modelled resistor of the MB	0.3 Ω
R_6	modelled resistor of LCS	0.04 Ω
V_{DC}	voltage of DC system	200 kV
L_{line}	line π model series inductance	0.05 H
C_{line}	line π model shunt capacitance	0.6 μF
P_{flow}	nominal DC line power flow	10 MW
R_{fault}	fault resistance	0.01 Ω
V	DC system voltage	400 kV
I_{dc}	DC line current	2 kA

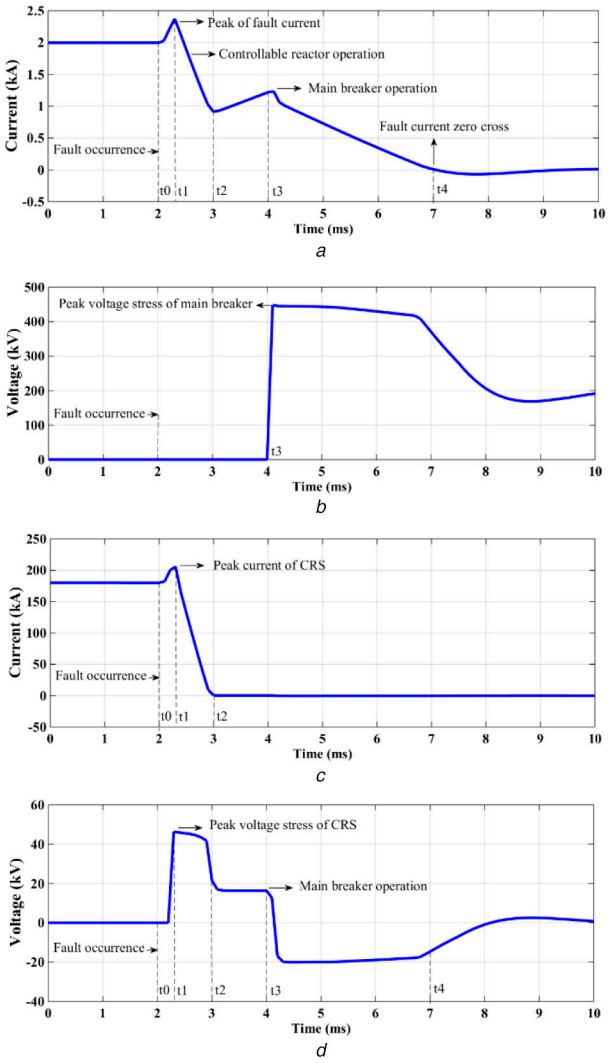

Fig. 6 *HCR-B simulation results*
(a) DC line normal and fault current,
(b) Voltage stress of the MB,
(c) CRS normal and fault current,
(d) Voltage stress of CRS

are DC line current and voltage of the MB. Nominal voltage and current of the prototype are 400 V and 10 A. Breaker is installed between a VSC and a DC load, and fault happens between the line and ground in the load side. Laboratory setup is depicted in Fig. 7. Electrical data of the laboratory elements are listed in Table 3.

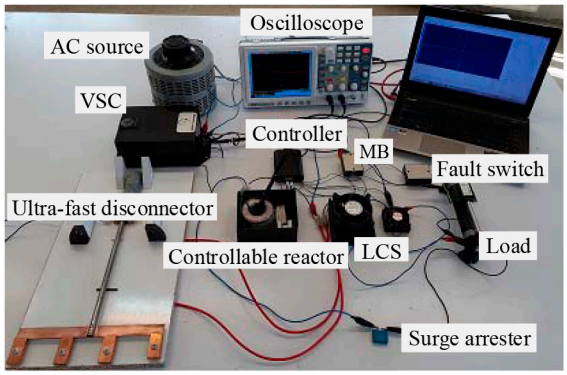

Fig. 7 *Developed laboratory setup*

Table 3 Experimental DC system and HCR-B parameters value

Parameter	Description	Value
L_1	reactor primary inductance	0.2 H
L_2	reactor secondary inductance	0.02 H
R_1	reactor dumping resistor	100 Ω
R_2	bypassing resistor of reactor	0.1 Ω
R_3	reactor primary resistance	0.04 Ω
R_4	reactor secondary resistance	0.01 Ω
R_5	modelled resistor of the MB	0.3 Ω
R_6	modelled resistor of LCS	0.04 Ω
V_{DC}	voltage of DC system	400 V
L_{line}	line π model series inductance	0.05 H
C_{line}	line π model shunt capacitance	0.6 μF
P_{flow}	DC line power flow	500 W
R_{fault}	fault resistance	0.01 Ω

Figs. 8*a* and *b* show DC line current and the MB voltage stress in both normal and fault current breaking states. In the laboratory setup, fault is occurred at t_0 by a solid-state switch. Maximum fault current reaches 28 A and fault current breaks at 3 ms. The maximum experienced over voltage by the MB reaches 425 V that is approximately two times greater than the line DC voltage. These figures confirm the simulation results in Figs. 6*a* and *b*. Figs. 6*c* and *d* present profiles of LCS current and CRS voltage stress, respectively. It is shown that LCS meet 27 A as maximum current. On the other hand, CRS experiences 26 V as the peak value of voltage stress.

7 HCR-B performance and comparison study

In this section, peak value of current and voltage of the main elements of the proposed HCR-B are presented. A summarised electrical data in each working period of HVDC breaker operation is given in Table 4. Considered electrical elements are controllable reactor, CRS, LCS, UFD, MB and surge arrester.

According to the presented data in Table 4, current and voltage limitation for all the elements are our clues to choose semiconductors for HCR-B.

To show advancements of HCR-B, a comparison between common hybrid breaker [17] and HCR-B is presented. This comparison is carried out between the main elements, electrical limitations and number of the required semiconductor switches. In Table 5, important features of HVDC breakers are compared in per-unit data with hybrid breaker. On the other hand, considering the Press Pack IGBT switch specifications [26], the required number for both breakers are given.

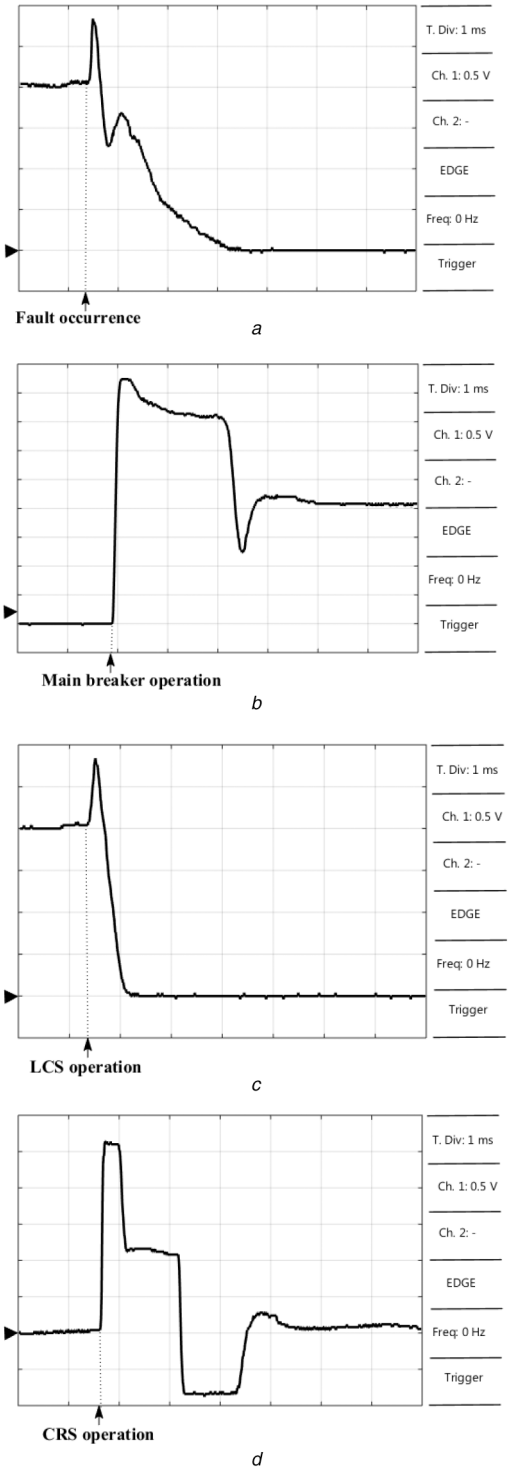

Fig. 8 *HCR-B experimental results*
(a) DC line normal and fault current,
(b) Voltage stress of the MB,
(c) CRS normal and fault current,
(d) Voltage stress of CRS

8 Conclusion

In this paper, a controllable reactor hybrid circuit breaker (HCR-B) for HVDC applications was proposed. This breaker contains a limiter reactor which its inductance can be changed by a controlled solid-sate switch. Performance of the proposed HCR-B is studied by simulations and it is validated by a scaled-down experimental prototype. It is proven that, HCR-B can break DC current successfully and decreases magnitude of the line fault current, recovery voltage of the MB, dissipation energy of the surge arrester and line current rate of raise. It is evident that the number of the required semiconductors considerably decreases.

Table 4 Summery of HCR-B simulation results

Period (t_0–t_2), 1 ms	
peak voltage of CRS	48 kV
peak voltage of L_1	180 kV
peak voltage of LCS	200 V
peak voltage of UFD	0 V
peak voltage of MB	350 V
peak current of CRS	250 A
peak current of L_1	2 kA
peak current of LCS	2.4 kA
peak current of UFD	2.4 kA
peak current of MB	2.4 kA
peak current of surge arrester	0 A

Period (t_2–t_3), 1 ms	
peak voltage of CRS	16 kV
peak voltage of L_1	190 kV
peak voltage of LCS	0 V
peak voltage of UFD	350 V
peak voltage of MB	350 V
peak current of CRS	2 A
peak current of L_1	1 kA
peak current of LCS	0 A
peak current of UFD	0 A
peak current of MB	1.2 kA
peak current of surge arrester	0 A

Period (t_3–t_4), 3 ms	
peak voltage of CRS	−20 kV
peak voltage of L_1	120 kV
peak voltage of LCS	0 V
peak voltage of UFD	450 kV
peak voltage of MB	450 kV
peak current of CRS	0 A
peak current of L_1	1 kA
peak current of LCS	0 A
peak current of UFD	0 A
peak current of MB	0 A
peak current of surge arrester	1.3 kA

Table 5 Comparison of HCR-B performance

Compared data	HCR-B	Hybrid breaker
MB peak voltage	2.5 p.u	2.8 p.u
breaker peak current	1.2 p.u	4.25 p.u
maximum rate of current raising	1500 A/ms	1940 A/ms
arrester dissipation energy	0.63 MW	4 MW
N^o required IGBTs[a] (4.5 kV)	100	125

[a]For 200 kV DC line for equal fault current magnitude.

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