Foreword
Special Issue on Low Temperature Processing of Electronic Materials for Cutting Edge Devices

THERMAL budgets hinder leading edge ultra-scaled and novel designs, and moving to reduced temperature processing is becoming an acute impediment globally.

Early-day electron devices and circuits were typically synthesized of only one, or just a few, materials, so that few thermodynamic constraints were placed upon their processing, essentially temperature and time of specific processes. Through the years, temperature was largely unbounded, so that more perfect crystalline materials with enhanced properties could be exploited.

But now, most devices and circuits have matured to include a myriad of materials and elements on the Periodic Table. So, their coexistence in the same device, or in the same circuit/system, presents severe thermodynamic constraints, principally temperature. This is further exacerbated when devices are scaled below 10nm, and critical features are often below 2nm. At these ultra-scaled dimensions, interactions, even if minute, between dissimilar materials can be deleterious to device performance.

Similar thermal budget limitations are imposed for electronics placed atop flexible substrates, taking this same overarching temperature constraint to large-scale circuits, such as Internet-of-Things (IoT) objects and wearables, presents a further set of inhibiting limitations upon process temperatures in order to accommodate flexible substrates, such as plastics and paper.

This unique special issue does not focus upon one specific material system, or one specific device topology, but instead it aims to bring a wide range of materials and devices under one heterogeneous integration tent that all share in common their unique temperature-constrained processes. In this way, different communities may benefit from the cross pollination of ideas, driven by the same thermodynamic limitations of temperature and time.

Our intent with this special issue was to consolidate the latest advances on the most recent developments and the state-of-the-art in the field of electronic, optoelectronic, and sensor devices based on ultra-low temperature processing. The innovations we desired to capture in this Special Issue are essentially any novel process(s) that pushes the processing temperature lower by 50-100 ºC, or more, than their conventional counterparts.

The Special Issue begins with a review of low temperature process modules (≤500 ºC) planar FDSOI CMOS for 3D heterogeneous integration by Claire Fenouillet-Beranger, CEA-LETI. Daniele Caimi, IBM Research Europe follows with a treatise on heterogeneous integration of III-V materials by direct wafer bonding. Tadeu Mota Frutuoso, CEA-LETI presents RF performance using low temperature sequential integration. Mengze Li, University of Technology Sydney reveals a compact multilayer bandpass filter synthesized by low-temperature additive manufacturing. Robert Hubbard, Lambda Technologies additionally highlights the virtues of low-temperature processing of electronic materials realized by uniform microwave fields. Jae Hur, Georgia Institute of Technology follows with a ferroelectric hafnium zirconium oxide compatible with back-end-of-line processing. And in the flexible electronics community, Avik Sett, IIT Kharagpur realizes a flexible room temperature ammonia gas sensor based upon low-temperature tuning of functional groups in graphene. Similarly themed is Battina Sindhu, Birla Institute of Technology and Science, who shows us a laser-induced graphene printed wearable flexible antenna-based strain sensor for wireless human motion monitoring. Finally, a collaboration between Peide D. Ye, Purdue and Suman Datta, Notre Dame, point to a pathway for back-end-of-line (BEOL) compatible indium-tin-oxide (ITO) transistors with a ferroelectric gate insulator.

The Special Issue meets our goal of providing a consolidation of the latest advancements in low temperature processing for cutting edge devices. The papers also show that ~~this~~ fundamental understanding in integration processes is vital for future electronics ~~and integrations~~. We would like to particularly thank all authors for their timely contributions during these challenging times of Covid-19 pandemic.

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Paul R. Berger (S'84 M'91 SM'97 F'11) is a Professor in Electrical & Computer Engineering at Ohio State University and Physics (by Courtesy). He is also a Distinguished Visiting Professor at Tampere University in Finland. He received the B.S.E. in engineering physics, and the M.S.E. and Ph.D. (1990) in electrical engineering, respectively, all from the University of Michigan, Ann Arbor. Currently, Dr. Berger is actively working on quantum tunneling devices, printable semiconductor devices & circuits for IoT, bioelectronics, novel devices, novel semiconductors and applied physics.

Formerly, he worked at Bell Laboratories, Murray Hill, NJ (1990-'92) and taught at the University of Delaware in Electrical and Computer Engineering (1992-2000). In 1999, Prof. Berger took a sabbatical leave while working first at the Max-Planck Institute for Polymer Research, Mainz, Germany and then moved on to Cambridge Display Technology, Ltd., Cambridge, United Kingdom. In 2008, Prof. Berger spent an extended sabbatical leave at IMEC (Interuniversity Microelectronics Center) in Leuven, Belgium. Prof. Berger was also a Finnish Distinguished Professor (FiDiPro) at Tampere University of Technology (2014-2019), and he continues as a Fulbright-Nokia Distinguished Chair in Information and Communications Technologies (2020-2022) with the newly merged Tampere University.

He has authored over 240 referred publications and presentations with another ~100 plenary, keynote, invited talks, 5 book sections and been issued 25 patents with 3 more pending from 60^{+} disclosures with a Google Scholar H-index of 36. Some notable recognitions for Dr. Berger were an NSF CAREER Award (1996), a DARPA ULTRA Sustained Excellence Award (1998), a Faculty Diversity Excellence Award (2009) and Outstanding Engineering Educator for State of Ohio (2014). He has been on the Program and Advisory Committees of numerous conferences, including the IEDM, DRC, ISDRS, EDTM and IFETC meetings. He will be hosting the IFETC in '21 as General Chair. He currently is the Chair of the Columbus IEEE EDS/Photonics Chapter; Vice Chair of IEEE Columbus (2021-2022) and Faculty Advisor to Ohio State's IEEE Student Chapter. In addition, he is an elected member-at-large to the IEEE EDS Board of Governors (19'-21'), where he is also Vice President of Strategic Directions (20'-21') and a member of the EDS Finance Committee. He is an IEEE EDS Fellow (2011) and Distinguished Lecturer (since 2011), as well as a Senior member of the Optical Society of America.

Muhammad Mustafa Hussain (PhD, ECE, UT Austin, Dec 2005) is a Professor in Electrical Engineering of King Abdullah University of Science and Technology (KAUST). He is also a Visiting Professor of EECS, University of California, Berkeley. Before joining KAUST, he was Program Manager in SEMATECH, Austin. His program was funded by DARPA NEMS, CERA and STEEP programs. A regular panelist of US NSF grants reviewing committees, Dr. Hussain is the Fellow of American Physical Society (APS), Institute of Physics, UK and Institute of Nanotechnology, UK, IEEE Electron Devices Society Distinguished Lecturer, Editor-in-Chief of Applied Nanoscience (Springer-Nature), Editor of IEEE Transactions on Electron Devices, and an IEEE Senior Member. He has authored 300+ research papers, 50+ issued and pending US patents. His students are serving as faculty and researchers in MIT Media Lab, UC Berkeley, Harvard, UCLA, Yale, Purdue, Intel, TSMC, KACST, KFUPM, KAU, and DOW Chemicals. Scientific American has listed his research as one of the Top 10 World Changing Ideas of 2014. Applied Physics Letters selected his paper as one of the Top Feature Articles of 2015. He and his students have received 40 research awards including IEEE Outstanding Individual Achievement Award 2016, Outstanding Young Texas Exes Award 2015 DOW Chemical Sustainability Challenge Award 2012, etc. His research has been highlighted extensively in international media like in Washington Post, Wall Street Journal (WSJ), IEEE Spectrum, etc. His research is focused on futuristic electronics enabled accessible technology for all.

Francesca Iacopi received her MSc in Physics from Roma La Sapienza University, Italy (1996), PhD in E.E./Materials Science from the Katholieke Universiteit Leuven, Belgium (2004), and she is currently Professor of Nanoelectronics, in the Faculty of Engineering and IT of the University of Technology Sydney, and Chief Investigator of the ARC Centre of Excellence in Transformative Meta-Optical Systems (TMOS).

Iacopi over 20 years' R&D experience in semiconductor Industry and Academia, across the fields of CMOS devices, MEMS, interconnects fabrication and advanced packaging. Her research emphasis is in the translation of basic scientific advances in nanomaterials and novel device concepts into industrial processes. Her seminal work at IMEC on low-k dielectrics for on-chip interconnects over the 1999-2009 decade together with Intel, AMD and other partners, has informed the industrial uptake of porous dielectrics into modern semiconductor microprocessors. More recently, she invented a process to obtain graphene on silicon in a site-selective fashion, with applications in integrated micro-technologies from electronics, photonics, to energy storage and (bio)sensing. Major awards include a Gold Graduate Student Award from the Materials Research Society (2003, USA), a Future Fellowship from the Australian Research Council (2012-2016), a Global Innovation Award ("Processes enabling low -cost graphene/silicon carbide MEMS", 2014, Washington DC) and was listed among the 30 most innovative Australian engineers in 2018. Prof. Iacopi is a Fellow of the Institute of Engineers Australia, serves in the Board of Governors of IEEE EDS (2021-23), as well as in various standing technical and award committees for EDS and the Materials Research Society.

Willy Rachmady Ph.D. is a Principal engineer in the Components Research, Technology Development Group, Intel Corporation. Dr. Rachmady has led the development of advanced process modules and novel device integration for Intel's transistor and process technologies. He received his B.S. degree in chemical engineering at Lafayette College (1996) and his Ph.D. in chemical engineering at the Pennsylvania State University (2001). Since joining Intel in 2002, Dr. Rachmady has contributed to the development and implementation of key enabling processes and transistor architectures for many generations of Intel's silicon technologies, including strained Si, High-K/Metal Gate and Trigate. He currently leads the research and development efforts in emerging silicon and non-silicon nanoelectronics devices, 3D process integration, and interconnects. He participated in organizing major international conferences with the latest serving as the short course chair (2017-2018) and the publicity chair (2019-2020) for VLSI Symposia. He also served as an advisory board member to NSF and academic research centers. He has authored over 26 peer-reviewed publications and has been awarded ~~with~~ 198 US patents.

Jörg Schulze studied experimental physics at the TU Braunschweig, Germany. In 2000 he received the Ph.D. degree (Dr.-Ing.) in EE from the EE&IT Faculty of the University of the German Federal Armed Forces Munich. From the same faculty he received in 2004 his post-doctoral degree (Habilitation). He was active as Senior Consultant for Technical Risk Management and as Head of Competence Field "Robust Design Optimization" in Siemens Corporate Technology (2005-2008). Since 2008 he is working at the University of Stuttgart, Germany, as Professor of EE and Head of the Institute of Semiconductor Engineering. His main interest is directed to group-IV-based epitaxy, nano-electronics, photonics & plasmonics, quantum electronics and spintronics.

Huang-Chun Wen, Ph.D. is a Senior Member of the Technical Staff at Texas Instruments, and is currently the process development manager for Technology Transfer and Ramp Support. Dr. Wen received her Ph.D. degree in Electrical and Computer Engineering in 2006 from the University of Texas at Austin, and her B.S. and M.S. from National Chiao Tung University in Taiwan. Before joining TI, she was a researcher at SEMATECH working on advanced CMOS integration. Since joining TI in 2007, she has been the process integration and memory expert, leading the successful development and ramp of multiple new technologies. Her experience covers a breath of domains in the semiconductor industry, from CMOS to memory to bipolar silicon processing, and new packaging and test methodologies. She was the recipient of the 2018 Women of Color in Technology Rising Star Award, and VP for the Chinese Institute of Engineers – DFW chapter. She has authored/co-authored more than 75 journal and conference publications and holds 4 US patents.

Peide Ye is Richard J. and Mary Jo Schwartz Professor of Electrical and Computer Engineering at Purdue University in USA. He received BS from Fudan University, Shanghai, China, in 1988 and Ph.D. from Max-Planck-Institute of Solid State Research, Stuttgart, Germany, in 1996. Before joining Purdue faculty in 2005, he worked for NTT Basic Research Laboratory, NHMFL/Princeton University, and Bell Labs/Lucent Technologies/Agere Systems. His current research work is focused on atomic layer deposition technology and its device integration on novel channel materials including III-V, Ge, 2D materials and complex oxides. He authored and co-authored more than 200 peer reviewed articles and 350 conference presentations including many invited, keynote and plenary talks. He also served as chairmen and program committee members on top international conferences and symposia. He received IBM Faculty Award, Sigma Xi Research Award, and Arden Bement Jr. Award. He is a Fellow of IEEE and APS (American Physical Society).