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A 5-Level HERIC Active-Clamped Inverter With Full Reactive Power Capability for Grid-Connected Applications

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ABSTRACT Distributed generation systems integrated into the modern electrical grid demand novel circuit architectures that can combine high efficiency and high power density together. The transformerless highly efficient and reliable inverter concept (HERIC) topologies are notable due to their mitigated leakage current concerns, constant common-mode voltage, and high efficiency. Nonetheless, the HERIC-based structures feature a maximum of three-level ac output voltage, forcing the conversion system to integrate large output filters to meet the grid codes. This article introduces a novel HERIC active-clamped converter with bidirectional power flow and full reactive power capabilities that can achieve five-level output voltage. This is accomplished by means of a phase-shifted pulsewidth modulation technique that effectively doubles the apparent switching frequency of the inverter and improves the quality of the injected ac power. Consequently, the topology can achieve higher power conversion efficiency, while using the same or a smaller output filter. To verify the feasibility of the proposed converter, a 2.5-kW SiC-based prototype was built and tested in the laboratory under different operation conditions.

INDEX TERMS Highly efficient and reliable inverter concept (HERIC)-clamped inverter, multilevel inverters, power converters, pulsewidth modulation inverters (PWM).

I. INTRODUCTION

Power electronic converters serve various purposes and attract attention due to the increasing number of converter-based generation/load units [1], [2]. Grid-tied energy conversion systems for renewables, motor drives, energy storage, and electric vehicles have been gaining more interest since the latest decade [3], [4], [5]. Some critical factors enabling the efficiency enhancement of a conversion system are improved modulation scheme, reduced voltage and current stress across semiconductors, selective harmonic elimination, and suppression of leakage current caused by high-frequency common-mode voltage (HF-CMV) [6], [7]. That said, transformerless dc-to-ac conversion systems with multilevel output voltage waveform might potentially provide a higher power density and efficiency while reducing the overall cost and size of passive components [8].

Herein, transformerless grid-connected conversion systems have been a popular, efficient, and more power dense solution in recent years, resulting in widespread usage of commercialized versions of newly proposed converters [9]. Conventionally, three-level (3L) inverters with unipolar sinusoidal pulsewidth modulation (PWM) are employed to tackle the constant CMV problem could reduce the number of semiconductor devices, size of passive components, and improve efficiency and total harmonic distortion (THD). With the concept of ac- and dc-decoupling, many H4-based

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transformerless topologies have been introduced. The well-known highly efficient and reliable inverter concept (HERIC) was patented in [10] with an ac-decoupling technique. The original HERIC converter encompasses many benefits, such as high efficiency and reduced leakage current, albeit it can operate with a power factor close to unity. Since many grid codes nowadays require reactive power support capability, this drawback can be an obstacle to modern power grid implementations. To overcome this issue, Freddy et al. [11] proposed a modulation technique where the ac-decoupling circuit operates with both fundamental and switching frequencies. In turn, this approach leads to a wider power factor operating region, but at the cost of higher switching losses. Similarly, the H5 converter with the additional switch for dc-decoupling was proposed by SMA Solar Technology AG [12]. As an extension of the dc-decoupling technique, different variations of the H6-based topologies were originated for further leakage current reduction [13], [14]. However, with the unipolar modulation and decoupling during freewheeling stages, the high-frequency resonance phenomena caused by the junction capacitance of the switches might amplify the leakage current generation. Even with a relatively low leakage current produced by the aforementioned topologies, grid codes, such as VDE-AR-N 4105, IEC 60755, VDE 0100-410, and VDE 0100-721, are not entirely complied since parasitic capacitive circuits generate nonconstant CMV. Additional measures in the design of a suitable electromagnetic interference (EMI)/common-mode filter are required to fully mitigate the leakage current concern [15].

Alternatively, to address the foregoing issue, active- and passive-clamped converter topologies were introduced, i.e., the optimized H5 [16] and full-bridge zero-voltage rectifier [17]. Within this concept, the 3L HERIC active-clamped was presented in [18] and is designed to clamp the mid-point voltage to $+V_{DC}/2$. The 3L HERIC active-clamped topology utilizes the mid-point clamped circuit at the switching frequency, creating a zero output voltage state during both positive and negative half-cycles. Thus, the 3L HERIC active-clamped converter can operate within four quadrants but with less efficiency than the conventional HERIC converter. The charging current of the junction parasitic capacitance in the OFF-state condition of the switches can be significantly reduced, and the HF-CMV is clamped to half of the dc-link voltage. Consequently, this reduces the complexity of designing the output EMI filter and results in a very low leakage current value.

Similar to mid-point clamped topologies, neutral-point-clamped (NPC)-based structures also feature relatively constant CMV since they clamp freewheeling stages to the neutral point. With the increasing number of voltage levels, NPC-based structures can incorporate active and passive components with less voltage ratings. However, NPC-based structures suffer from the half dc-link utilization that dictates higher requirements for dc-sources, active, and passive components.

The other way to fully eliminate the leakage current concern is by utilizing well-known common-ground topologies, i.e., Karschny transformerless inverter [19], dual-buck [20], and switched-capacitor-based structures [21], [22]. However, apart from the negative half-cycle voltage concerns, additional large capacitors or inductors must be integrated into the circuits. Hence, it is still a challenge to attain compact and efficient designs with common-ground structures compared with the aforementioned topologies.

Taking into account the above, there is a high endeavor to reduce the size of the output filter by generating a multilevel voltage at the output [8]. In turn, the reduced output filter size exhibits efficiency/power density improvement while retaining the quality of the injected current. The five-level (5L) flying-capacitor-based topologies achieve all possible voltage levels and constant CMV with 11 power switches [23], and with 12 switches and mid-point clamped structure in [24]. In [25], an H-bridge-based structure with a bidirectional switch for mid-point clamping enables an alternating CMV that changes from half to one-quarter and zero of dc-link voltage. The H8-5L converter introduced in [26] can generate a 5L output voltage waveform with eight switches by employing the integrated switched-capacitor technique that entails discontinuous current stress on the switches and additional losses. Enhancement of inverter output voltage levels with a reduced leakage current profile is also achievable using NPC- or common-ground-based topologies. However, additional active and passive components are required imposing high power density design challenges. Furthermore, implementing a phase-shifted PWM (PS-PWM) for most of the abovementioned 5L inverter topologies is impossible. As a result, the frequency at the output of the converter is identical to the switching frequency, constraining further reduction of the output filter size.

Given the excellent performance and reduction of the HF-CMV and leakage current of 3L HERIC active-clamped [18], this article proposes a new version of the HERIC-clamped converter to achieve a 5L output voltage waveform. In contrast with the original 3L topology and sinusoidal bipolar modulation scheme, the output voltage levels can be increased via either level-shifted (LS) or PS-PWM techniques. Due to the increased apparent output switching frequency, the output filter size requirements can be significantly reduced. Conduction and switching losses are also drastically lowered compared with the existing 3L version. Therefore, with an identical THD of the injected grid current, the conversion system can achieve a higher efficiency and power density. In addition, the proposed converter can accomplish bidirectional power flow and full reactive power capability, which can cover a wide range of power conversion applications in modern power grids [27]. The main contributions of this article are given as follows.

1) By means of just one additional active semiconductor switch and redundant switching states, a modified 5L HERIC active-clamped converter is able to generate a 5L output voltage waveform. This leads to lower EMI noises, caused by high di/dt and dv/dt, lower filter

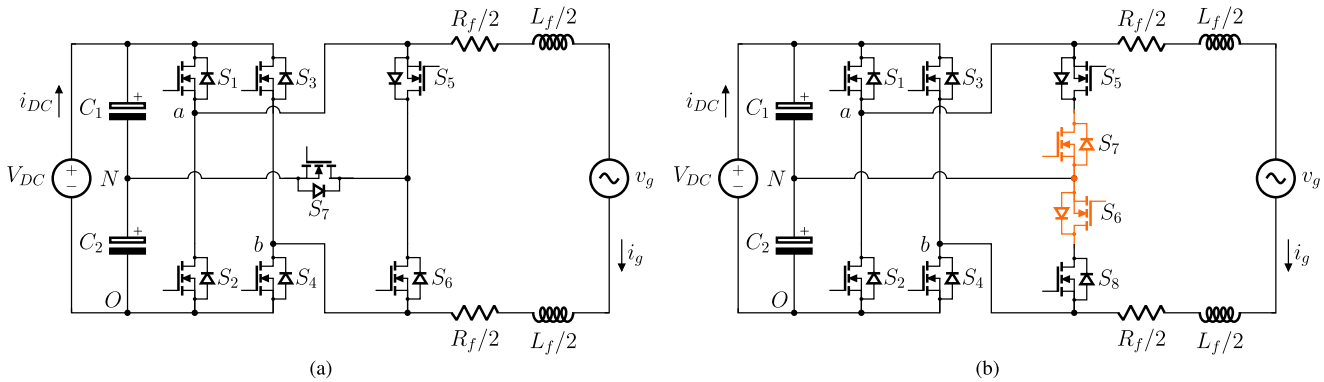


FIGURE 1. HERIC active-clamped inverters. (a) Conventional 3L HERIC active-clamped converter [18] and (b) the proposed 5L HERIC active-clamped converter.

TABLE 1. Switching States of the Proposed 5L HERIC Active-Clamped Inverter

Switching State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	v_{aO}	v_{bO}	v_{out}	v_{CM}	V_{C1}	V_{C2}
A	1	0	0	0	0	1	0	1	$+V_{DC}$	$+V_{DC}/2$	$+V_{DC}/2$	$+3/4V_{DC}$	↓	↑
B	0	0	0	1	1	0	1	0	$+V_{DC}/2$	0	$+V_{DC}/2$	$+1/4V_{DC}$	↑	↓
C	0	0	1	0	1	0	1	0	$+V_{DC}/2$	$+V_{DC}$	$-V_{DC}/2$	$+3/4V_{DC}$	↑	↓
D	0	1	0	0	0	1	0	1	0	$+V_{DC}/2$	$-V_{DC}/2$	$+1/4V_{DC}$	↓	↑
E	1	0	0	1	0	0	0	0	$+V_{DC}$	0	$+V_{DC}$	$+1/2V_{DC}$	—	—
F	0	1	1	0	0	0	0	0	0	$+V_{DC}$	$-V_{DC}$	$+1/2V_{DC}$	—	—
G	0	0	0	0	1	1	1	1	$+V_{DC}/2$	$+V_{DC}/2$	0	$+1/2V_{DC}$	—	—

size, higher power density, more flexibility in choosing a modulation scheme, and, potentially, lower costs for the overall conversion system.

2) With the applied PS-PWM, the proposed topology exhibits higher power conversion efficiency than the original topology, while retaining the same THD level and output filter.

The rest of this article is organized as follows. The circuit description of the proposed HERIC 5L active-clamped is presented in Section II. A grid-connected implementation and working principle of the modulator to attain the 5L output voltage waveform is discussed in Section III. Then, Section IV presents passive component design considerations with loss and efficiency comparisons between the original and proposed topologies. The feasibility of the proposed converter is demonstrated experimentally under grid-tied conditions in Section V. Finally, Section VI concludes this article.

II. PROPOSED 5L HERIC ACTIVE-CLAMPED TOPOLOGY

The well-known 3L HERIC active-clamped converter depicted in Fig. 1(a) utilizes a bidirectional path formed by switches S_5 and S_6 to enable the ac-decoupling approach. That said, the dc-link is divided by two capacitors C_1 and C_2 and separated by the mid-point clamping branch. The additional switch S_7 clamps the CMV to half of the dc-link voltage. With the decoupling approach and a 3L modulation scheme, the clamping scheme $S_5 - S_7$ generates the zero-voltage level at both positive and negative fundamental voltage half-cycles with the unipolar PWM. This mid-point clamping branch opens up a potential for implementation of the so-called, redundant switching states (RSSs). In this regard, to synthesize a 5L output voltage waveform with the original 3L active-clamped topology, one additional switch and S_7 can be placed into the decoupling circuit, as shown in Fig. 1(b). Subsequently, switching pairs S_5, S_7, and S_6, S_8 form two bidirectional switches to fully control the power flow during the RSSs.

Table 1 lists all switching states used to generate a 5L output voltage via the proposed 5L HERIC active-clamped topology. The differential voltage formed between v_{aO} and v_{bO} stands the output voltage of the inverter v_{out}, i.e. $v_{\text{out}} = v_{aO} - v_{bO}$. On the other hand, there are two $+V_{\text{DC}}/2$ and two $-V_{\text{DC}}/2$ switching states for creating half of the dc-link voltage at the output terminals of the inverter during positive and negative half-cycles. The circuit structure allows both LS-PWM and PS-PWM to generate the necessary gate switching pulses. As a result of the PS-PWM multiplicative effect, better THD and reduced output filter size can be achieved. The CMV is formed by the voltage of two terminals of the converter with respect to ground and is defined as $(v_{aO} + v_{bO})/2$. Unlike the original topology, RSSs introduce a variable CMV that ranges between $+V_{\text{DC}}/4$ and $+3V_{\text{DC}}/4$. The frequency of the CMV is half of the apparent frequency of the output voltage v_{out}, which makes the PS-PWM more attractive. Consequently, a smaller common-mode filter can be selected with a higher frequency of the CMV. The converter utilizes the full dc-link voltage. Hence, switches S_1–S_4 block the dc-link voltage (V_{DC}), and the switches in the decoupling circuit (S_5–S_8) block only half of the dc-link voltage.

The 5L HERIC active-clamped converter can demonstrate a degree of fault tolerance. In the event of an open-circuit fault in clamping circuit switches $S_5 - S_8$, the proposed converter can operate as a conventional 3L H-bridge inverter. That said, the converter can also withstand short-circuit faults of switches $S_5 - S_8$ if a fast-acting fuse is employed in the mid-point circuit that connects the dc-link capacitors string and switches $S_5 - S_8$.

III. MODULATION AND CONTROL STRATEGY

To synchronize any generation system, grid-side voltage v_g, power angle $\varphi^\star$, and grid frequency f_g must be determined in advance. For a general grid-feeding converter, the main control objective is to inject the desired value of current i_g. To attain this goal, a proportional–resonant (PR) control is employed in this work, provided its ability to operate with the 2-D stationary reference frame, suitable dynamics at a resonant frequency ω_{RE}, and relatively simple implementation in a digital controller.

To synchronize the converter operation with the grid voltage, phase-locked loops or observers/filters can be used. By assuming a constant grid frequency, a grid voltage observer (GVO) is adopted in this work [28], [29]. In essence, a GVO estimates quadrature $\alpha\beta$-components for the grid voltage, i.e., $\hat{\mathbf{v}}_g(k) = [\hat{v}_{g\alpha}(k), \hat{v}_{g\beta}(k)]^{\text{T}}$, where $v_{g\alpha}$ is the component that is synchronized with the actual grid voltage, v_g. This quadrature grid voltage synchronization allows one to design a sinusoidal current reference that is suitable to be used along with a PR controller, i.e.,:

$$i_g^\star(k+1) = \frac{I_M^\star \hat{v}_{g\alpha}(k+1)}{V_M(k+1)}\cos(\varphi^\star) + \frac{I_M^\star \hat{v}_{g\beta}(k+1)}{V_M(k+1)}\sin(\varphi^\star) \tag{1}$$

where $I_M^\star$ is the desired current amplitude. In addition, the expression (1) can be rewritten in terms of the desired injected/absorbed active and reactive powers. The grid-side voltage amplitude $V_M(k+1)$ is determined as follows:

$$V_M(k+1) = \sqrt{\hat{v}_{g\alpha}^2(k+1) + \hat{v}_{g\beta}^2(k+1)}. \tag{2}$$

The dynamic equation of the injected current in the discrete-time domain can be obtained by utilizing the forward-Euler method for $\text{d}i_g/\text{d}t$. Due to the nature of digital signal processors (DSP), the modulation stage will hold the last value to implement it in the next sampling instant, effectively providing one sample delay. Hence, it is important to highlight that in this work, the controller is designed to compensate for computation delays by using the estimated $(k+1)$ values,

$$i_g(k+1) = \left(1 - \frac{R_f}{L_f}T_s\right) i_g(k) + \frac{T_s}{L_f}\left(v_{\text{out}}(k) - \hat{v}_{g\alpha}(k)\right) \tag{3}$$

where R_f and L_f are the L-type filter equivalent parameters, T_s is the sampling period of the control strategy, $v_{\text{out}}(k)$ stands for the voltage before the filter and is obtained based on the previous sampling instant, and $i_g(k)$ is the measured grid current. Also, it is worth mentioning that the value of grid-side impedance is neglected in the controller design (i.e., stiff grid).

The obtained parameters from (1) and (3) form the tracking error:

$$e(k+1) = i_g^\star(k+1) - i_g(k+1). \tag{4}$$

The error $e(k+1)$ is further led to zero by the PR controller $C_{\text{PR}}(z)$. The reference sine wave signal to modulate the desired output voltage $v_{\text{out}}(k+1)$ is normalized by the dc-side voltage V_{DC} to achieve the control signal $d(k+1) \in [-1, 1]$, i.e.,

$$d(k+1) = \frac{v_{\text{out}}(k+1)}{V_{\text{DC}}}. \tag{5}$$

Then, the control signal $d(k+1)$ determines the actual switching states defined by the modulator presented in Fig. 3(b). The resultant closed-loop system is depicted in Fig. 3(a). As abovementioned, the proposed converter utilizes the PS-PWM scheme to generate a 5L output voltage waveform. The modulation signal v_{mod} is created by means of the instantaneous absolute value of $d(k+1)$. In turn, the switching pulses are created with two high-frequency carrier waves v_{cr1} and v_{cr2} that range within [0, 1] (i.e. $v_{\text{cr},m} = 1$). Referring to Fig. 4, the operation regions of the modulator can be highlighted as follows.

1) *Positive half-cycle:* from 0 to $+V_{\text{DC}}/2$ (Area I *AGBG*).
2) *Positive half-cycle:* from $+V_{\text{DC}}/2$ to $+V_{\text{DC}}$ (Area II *EAEB*).
3) *Negative half-cycle:* from 0 to $-V_{\text{DC}}/2$ (Area III *CGDG*).
4) *Negative half-cycle:* from $-V_{\text{DC}}/2$ to $-V_{\text{DC}}$ (Area IV *FCFD*).

To keep the mid-point voltage balanced, it is necessary to utilize RSSs to generate $\pm V_{\text{DC}}/2$ output voltage levels. From Fig. 3(b), the switching states A and B create $+V_{\text{DC}}/2$, whereas $-V_{\text{DC}}/2$ is generated by C and D. Thereby, the apparent frequency is twice the carrier wave frequency f_{sw}. Alternatively, LS-PWM can also be applied to achieve the desired 5L output voltage. To utilize the LS-PWM, triggers or separators to distinct $\pm V_{\text{DC}}/2$ switching states must be integrated into the modulator, which in turn makes the practical implementation more challenging.

The gate pulses generated by the modulator illustrated in Fig. 4 can synthesize a distinct 5L output voltage waveform (see Fig. 4). It is worth noting that the complimentary transition between states involves charging and discharging of capacitors C_1 and C_2, as presented in Table 1. Moreover, these RSSs generate varying CMV, entailing a relatively higher leakage current. All switching states with illustrated current paths are presented in Fig. 2.

IV. PASSIVE ELEMENTS DESIGN GUIDELINES AND EFFICIENCY ANALYSIS

A. DESIGN CONSIDERATIONS

In the single-phase implementation, the proposed HERIC 5L inverter operates with the dc-link current, i_{DC}, pulsating at

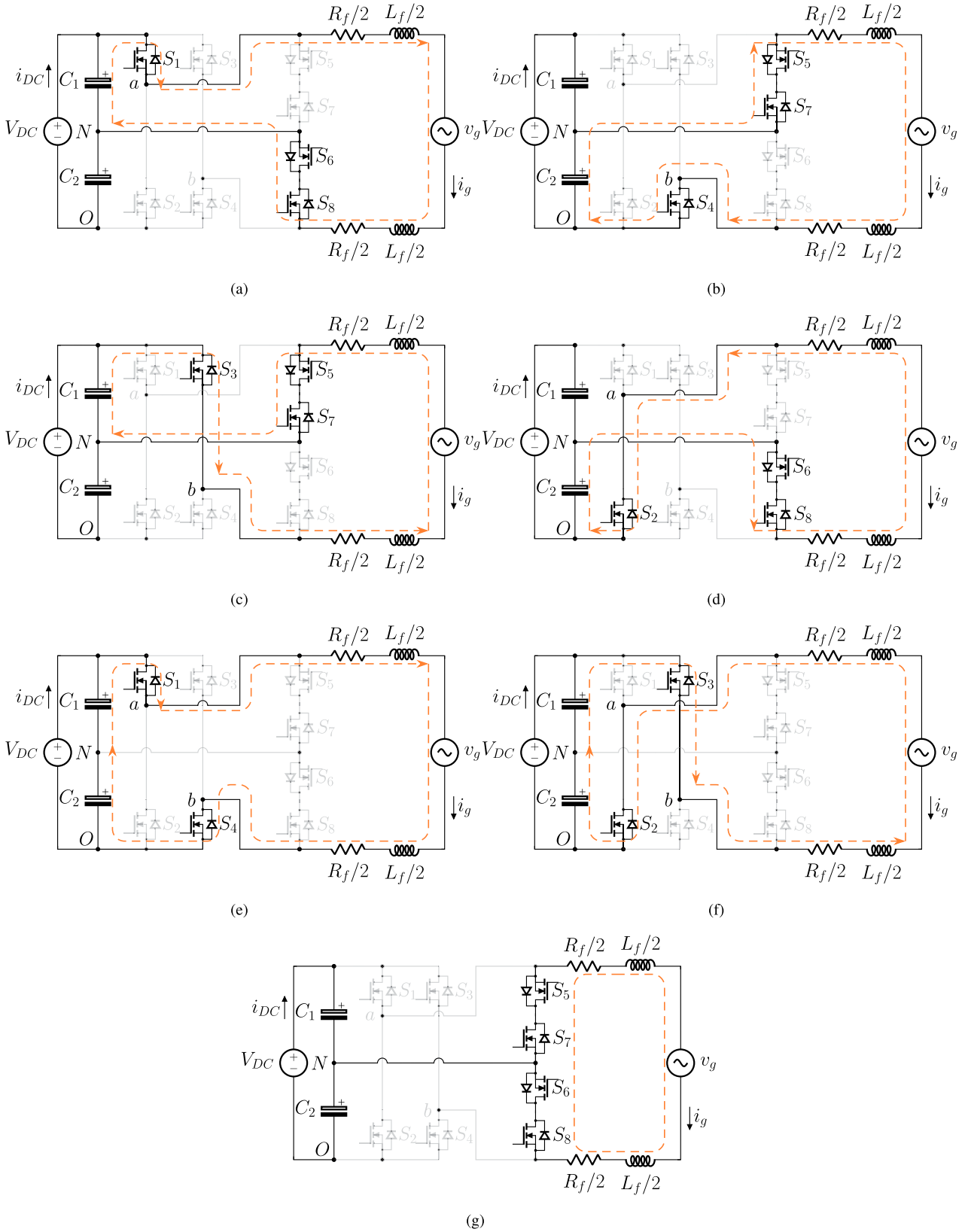


FIGURE 2. Current flowing paths during all modulation states and output voltage levels of the proposed 5L HERIC converter at unity power factor. (a) A: $+V_{DC}/2$, (b) B: $+V_{DC}/2$, (c) C: $-V_{DC}/2$, (d) D: $-V_{DC}/2$, (e) E: $+V_{DC}$, (f) F: $-V_{DC}$, and (g) G: 0.

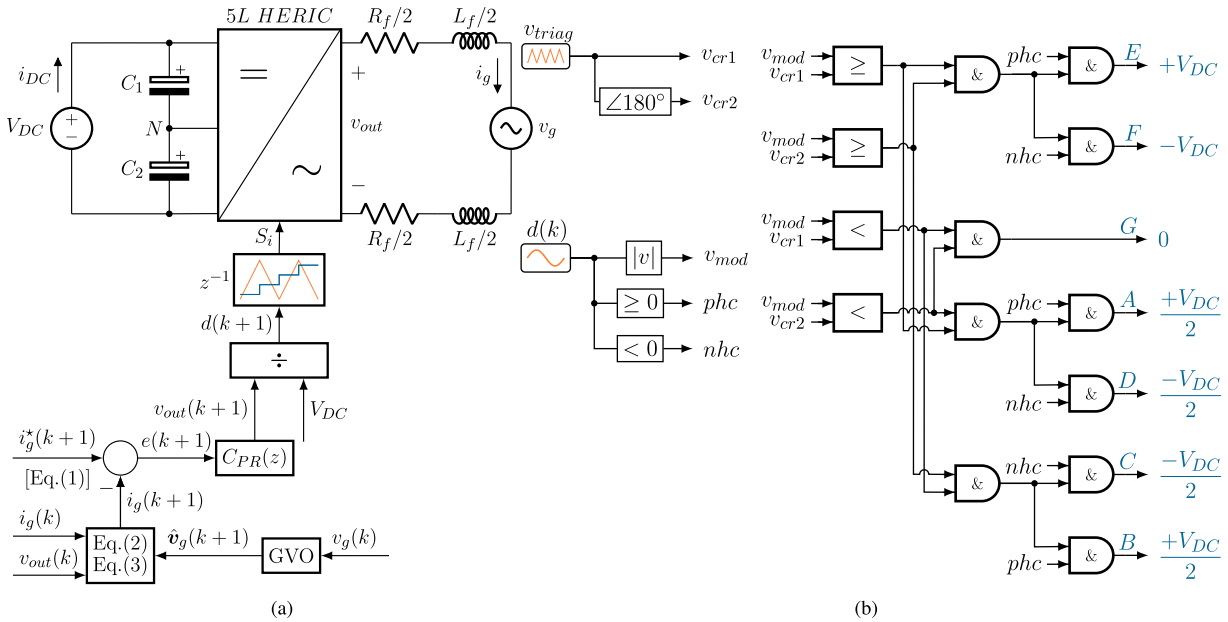


FIGURE 3. Control and modulation of the proposed 5L HERIC active-clamped converter. (a) PR current controller diagram and (b) switching states logic to attain 5L output voltage using two carriers $v_{cr,1}$ and $v_{cr,2}$ with 180° PS.

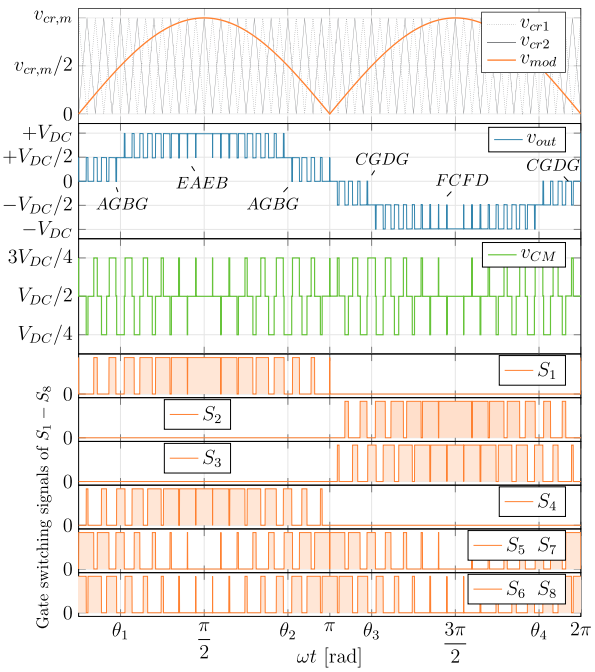


FIGURE 4. Applied low-frequency PS-PWM to the proposed HERIC 5L active-clamped topology within one fundamental voltage cycle.

twice the line frequency. The capacitor string formed by C_1 and C_2 is a passive power decoupling buffer to prevent the HF components from flowing through the input dc-source [24], [30]. Therefore, one way to determine the dc-link capacitor size is based on the required voltage ripples [31]

$$C_1 = C_2 = \frac{V_M I_M}{\omega V_{\rm DC} \Delta V_{\rm DC}} \tag{6}$$

where ω is the angular grid voltage frequency and $\Delta V_{\rm DC}$ is the voltage ripples across the capacitors. That said, I_M stands for the grid current amplitude.

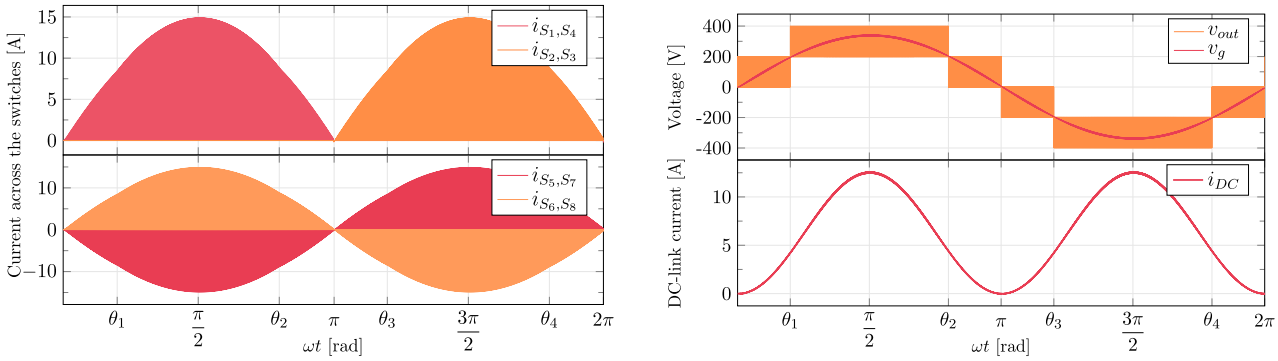
The current ripple of the output filter-inductors is a function of applied volt–seconds within one switching cycle, determined by the apparent frequency, which is twice the switching frequency $f_{\rm sw}$ in case of using PS-PWM in the 5L converter. Taking the abovementioned into consideration, the filter-inductor size is tied to the number of output voltage levels with the relationship $\propto 1/(n-1)^2$ [32], where n represents the number of output voltage levels. On top of that, the employed PS-PWM doubles the effective switching frequency, which results in further reduction of the filter-inductor size. Within one switching cycle, the piecewise approximation leads to the following equation that represents the current ripples across the filter-inductor with the PS-PWM [see Fig. 3(b)]

$$\Delta i_g^{p-p} = \frac{V_{\rm DC}}{(n-1)^2 f_{\rm sw} L_f} = \frac{V_{\rm DC}}{16 f_{\rm sw} L_f} \tag{7}$$

where i_g^{p-p} is the peak-to-peak value of the current flowing through the output inductor L_f.

With the proposed modulation scheme and 5L output voltage, the inverter can employ a filter 4 times smaller than 3L HERIC active-clamped converter modulated by unipolar SPWM and demonstrate the same THD level of the injected current. More importantly, with the smaller filter-inductor size, magnetic and electrical losses will be reduced, which leads to overall efficiency improvement.

Further to the abovementioned, the proposed converter has split-inductors at its terminals. To mitigate the effect of the differential-mode current on the overall leakage current, the output filter is split equally. Provided that the



(a) (b)

FIGURE 5. Simulation results with PLECS software at rated power of 2.5 kW. (a) Current across the switches S_1–S_8, and (b) output voltage v_{out}, voltage after the filter v_g, and dc-link current i_{DC}.

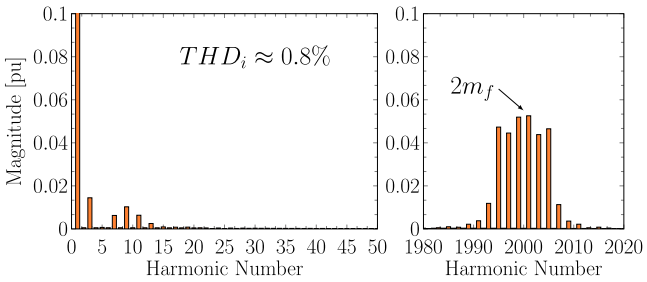


FIGURE 6. Simulated THD of the injected current to the grid at rated power, $f_{sw} = 50$ kHz, and $L_f = 0.6$ mH.

CMV does not remain constant, the converter generates the leakage current i_{CM} that circulates between the ground and parasitic capacitance of the dc-source. In this regard, to meet the grid-code requirements, common-mode chokes should be installed, unless a transformer is utilized.

To verify the performance of the proposed converter, some simulation results are presented in Fig. 5. The applied PS-PWM is synchronized with the modulation signal v_{mod}. Hence, the frequency modulation index can be employed to analyze the THD performance.

$$m_f = \frac{f_{sw}}{f_{mod}}. \tag{8}$$

Being mindful of the multiplicative effect of the PS-PWM, the harmonic distribution lies clusterwise near even frequency modulation indices (see Fig. 6).

B. EFFICIENCY ANALYSIS

An overall efficiency study is undertaken to reflect the changes between the original 3L and the proposed 5L converter topologies. The most convenient and clear criteria for comparison are power quality and efficiency. The conversion system can vary either an output voltage frequency or a filter size to achieve the same quality of the injected current. In this work, the apparent frequency was fixed at 100 kHz. Therefore, the 3L HERIC active-clamped requires to be modulated via a single carrier with $f_{sw}^{3L} = 100$ kHz, whereas the proposed 5L HERIC active-clamped must have two phase-shifted carriers with $f_{sw}^{5L} = 50$ kHz. Being mindful that the ripples across an inductor determine the THD content, the filter size for comparison can be derived from (7). Given the same output voltage frequency, 3L HERIC active-clamped converter must have a filter twice larger than the proposed 5L HERIC active-clamped inverter.

That said, to reach a THD content less than 1% in the injected grid current with the foregoing L-type filter, the 5L HERIC inverter requires $L_f/2 = 0.6$ mH inductors. At the same time, the conventional 3L HERIC should have $L_f/2 = 1.2$ mH inductors. The increase in the filter size entails higher electrical and magnetic losses due to the higher equivalent series resistance (ESR), number of winding turns, and the physical core size. In turn, this will entail larger power losses in the overall conversion system.

The efficiency curves are obtained using PLECS software and can be observed in Fig. 7(a). The thermal model for the power switches is provided by the manufacturer and is assumed the same for both topologies—UJ4C075018K4S. In essence, the efficiency analysis comprises losses in MOSFETs, both conduction and switching losses, and in the output filter. Since the magnetic parameters of inductors are usually not covered by datasheets, they were not included in the overall efficiency analysis. Further to the abovementioned, the ESR of dc-link capacitors is very small at rated switching frequencies and does not affect the efficiency analysis results significantly. The conduction losses of the inductors can be estimated by their ESRs. For the sake of generality, both converters are simulated with the same parameters of dc-link capacitors, input voltage, and injected grid power of 2.5 kW.

The efficiency study and loss distribution findings at the rated power are shown in detail in Fig. 7(b). One can infer from Fig. 7 that the proposed HERIC 5L inverter can attain a higher efficiency than its 3L counterpart with the same THD content. With the increase in the generated output voltage levels, the voltage stress on the semiconductors is lessened, resulting in reduced switching losses. In addition, the use of

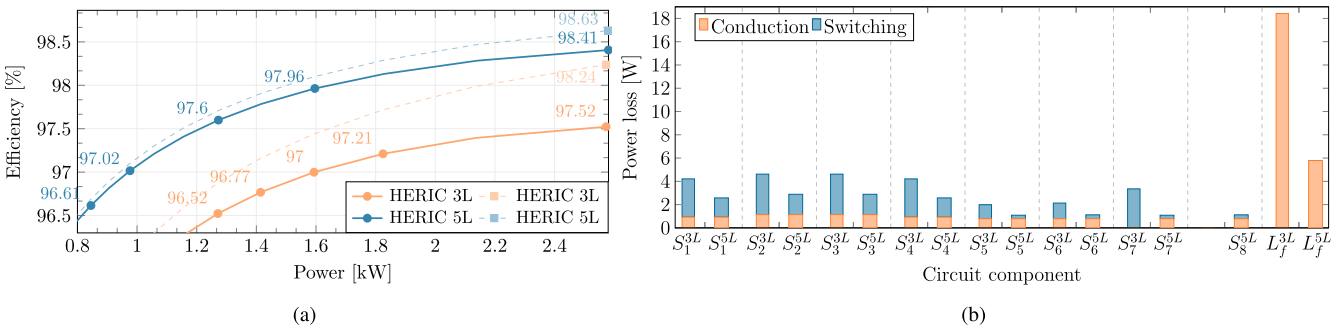


FIGURE 7. **Efficiency and loss breakdown comparison between the proposed 5L HERIC and 3L HERIC active-clamped converters with the same THD level of the injected current, 100 kHz output voltage frequency, and dc-link capacitors. (a) Calculated efficiency curve. Solid line—efficiency of the conversion systems including the output filter; dashed line—efficiency of the converter circuits excluding the output filter. (b) Loss breakdown comparison between HERIC 5L and 3L active-clamped converters. Loss analysis and efficiency calculation are obtained using PLECS software.**

TABLE 2. **Comparative Analysis Between the Proposed 5L HERIC Active-Clamped Converter and Other Existing 5L Topologies in a Single-Phase Implementation**

Topology	No. of Components				TSV [pu]/ MVS	Full dc-link voltage utilization	No. of dc sources	Modulation/ Output voltage frequency	Calculated/Reported leakage current [mA]	Calculated/Reported efficiency
	S	D	C	L						
5L NPC	8	6	4	2	$10/0.75V_{DC}$	No	1	LS/f_{sw}	20.8*	97.1%**
5L ANPC	8	0	3	2	$6/0.5V_{DC}$	No	1	PS/$2f_{sw}$	16.1*	97.71%**
5L CHB	8	0	2	2	$4/V_{DC}$	Yes	2	PS/$4f_{sw}$	31.3*	97.47%**
[23]	11	0	3	2	$6/V_{DC}$	Yes	1	PS/$2f_{sw}$	27@1 kW	96.02%@0.8 kW
[24]	12	0	4	2	$6/V_{DC}$	Yes	1	PS/$2f_{sw}$	29.5@1 kW	96.55%@1 kW
[25]	6	2	2	2	$6/V_{DC}$	Yes	1	LS/f_{sw}	17@2 kW	97.8%@0.4 kW
[26]	8	1	2	2	$6.5/V_{DC}$	Yes	1	LS/f_{sw}	11.7@1 kW	96.8%@5 kW***
[33]	12	0	3	2	$8/V_{DC}$	Yes	1	PS/$2f_{sw}$	14.2@1 kW	96.7%@1 kW
[34]	8	2	2	2	$7/V_{DC}$	Yes	1	PS/$2f_{sw}$	41.1@1 kW*	98.34%@1.8 kW***
Proposed	8	0	2	2	$6/V_{DC}$	Yes	1	PS/$2f_{sw}$	36@1.5 kW	96.94%@2.5 kW

*The leakage current is calculated with the switching frequency (50 kHz), output power (2.5 kW), output filter (6.6 mH, 200 mΩ), and the common-mode choke at the output of the converter (2×3.3 mH).

**The efficiency is calculated by using the output filter (6.6 mH, 200 mΩ), dc-link capacitors (0.47 mF), switching frequency (50 kHz), output power (2.5 kW), and thermal model of the switch UJ4C075018K4S. The efficiency analysis includes losses in the converter circuit and the output filter.

***Reported simulated efficiency by the authors of the cited manuscript.

a smaller filter-inductor also reduces the conduction losses. The efficiency improvement paves the way for transformerless grid-tied converters to lower the manufacturing costs for filtering, and cooling systems, allowing for a higher power density of an overall conversion system.

V. COMPARATIVE STUDY

This section is intended to provide a comparative summary with other 5L single-phase converter topologies.

Criteria for comparison are presented in Table 2 and involve the number of active and passive components, total standing voltage (TSV), maximum voltage stress (MVS), dc-link voltage utilization, number of the required dc-sources, attained output voltage frequency with an implemented modulation technique, calculated and reported leakage current, and efficiency. It is worth to highlight that some converters were introduced a long time ago and should be compared with other modern topologies on the basis of state-of-the-art semiconductors and passive components. Therefore, efficiency and leakage current values for some topologies were obtained using simulation.

One can see from Table 2, the proposed topology shares a similar number of active and passive components with the 5L two-cell cascaded H-bridge (CHB) converter. Even though the 5L CHB converter can outperform the proposed topology in terms of the THD content, its main drawback is the requirement of an isolated dc-source per H-bridge cell. Consequently, this complicates the leakage current analysis and CMV modeling [35]. The operation of the 5L CHB converter involves a fluctuating HF-CMV with a pulsating leakage current, which brings additional requirements to the modulation and EMI filter design [36]. Oppositely, PS-PWM applied to the 5L CHB converter can significantly reduce the output filter size requirements.

The 5L NPC converter has a larger number of passive components than the proposed 5L HERIC active-clamped topology and requires an additional control loop to ensure

the voltage balance of the capacitors. That said, a well-known 5L active NPC (ANPC) inverter, which is a modification of the NPC converter, has a floating phase capacitor between the series-connected output switches [37]. Compared with the traditional 5L NPC converter, 5L ANPC allows for higher efficiency due to the switching losses reduction, higher flexibility for applicable modulation techniques, and higher power density since the number of components is drastically reduced. However, both 5L NPC and 5L ANPC converter topologies operate with a dc-source that is at least twice larger than the peak of the required ac voltage. A very attractive advantage of utilizing 5L NPC/ANPC converters is a low value of generated leakage current that results from a constant CMV.

The proposed topologies in [23], [24], [33] are designed for the solar industry applications and can successfully deal with an HF-CMV by making it almost constant throughout all fundamental voltage cycles. These attain a 5L output voltage waveform by employing floating capacitors and can reduce a leakage current generated by the conversion system. The latter merit is achieved by means of additional passive and active components that make an impact on the converter efficiency. The 5L output voltage waveform can be generated via integrating SC-based circuits. In [26], the SC technique entails large and discontinuous currents tied to the charging processes of the capacitors. In turn, this leads to higher currents flowing through the semiconductors and ESRs of passive components, which effectively reduces the efficiency of the conversion system. On the other hand, this process precedes the capacitor voltage ripples that can significantly distort the quality of the output voltage waveform unless very large capacitors are employed. Even though the converter topology proposed in [26] can mitigate the leakage current concern, both high power density and efficiency would be challenging to attain simultaneously. On top of that, the semiconductors must have enough capacity to handle the charging currents of the capacitors. The T-type circuit configuration presented in [25] employs RSSs to generate the 5L output voltage waveform, in which the resultant CMV has both high-frequency and low-frequency components that are accompanied by current spikes, when the CMV reaches zero voltage. Due to the low-frequency components in the resultant CMV, additional requirements to active or passive filters would be applied to further attenuate the CMV. A recently presented 5L HERIC passive-clamped converter in [34] is a modification of the 3L HERIC passive-clamped from [18]. As opposed to the proposed converter topology, 5L HERIC passive-clamped converter operates with a higher number of semiconductor devices and TSV. Moreover, diodes in the clamping circuit limit the power factor operating area, which restricts the potential applications of the converter.

The resultant experimental efficiency of the proposed converter is 96.94% at the rated power of 2.5 kW, as shown in Fig. 14. The efficiency analysis for the proposed topology involves energy dissipation in semiconductor devices and the output filter and is measured with respect to the dc- and grid-sides. Since MOSFETs used in the converter are overrated

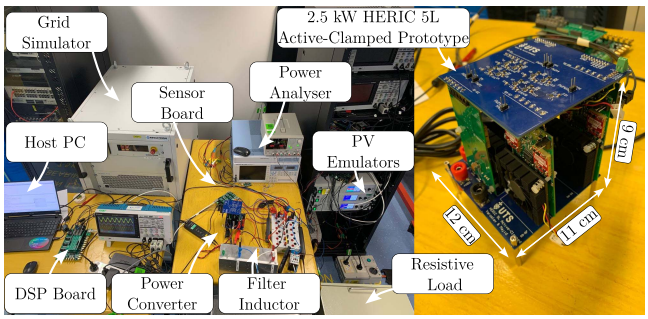


FIGURE 8. 2.5-kW prototype of HERIC 5L active-clamped converter with the measurement and grid-connection setup.

TABLE 3. List of Parameters for the Measurements

Description	Value/Type
Power Rating (P_R)	2.5 kW
Carrier Frequency (f_{sw})	50 kHz
Line frequency (f_l)	50 Hz
Dc-link Voltage (V_{DC})	360 V
Dc-link Capacitors ($C_{1,2}$)	0.47 mF
Filter Inductor (L_f)	6.6 mH, 200 mΩ
Power MOSFETs	UJ4C075018K4S
Gate Drivers	UCC21520DW
DSP	TMS320F28379D

for this power output, the efficiency curves do not reach the peak values at the rated power. Although the proposed topology exhibits the largest leakage current among the converters under comparison, it should be highlighted that this value is achieved at higher power than that of competitors. The industrial implementation of almost all power electronic converter topologies will require EMI filters, e.g., common-mode filters, in order to limit the leakage current and comply with the safety and EMC standards [6], [7], [18], [25]. Therefore, additional filtering can be implemented to further attenuate the leakage current generated by the converter.

VI. EXPERIMENTAL RESULTS

In this section, some laboratory-based experimental results are presented in order to evaluate the efficacy and circuit practicality of the proposed 5L HERIC active-clamped inverter in generating a distinct 5L output voltage waveform. A silicon carbide (SiC)-based prototype has been built with the parameters enlisted in Table 3. To test the system under grid-tied conditions, a grid simulator (REGATRON TC30.528.43-ACS) has been employed, which can operate in four quadrants. PV emulators (EA-PSI-9750-12) as a dc-source have been used. The resultant setup can be observed in Fig. 8.

The closed-loop system utilized for the grid-connection has been discussed in detail in Section III. The methodology whereby the PR controller was tuned and implemented is discussed in [38]. To minimize the effect of HF-CMV and decrease the leakage current, a common-mode choke is used after the main L-filter. The amplitude of the grid voltage is

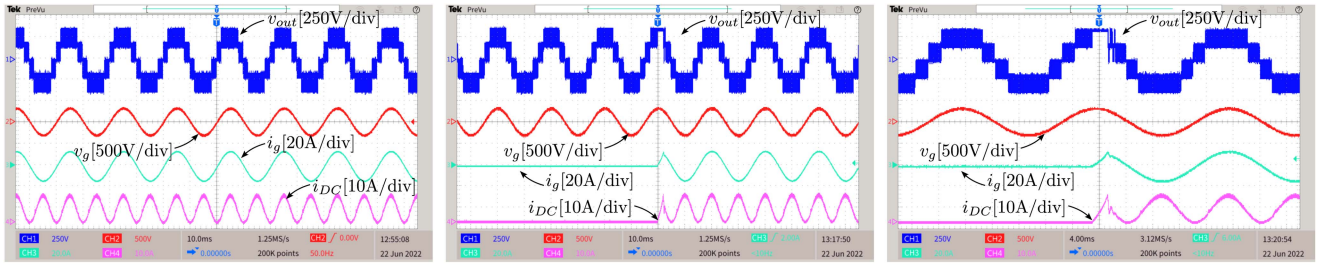


FIGURE 9. Experimental results of the proposed 5L active HERIC converter at the grid-connected conditions. From top to bottom: Inverter output voltage v_{out} (blue), grid-side voltage v_g (red), grid-side current i_g (aquamarine), and dc-side current i_{DC} (purple). (a) Rated operation conditions at 2.5 kW power. (b) Converter operation under an active power step change from 0 to 2.5 kW. (c) Zoomed results of (b).

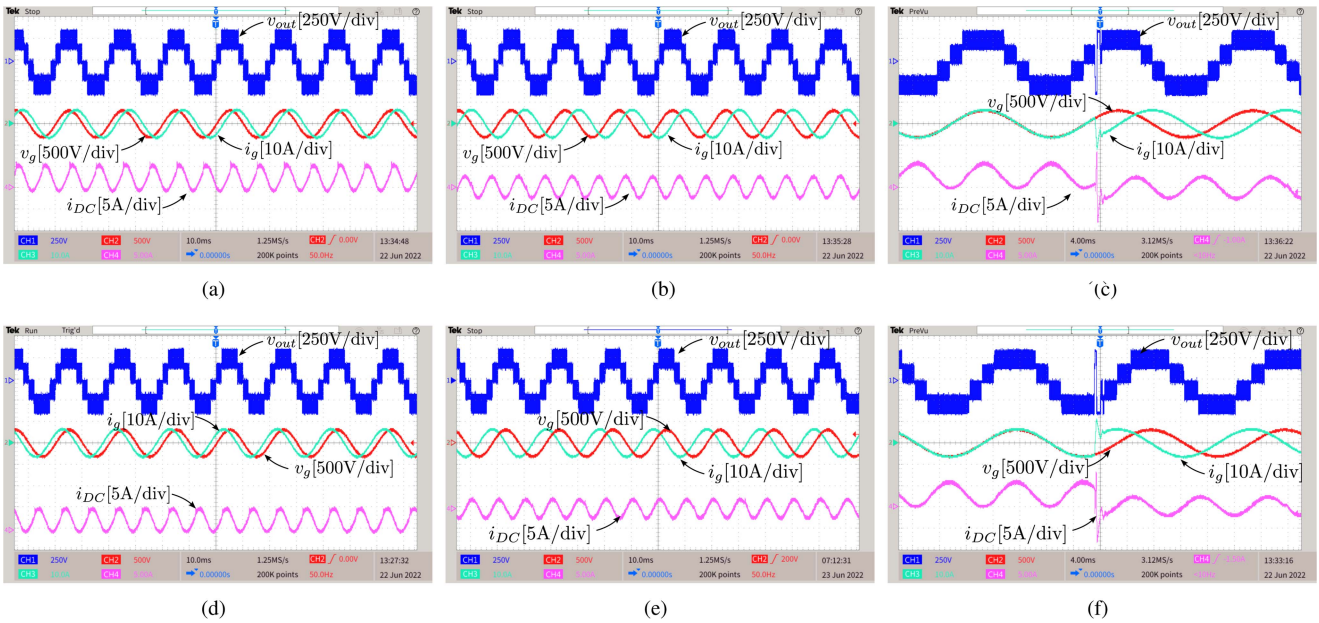


FIGURE 10. Experimental waveforms of the converter at reactive power capability tests, $S = 1$ kVA. From top to bottom: Inverter output voltage v_{out} (blue), grid-side voltage v_g (red), grid-side current i_g (aquamarine), and dc-side current i_{DC} (purple). (a) Lagging power factor of 0.707 ($\varphi^\star = -45°$). (b) Purely lagging power factor ($\varphi^\star = -90°$). (c) Dynamic change of power factor from unity to purely lagging. (d) Leading power factor of 0.707 ($\varphi^\star = 45°$). (e) Purely leading power factor ($\varphi^\star = 90°$). (f) Dynamic change of power factor from unity to purely leading.

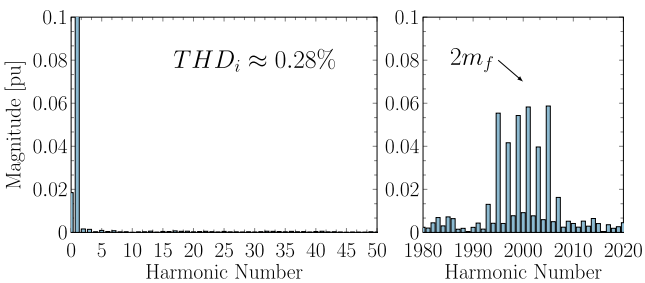
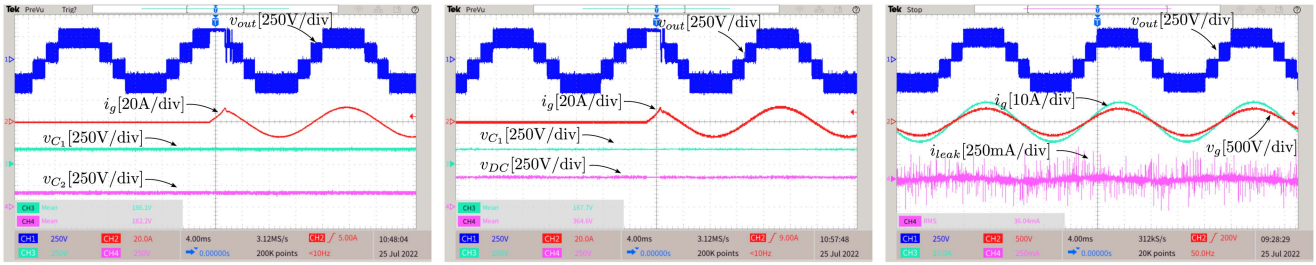


FIGURE 11. Experimental harmonic performance of the injected current to the grid at rated power of 2.5 kW.

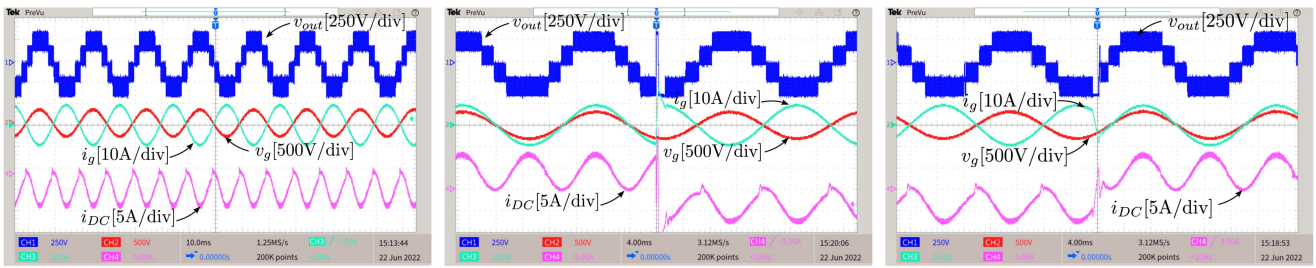
set at 311 V with the line frequency of 50 Hz. Hence, with the sufficient dc-link voltage of 360 V, the modulation index can be fully scaled. The resulting waveforms of the proposed converter under 2.5-kW test conditions can be observed in Fig. 9(a). The performance of the converter during a step change in the grid current reference is illustrated in Fig. 9(b) and (c). From Fig. 9(c), it is evident that the PR controller can track the reference, indicating the proper parameters tuning and overall closed-loop system response. It is worth mentioning that the step change results were obtained when the grid voltage was at its peak to verify the dynamic performance of the PR controller.

As for the reactive power capability tests, the inverter was tested under various power factors at an apparent power of 1 kVA [see Fig. 10(a), (b), (d), and (e)]. Herein, one can infer that the proposed inverter has full reactive power capabilities operating with purely lagging [see Fig. 10(b)] and purely leading power factors [see Fig. 10(e)]. Power factor step change results are presented in Fig. 10(c) and (f). As a consequence, with the grid-supporting control scheme, the



(a) (b) (c)

FIGURE 12. Experimental results of capacitors voltage balancing capability during active power step change from 0 to 2.5 kW and the generated leakage current at 1.2 kW steady-state output power. From top to bottom: Inverter output voltage v_{out} (blue), grid-side current i_g (red), voltage of the capacitor C_1 v_{C1} (aquamarine), and voltage of the capacitor C_2 v_{C2}/ dc-link voltage v_{DC} (purple). (a) Active power step change from 0 to 2.5 kW. (b) Active power step change from 0 to 2.5 kW. (c) Steady-state operation of the converter at the power of 1.5 kW: inverter output voltage v_{out} (blue), grid-side voltage v_g (red), grid-side current i_g (aquamarine), and leakage current i_{leak} (purple).



(a) (b) (c)

FIGURE 13. Experimental results of the converter's bidirectional power flow capabilities. From top to bottom: Inverter output voltage v_{out} (blue), grid-side voltage v_g (red), grid-side current i_g (aquamarine), and dc-side current i_{DC} (purple). (a) Steady-state operation at −1.2 kW active power. (b) Active power step change from 1.2 to −1.2 kW. (c) Active power step change from −1.2 to 1.2 kW.

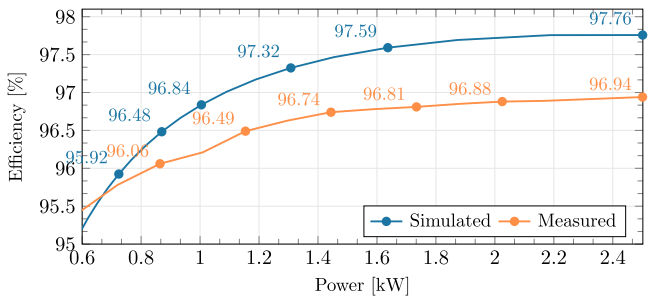


FIGURE 14. Measured and simulated efficiency curves of the proposed converter. The simulated efficiency results are obtained on the basis of the parameters listed in Table 3 and include power losses in semiconductors and the output filter.

proposed inverter can participate in voltage regulation and reactive power support. At nominal power, the converter has a THD of ≈ 0.28% in the injected grid current, with harmonic clusters located near frequencies of $2m_f$, see Fig. 11.

Before the grid-connected operation, capacitors C_1 and C_2 are equally precharged to $v_{DC}/2$. Given a distinct 5L output voltage waveform during steady-state conditions, it can be inferred that the mid-point voltage is maintained constant and equal to $v_{DC}/2$. To evaluate the mid-point voltage behavior during transients, experiments with active power step change were conducted [see Fig. 12(a) and (b)]. As the experimental results show, the converter is capable of keeping the voltage across the capacitors equal to $v_{C_1} = v_{C_2} = v_{DC}/2$, during transient and steady-state operating conditions. Additional tests were performed to determine the leakage current generated by the conversion system. From Fig. 12(c), with the presence of a common-mode choke after the main output filter, the resultant rms value of the leakage current is 36 mA at 1.5 kW active power output and $v_g^{p-p} = 311$ V.

Fig. 13(a)–(c) demonstrates the bidirectional power flow capability of the converter. The PV emulators are connected in parallel with the passive load to absorb the active power from the grid emulator (see Fig. 8). The steady-state condition during negative power flow is illustrated in Fig. 13(a). A power flow inversion from positive to negative was performed at the peak of the grid voltage within 3 ms, as shown in Fig. 13(b). Alternatively, the additional test was conducted where a step power change from −1.2 to 1.2 kW is applied [see Fig. 13(c)]. The test was performed when the grid voltage was near its peak. The converter could change the direction of the injected current within 4 ms.

The efficiency curve is obtained via the power analyzer Yokogawa WT1806E, connected to the input (dc-side) and output of the conversion system (grid-side), including the output filter and the common-mode choke. From Fig. 14, the conversion system attains 96.94% efficiency at the rated power of 2.5 kW. However, since the converter operates with overrated MOSFETs, the efficiency peak is not attained.

VII. CONCLUSION

The 3L active-clamped HERIC topology is an attractive solution for transformerless applications due to its desirable features such as relatively constant CMV, reduced leakage current, and high efficiency. However, the overall power efficiency and power density can still be improved by utilizing the multilevel output voltage concept. In this regard, this article proposed a version of the HERIC converter that can generate a 5L output voltage waveform by adding only one additional switch. As a consequence, with the same THD profile, the converter can demonstrate a higher efficiency and power density by integrating a smaller output filter-inductor. With the improved 5L HERIC active-clamped converter, PS-PWM can be applied to attain a better THD profile and reduce the output filter requirements. Even though the HF-CMV concerns persist with the proposed topology, a common-mode filter can be integrated into the conversion system to attenuate the leakage current to achieve acceptable values. A 2.5-kW SiC-based converter prototype was built in the laboratory and tested under different conditions to justify the feasibility and efficacy of the proposal.

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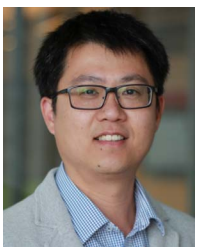

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