Advanced Power Control System For Enhancing Second-Life Battery Energy Storage Systems Integration and Reliability

by **Pablo Poblete**

Thesis submitted to the University of Technology Sydney (UTS) in partial fulfillment of the requirements for the Degree of Doctor of Philosophy

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Certificate of Authorship / Originality

I, Pablo Poblete, declare that this thesis is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the School of Electrical and Data Engineering at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

I certify that the work in this thesis has not previously been submitted for a degree nor has it been submitted as part of the requirements for a degree at any other academic institution except as fully acknowledged within the text. This thesis is the result of a Collaborative Doctoral Research Degree program with Pontificia Universidad Católica de Chile.

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To my family and especially to my wife Valentina.

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Abstract

Electric power grids are rapidly transforming due to the increasing integration of variable renewable energy sources (RES), distributed generation, and new loads associated with electric vehicle (EV) charging stations. These changes bring several technical challenges related to grid stability and integrity, increasing the operational complexity of future grids.

One of the most promising solutions to mitigate some of the issues related to RES is using battery energy storage systems (BESS). BESS can absorb active power when there is a surplus of RES power generation and output this power when it is most convenient. Moreover, BESS can also operate as an energy backup and provide ancillary services to the grid, increasing the power system flexibility. However, the high investment costs of Lithium-ion batteries impose a relevant cost barrier to the widespread adoption of this technology.

Intending to provide a new energy storage alternative that can accelerate the transition towards RES, this thesis presents a novel Cascaded H-Bridge (CHB) converter control and modulation strategy for the effective integration of second-life BESS (SL-BESS) into the electrical grid. These systems use batteries that have reached the end of their first operational life but still retain sufficient capacity for another use in a less demanding application. In particular, this work gives special attention to optimal modulation techniques, and optimal current and state of charge control strategies for the CHB converter with battery packs directly connected to each H-Bridge sub-module.

Simulation and experimental results are provided to verify the effectiveness of the proposed modulation and control strategies for a three-phase CHB converter-based SL-BESS prototype formed by second-life Lithium-ion battery packs.

Contents

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List of Acronyms

RES	: renewable energy sources.
EV	: electric vehicle.
BESS	: battery energy storage system.
LIB	: Lithium-ion battery.
BP	: battery pack.
SL-BESS	: second-life battery energy storage system.
CHB-BESS	: cascaded H-Brdige based battery energy storage system.
Δ-CHB-BESS	: delta-connected CHB-BESS.
BMS	: battery management system.
EMS	: energy management system.
PCS	: power conversion system.
SoC	: state of charge.
SoH	: state of health.
2L-VSC	: two-level voltage source converter.
CHB	: cascaded H-Bridge.
SM	: sub-module.
PR	: proportional-resonant.
PI	: proportional-integral.
MPC	: model predictive control.
DS-MPC	: dual-stage model predictive control.
QP	: quadratic program.
KF	: kalman filter.
PS-PWM	: phase-shifted pulse width modulation.
PS-angle	: PWM carrier phase-shift angle.
OVA-PS-PWM	: optimal variable-angle phase-shifted pulse width modulation.

Chapter 1

Introduction

Nowadays, there is an increasing global concern for reducing fossil fuel reliance by promoting generation technologies related to clean and renewable energy sources (RES), such as solar photovoltaic (PV) and wind turbines. This tendency in the generation sector is being carried out not only for the RES capability to reduce carbon emissions but also for its capability to promote economic growth [1], [2]. Consequently, the global renewable power capacity is expected to be expanded by 50% between 2019 and the end of this year [3]. Moreover, this increasing trend in RES should be sustained in the following decades, as Chile, Australia, USA, and EU governments have announced their target to reach zero carbon emissions by 2050, while China aims to reach this target by 2060.

The intermittent nature of some RES and new types of loads, such as electric vehicles (EVs) charging stations, variable-speed drives, power supplies, and light-emitting diode drivers, have brought new technical challenges to the grid stability and its operation [4], [5]. These challenges are related to the temporal energy mismatch between local generation and consumption, which can affect the output power quality of the grid, i.e., the ability of the electrical system to create an ideal power supply with a pure noise-free sinusoidal waveform [6]. Poor power quality leads to disturbances in the power flow through transmission lines, increasing power losses and conditioning the continuity of service in the most severe cases. As a consequence, significant operating reserves are required to meet the demand in case of sudden variations in the output of RES, which causes an increase in the operational cost and complexity of the electricity network [4]. Some of the expected power quality issues associated with a high RES penetration include the fluctuation in voltage, increased

reactive power flow, harmonics injection, and excessive neutral currents [7].

A solution to enhance grid stability despite high RES adoption levels is to use battery energy storage systems (BESS), which have attracted the scientific community and the industry attention in recent years [4]. BESS can provide multiple services to grid operators, distributed generators, energy retailers, and consumers [8], [9]. For instance, BESS can absorb active power to charge the batteries when there is a surplus of RES power generation and output this power when it is most convenient. Furthermore, BESS can provide operating reserves and allow the creation of new revenue models for existing RES-based power generators, such as energy arbitrage, peak-shaving, and voltage and frequency control.

Despite the technical benefits obtained by incorporating BESS into the electrical grid, the high investment cost of new batteries is still a prominent barrier that limits the massive integration of this technology. Accordingly, developing profitable projects is challenging if the energy prices are not increased or new monetary incentives for ancillary services are not introduced. Hence, the economic viability of BESS is still unclear for the following years for some energy markets [10].

On the other hand, the world has initiated a revolution in transportation electrification, in which the EV market has shown exponential growth in recent years [11]. Indeed, the number of EVs and hybrids in circulation will reach 130 million by 2030, based on the forecast presented in [3]. The first life of these EV batteries will be considered to be over after the warranty period of the EV, which usually is over after reaching more than 160,000 kms driven. After this period, the remaining energy capacity of the EV batteries tends to vary between 70% and 80% of their nominal value [12]. Furthermore, intact BPs or battery modules from crashed EVs can exhibit higher remaining energy capacities by the end of their first life due to reduced aging [13].

Consequently, this significant remaining capacity, together with the high energy density and long life of Lithium-ion batteries (LIBs) [14], makes the LIBs, discarded from the EV market, attractive for their reuse in grid-connected second-life battery (SLB) energy storage applications. Moreover, this reutilization offers substantial environmental and economic benefits [15].

SLB costs are significantly lower than new batteries, while they retain most of their performance capabilities [16]. As a result, these batteries can potentially overcome the high investment cost barrier of BESS. Furthermore, SLB applications are expected to play

a crucial role in the next decade by giving more time to the recycling industry to scale up the technology required to effectively recycle LIBs [17].

One of the major challenges of creating high-power second-life BESS (SL-BESS) is related to the fact that incorrect handling of LIBs with different capacities can lead to inefficient use of the available stored energy. Moreover, inadequate LIBs charging/discharging operations might lead to significant safety risks, with one of the most severe consequences being battery incineration due to thermal runaway [18]. Therefore, the performance and safety concerns related to LIBs become more prominent in SL-BESS than in standard BESS, as SLBs can present significant differences among battery modules. For instance, an SL-BESS can contain batteries from different EV models and/or batteries with different degradation levels. In this sense, special attention must be given to the power converters and control algorithms that can allow the efficient and safe integration of SLBs into the electrical grid.

The following section reviews the main topics related to BESS and SL-BESS applications used in industry or proposed in the current literature.

1.1 Battery Energy Storage System Components

In this section, the main components of a BESS are described and grouped into four categories: 1) battery and power conversion system (PCS), 2) battery management system (BMS), 3) energy management system (EMS), and 4) converter control. A diagram of these categories is illustrated in Fig. 1.1.

1.1.1 Battery and PCS

Power electronics is the key enabling technology allowing the connection of BESS to the electricity grid [19]. The PCS serves as the interface between the battery dc-voltage and the grid ac-voltage. Therefore, it enables the controlled, secure, and efficient power exchange between the batteries and the system they are connected to [20]. In this way, the PCS allows the BESS to meet grid codes and standards when providing services to the energy market [4].

The nominal voltage of electrochemical cells is very low concerning the required grid connection voltages. Taking Lithium-ion cells as an example, they typically have nominal

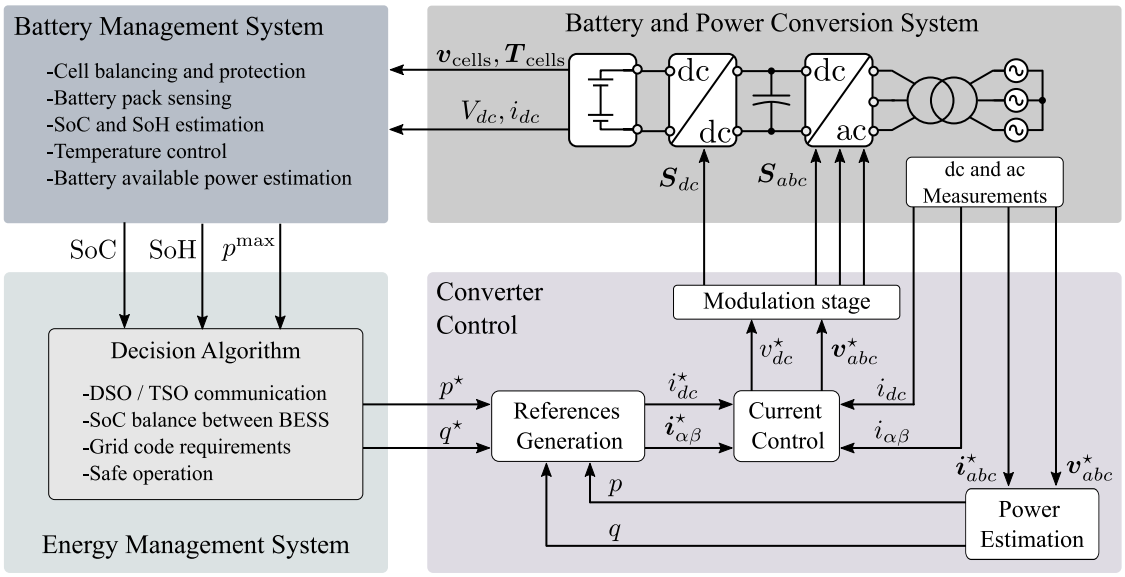


Figure 1.1: BESS main components.

voltages of 3.2 V - 3.6 V for Lithium Iron Phosphate (LFP) chemistry and 3.6 V for Lithium Cobalt Oxide (LCO), Lithium Nickel Cobalt Aluminum Oxide (NCA), and Lithium Nickel Manganese Cobalt Oxide (NMC) chemistries. Additionally, the capacity of commercially available cells is usually limited to a few hundred Ah or less. As a consequence, several cells must be connected in series and parallel to achieve the desired power and energy capacity requirements of a grid-connected BESS.

The trade-off regarding how many cells to wire in series versus in parallel to achieve the battery pack (BP) maximum power design requirements is generally determined by several factors, such as manufacturing economics and BP safety, volume, and modularity [18], [20]. A higher BP voltage for the same power reference leads to a lower battery current. Hence, the conduction losses are reduced for the same output power. However, the series connection of cells requires specialized balancing and measuring circuits installed as part of the BMS, increasing its complexity. These balancing circuits for series-connected cells are required to compensate for their energy capacity imbalance and to operate the battery pack efficiently and safely [21], [22]. If the cell balance condition is not met, then one or more cells have a state of charge (SoC) that is too high or too low regarding others, leading to a reduced effective energy capacity of the pack, increased capacity fading of cells, or even safety hazards [18], [23].

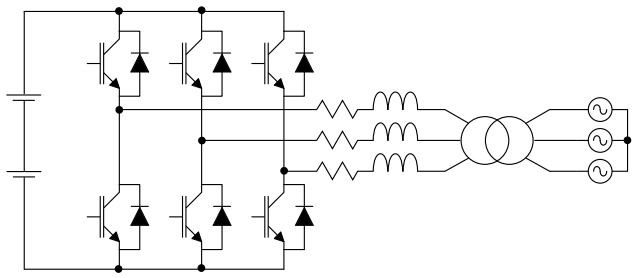


Figure 1.2: BESS based on the conventional 2L-VSC.

The factors mentioned above involved in the battery pack design have led researchers to propose several PCS topologies for integrating BESS into the electrical grid [4], [20], [24]. The different features of some of the most popular topologies are discussed in the following section.

Conventional 2L and 3L Voltage Source Converters

The two-level voltage source converter (2L-VSC) is shown in Fig. 1.2. This configuration is currently the industry's preferred choice for interfacing BESS with the grid [8]. However, an additional line frequency transformer is required to connect the BESS to medium/high voltage transmission lines, which is bulky, costly, and it introduces additional losses. Despite these drawbacks, this transformer offers the advantage of limiting the rise time of short-circuit currents, helping the converter protection system. In this way, the 2L-VSC handles the bidirectional power flow between the battery and the ac grid, whereas the transformer boosts the voltage of hundreds of volts of the battery pack to medium voltage (MV) levels, i.e., tens of KVs.

The same scheme can be applied to the conventional three-level voltage source converters (3L-VSCs) topologies, such as neutral point clamped (NPC), flying capacitor (FC), and T-Type converters [8], [24], which are shown in Fig. 1.3. The extra level of these converters allows an extra degree of freedom at the converter output voltage magnitude, improving the harmonic distortion and reducing the switching frequency. However, this benefit comes at the expense of using more semiconductor devices and more complicated control and modulation schemes [25], [26].

Many BPs with their respective 2L or 3L-VSCs must be connected in parallel to create a large-scale BESS with power ratings of several MWs. The main advantage of this config-

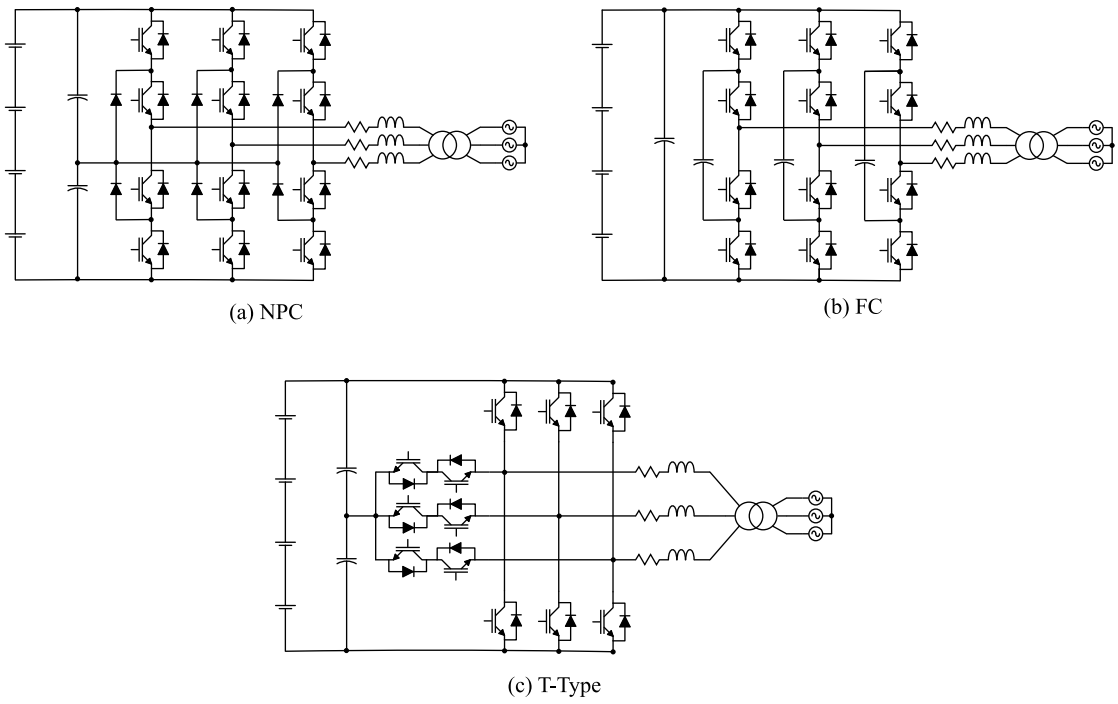


Figure 1.3: Three-level converter topologies.

uration is its high reliability and decoupled control of the BP power references [20]. Indeed, the failure in one BP or PCS does not necessarily lead to the whole system's interruption under this configuration, and each PCS can be easily disconnected from the rest of the system through a conventional voltage breaker.

The major limitation of these topologies for SL-BESS is related to the fact that large BPs are required to reach a minimum dc voltage level needed for connecting the inverter to the ac grid, which increases the BMS complexity [27]. Moreover, manufacturing these packs might not be feasible with SLBs, as the direct series or parallel connection of batteries with a different state of health (SoH) can lead to hazardous conditions. In fact, the direct connection of batteries with different capacity or internal resistance values, or the replacement of particular cells within an existing BP, is almost universally disapproved of by BESS manufacturers [28]. Accordingly, using these topologies with second-life BPs of reduced power and voltage might require extra semiconductor devices to boost the dc voltage. Moreover, connecting each second-life BP to independent inverters might also increase the PCS costs as these packs cannot easily reach hundreds of kW for prolonged periods of time.

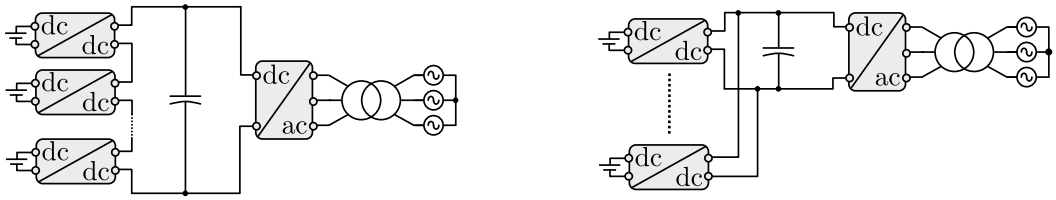


Figure 1.4: Front-end inverter with controllable dc-link topologies. (a) modules are connected in series (cascaded connection), and (b) modules are connected in parallel.

Front-End Conventional Inverter Topology with Controllable dc-link

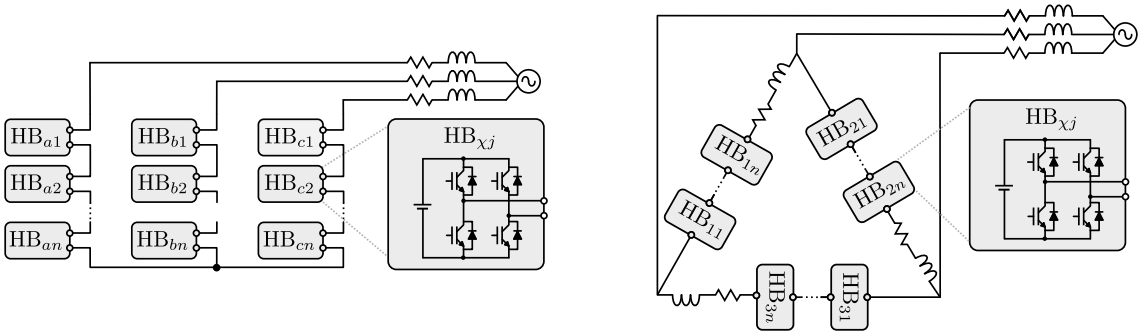
A different approach for reducing the BMS complexity is to divide the BP into smaller modules by using dc-dc converters with a cascaded or parallel connection. This configuration creates a controllable dc-link connected to a front-end 2L- or 3L-VSC, as shown in Fig. 1.4.

The reliability of these configurations is analyzed in [20]. Here, the cascaded connection showed the weakest configuration, as its efficiency is the lowest and it requires more complex active SoC balancing control schemes to connect battery modules of different capacities. Moreover, the dc-link voltage range is compromised by the failure of individual battery modules. As a result, the reliability and flexibility of the SL-BESS might deteriorate under this topology if the BP is divided into only a reduced number of battery modules.

On the other hand, better results in terms of efficiency and reliability were obtained for the parallel connection of battery modules to a front-end inverter [20]. The increase in reliability is due to each dc-dc converter independently controlling the current profile of its battery module. Therefore, batteries of different capacities and power ratings can be included in independent SMs, and their SoC can be balanced using conventional control schemes.

Cascaded H-Bridge Converter

The cascaded H-bridge converter (CHB) consists of three-phase arms, where each arm is formed by the series connection of multiple H-bridge (HB) sub-modules (SMs) and a filter inductor. These arms can be connected in either star (Y-CHB) or delta (Δ-CHB) configuration as illustrated in Fig.1.5. The modular structure of the CHB converter allows this topology to be directly connected to higher ac output voltage levels and provide



(a) Star-connected CHB (Y-CHB) (b) Delta-connected CHB (Δ-CHB)

Figure 1.5: CHB converter-based BESS with BPs directly connected to the SMs. (a) star configuration, (b) delta configuration.

fault-tolerant capabilities. In fact, the scalability of the CHB converter enables the transformerless connection of this converter to the MV grid with less harmonic distortion and reduced switching losses without increasing the voltage rating of individual switching devices [29].

In addition, the modular structure of the CHB allows the separation of the BP into smaller modules with fewer series-connected cells at their battery strings, decreasing the complexity of the BMS. Besides, the CHB converter allows uneven power distribution among its arms and its SMs, enabling the active balance of SoC among BPs [27], [30]. In this sense, EV BPs can be directly connected to independent converter SMs, allowing their integration without a significant intervention of the original packs. Alternatively, a dc-dc converter stage can be considered to interface each battery with the CHB converter SMs. However, this extra power conversion stage per BP can increase the converter cost, making it less attractive against the conventional 2L-VSC [4].

In [4], an efficiency and cost analysis for BESS converter topologies was carried out. The results of this analysis indicate that the transformerless CHB converter is the most affordable PCS for integrating BESS into the MV grid and exhibits lower losses than conventional 2L- and 3L-VSCs. These advantages and the capacity of the CHB converter to provide uneven power distribution among its SMs make this topology a promising alternative for next-generation SL-BESS inverters [20].

Nevertheless, the unbalanced power distribution among SMs poses additional challenges to the control system of the CHB converter [31], [32]. If the active power references are not

properly assigned among SMs, the battery with the lowest capacity might reach its minimum SoC threshold considerably faster than the others [33], limiting the performance of the BESS. Furthermore, the CHB converter has a limited capability to assign unbalanced power reference to its SMs [31]. Thus, neglecting these power limits in the SoC balancing control strategy deteriorates the converter current control tracking and may lead to undesired harmonic distortion due to overmodulation or even harm some batteries.

Finally, a potential issue of the CHB topology that has been recently investigated is the impact of the current ripple at the battery port when the batteries are directly connected to the HB-SMs. Two main ripple components can be identified in the battery port. One component is related to the high-frequency pulse-width modulation (PWM), whereas the other is given by the pulsating power injected by each converter leg at the double ac frequency of the grid. Accordingly, experimental results indicate that the current ripples might accelerate the capacity fade of the batteries if the ripple brings a considerable increase in the operating temperature of the BPs [34]. Nevertheless, it remains unclear to this date whether these ripple components significantly affect the lifespan of batteries, provided that temperature is controlled and low current rates are used [35].

Modular Multilevel Converter

As depicted in Fig.1.6, the three-phase modular multilevel converter (MMC) consists of three legs connected in parallel to a common dc-bus. Each leg is divided into two arms named as upper and lower. These arms are formed by the series connection of SMs with a filter inductor. Each converter leg's midpoint is connected to an ac output filter. One of the main applications of the MMC is high-voltage direct-current (HVDC) systems [36], as the converter allows the direct connection to a high-voltage dc-grid. Nevertheless, this dc-voltage connection is not mandatory for BESS applications [37].

The MMC also allows for splitting the BP into smaller SMs, similar to the CHB converter. Therefore, active SoC balancing can be implemented [37]–[39]. Moreover, the MMC offers an extra degree of freedom for SoC balancing when compared to the CHB converter, which is given by the converter circulating currents, i.e., the currents that circulate through the clusters of each phase leg, but without appearing in the output currents [40].

The MMC shares challenges similar to those of the CHB converter regarding the control complexity of the SoC balancing algorithms and the active power reference distribution

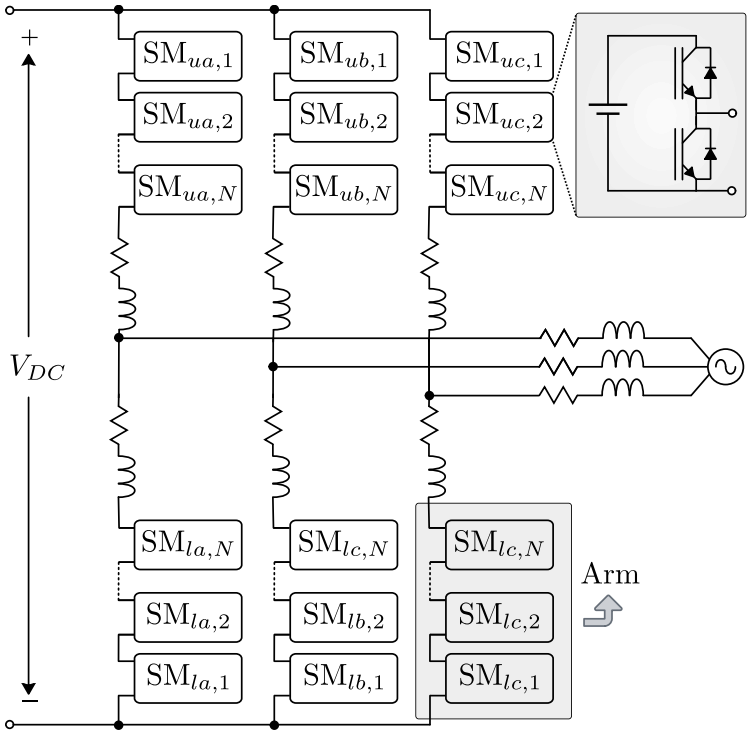


Figure 1.6: MMC-based BESS with BPs directly connected to the SMs.

among SMs. Besides, the MMC requires a higher number of components [4]. Nonetheless, both the MMC and the CHB converter are considered promising candidates for integrating modular SL-BESS [31], [41]. Therefore, research efforts are being concentrated on developing new power-sharing strategies that ensure effective SoC balance for both converter topologies [20].

1.1.2 Battery Management System

The BMS is an embedded system built specially to make the battery operation safe, reliable, and cost-effective [42]. In this sense, the BMS actively controls the BP functions to maximize its life by considering the maximum battery power and temperature ratings for its operation conditions. Moreover, the BMS is often responsible for providing accurate estimations of the battery SoC and SoH, which are reported to the EMS. Some of the main tasks usually performed by BMS are enumerated below [18]:

1. Protect the safety of the BESS: the BMS detects unsafe operating conditions, such as overcharge or overcurrent, and loss of insulation, disconnecting the battery pack

from its output power terminals if necessary.

2. Battery-pack sensing: the BMS continuously senses each series-connected cell voltage, the BP current, and some cell temperatures.

3. SoC and SoH estimation: the BMS makes estimations of the cell's SoC and SoH based on the measured signals.

4. Battery pack power estimation: the BMS estimates the maximum power the battery pack can deliver at each instant by considering the configuration of the cells in the BP and its temperature.

Battery SoC Estimation Methods

As previously mentioned, one of the primary functions of the BMS is calculating the battery SoC, which is an indicator that quantifies the remaining charge of a battery regarding its total capacity [43]. An accurate estimation of SoC produces additional benefits to the operation of the BP, such as promoting the longevity of the battery by avoiding over-charging and over-discharging. Moreover, precise SoC estimates improve the performance and power density of the battery by allowing the EMS to aggressively use the entire BP capacity [18].

The SoC estimation challenge arises since SoC cannot be directly measured in a battery. Therefore, it must be inferred from measurable variables, such as current, voltage, and temperature. A classification of the main SoC estimation methods is shown in Fig. 1.7.

Among the open-loop SoC estimation methods, the coulomb counting method is based on measuring the amount of charge added to or removed from the battery, leading to a straightforward implementation. However, this SoC estimation technique lacks a feedback signal to correct the state estimation. As a consequence, this method is susceptible to current sensor measurement errors, sensor noise, wrong SoC initialization, and errors in estimating the total capacity and coulombic efficiency parameters [18].

The open circuit voltage (OCV) look-up table method is based on performing SoC estimates based on a previously established relationship $v(k) \approx \text{OCV}(z(k))$, where $v(k)$ is the terminal voltage of the cell, and $z(k)$ refers to the battery SoC. This voltage and SoC relationship can be determined by slowly charging and discharging the battery for a full cycle [18]. Nevertheless, using an OCV look-up table only provides accurate estimates

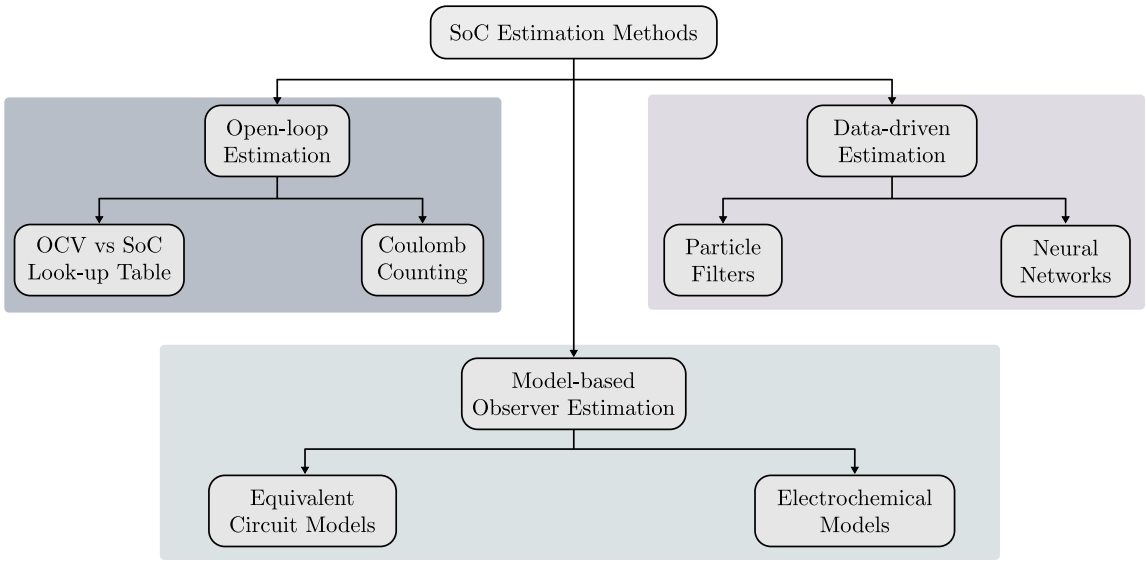


Figure 1.7: Classification of the main SoC estimation methods.

when the battery is resting, i.e., after being disconnected from a load for several minutes. Thus, the OCV method in practice is only used to calculate the SoC initial condition for a different estimation method after a resting period [44].

Data-driven methods have attracted the interest of the research community lately due to the recent advances in machine learning, and the greater availability of battery data [45]. These methods can establish a relationship between the measured variables, and the SoC and SoH without any previous knowledge of the chemistry and characteristics of the battery [46]. However, these algorithms are susceptible to the training data selection and may present a poor performance when this data cannot completely cover the present operating conditions of the BP [43].

Finally, model-based estimation methods consist of using a battery model to predict the battery terminal voltage based on the cell voltages, current, and temperature measurements while applying an estimation algorithm to compute the SoC [47]. Several models of different complexity have been proposed and analyzed for optimal control applications in [46]. The equivalent circuit models are widely used for their satisfactory performance and low computational burden. More advanced and precise electrochemical models have also been proposed [46]. However, their high computational load requirements often challenge their application for real-time control purposes.

1.1.3 Energy Management System

The EMS objective is to operate the BESS efficiently by optimally scheduling its operation and coordinating the multiple batteries and storage devices of the system, which can vary in size and technology [48]. The EMS collects from the BMS the battery status information and additional operational data such as measurements at the point of common coupling (PCC), energy market prices, weather forecasts, and commands from the distribution and transmission system operators [8].

Concerning the EMS control strategy, no solution emerges as the most common one, as there are many different BESS applications, such as peak shaving, renewable capacity firming, frequency regulation, and synthetic inertia, among others [8]. Nevertheless, model predictive control (MPC) strategies have been cataloged as promising techniques that can deal with the uncertainties of forecasts in multi-step optimization problems [49]–[51]. As a consequence, several MPC strategies for handling distributed BESS have been proposed in the field of microgrids, e.g., [49]–[54].

1.1.4 Converter Control for Grid-Connected ac-dc Converters for BESS

The control for grid-connected converters is focused on regulating the power flow between the BESS and the grid by controlling the power semiconductor devices. Usually, the active and reactive power references for these control loops in BESS are determined by the EMS [48].

The conventional methods for governing grid-connected power converters are given by linear controllers generating continuous modulating signals. These signals are then transformed into high-frequency pulses using a modulation stage [55]. Among these control schemes are the classical proportional-integral (PI) regulators in the rotating synchronous dq-reference frame, and the proportional-resonant (PR) controllers implemented in $\alpha\beta$-frame [56]. These control techniques are widely employed in several industrial applications due to their well-known design procedures. These techniques usually are categorized under the family of voltage-oriented control (VOC) schemes [57].

A different category of control methods for grid-connected ac-dc converters are direct power control (DPC) strategies. These techniques aim to directly govern the instantaneous active and reactive powers without using any inner-loop current regulator. Conventional

DPC strategies obtain the switching actions from look-up tables and hysteresis comparators [58]. Nevertheless, the hysteresis comparators lead to variable switching frequency, complicating the passive filter design. A different approach is proposed in [59], where PI regulators control the active and reactive powers by generating synchronous dq-voltage references directly from the active and reactive power tracking errors.

Modern control schemes such as sliding mode control [60], artificial intelligence control [61], [62], MPC [63], are becoming more popular for power converters since the last decade. This trend has been motivated by the continuous progress in digital control platforms, e.g., digital signal processors (DSPs) and field programmable gate arrays (FPGAs). The improvements of these control methods over the classical ones are related to the better handling of non-linearities and improved dynamic performance.

The previously mentioned standard dc-ac control techniques can be directly applied to 2L- and 3L-VSC topologies with a centralized BP. However, in cascaded multilevel converters that distribute the battery modules within the converter power cells, additional control loops are required to balance the internal energy of the BESS among BPs. These SoC balancing control loops are crucial for SL-BESS due to differences in capacity, and the SM power references disparity constraints imposed by the cascaded multilevel converter topologies [31]. Accordingly, the following section reviews different control schemes for the internal energy balance designed specifically for these power converters.

1.1.5 SoC Balancing Control Schemes for CHB Converters and MMCs

New control techniques have been developed in recent years to integrate BPs into multilevel converter topologies with cascaded cells, such as the CHB converter and the MMC. These control schemes are designed to track active and reactive power references to exchange power between the BESS and the electrical grid while providing an internal energy balance among SMs that regulates each BP SoC.

The necessity of closed-loop SoC balancing control schemes is related to the full utilization of the available energy in the BESS. Indeed, without active energy balancing among SMs, the battery with the lowest capacity, which is the first to reach 0% SoC during discharging, limits the BESS usable capacity. As a consequence, in this scenario, some BPs cannot be further discharged without over-discharging, which leads to permanent battery damage in the weakest BPs [18].

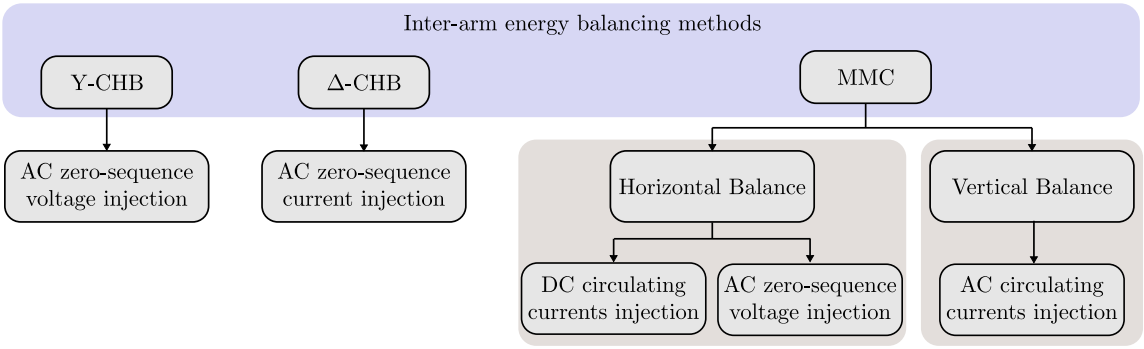


Figure 1.8: Inter-arm energy balancing methods for cascaded multilevel converters.

Both, the CHB converter and the MMC allow the SoC balancing control of the different BPs by regulating either the output power reference or the dc current for each SM. Therefore, batteries of different capacities or even SLBs of different manufacturers can be included in the same cascaded multilevel converter without necessarily limiting the system capacity to the weakest battery [64], [65]. Nevertheless, the maximum power imbalance among SMs is physically constrained in these converters as arbitrary power references for each cell are not feasible in many cases. These power limit constraints are not only given by the individual BP power ratings but also due to the coupling between the series-connected SMs, which share the same arm current [31]. Therefore, developing effective energy-balancing techniques for these converters adds complexity to the power converter control system.

The SoC balance control problem in cascaded multilevel converters is usually divided into two sub-problems: the inter-arm energy balance and the inter-SM energy balance problem. These control problems are described in the sections below.

Inter-arm Energy Balance

The primary control objective of inter-arm energy balance strategies is to equalize the average stored energy among the arms of the converter [66]. In this sense, the inter-arm energy balance controller is generally designed without paying attention to the SoC of individual BPs [32]. As a consequence, the control system for standard inter-arm energy balancing strategies usually models the converter arms as ideal controlled voltage sources. In order to balance the energy among phases in cascaded multilevel converters, the inter-arm energy balance strategies provide additional arm currents or voltage references, which

can transfer active power among the arms without affecting the power exchange with the electrical grid.

The voltage or current injection needed to achieve inter-arm power imbalance depends on the converter topology. Accordingly, Fig. 1.8 summarizes the required signals to transfer power among arms for standard cascaded multilevel converters. The calculation of these voltage and current references for each converter are reviewed in [66], [67] for the MMC, and in [32], [68], [69] for the CHB converter. In general, these techniques can find the required circulating current or zero sequence voltage references to achieve the desired inter-arm power imbalance, by using phasor analysis or analytical solutions based on the converter power references and instantaneous measurements at the PCC.

Inter-SM Energy Balance

The main control objective for the inter-SM energy balancing schemes is to maintain each BP SoC equal to the average SoC of all the BPs connected within an arm [70]. In the case of SL-BESS, achieving the inter-SM SoC balance is challenging, as the active power distribution among SMs can be highly unbalanced due to differences in energy capacity. In this sense, the inter-SM SoC balance control ensures that batteries with larger capacities operate with larger currents. Moreover, it allows the SMs connected to malfunctioning SLBs to provide zero active power without requiring a major shutdown of the SL-BESS.

In contrast with the inter-arm energy balancing strategy, the inter-SM SoC balancing control schemes do not depend on the cascaded multilevel converter topology but on the modulation technique applied to the power cells. Accordingly, the conventional modulation stages and the classification of the inter-SM energy balance control techniques regarding the converter modulation stage for cascaded multilevel converters are summarized in Fig. 1.9 and Fig. 1.10, respectively.

Phase-shifted pulsewidth modulation (PS-PWM) is one of the most popular modulation strategies for cascaded converters [71]. In this method, the switching signals for each SM are obtained using a standard PWM technique with a triangular carrier signal. A specific phase-shift-angle (PS-angle) is applied among the carriers to achieve the optimal harmonic performance [72]. As a result, the output voltage effective switching frequency of the cascaded converter becomes $2nf_c$, with n the number of SMs within each arm of the converter, and f_c the PWM carrier frequency.

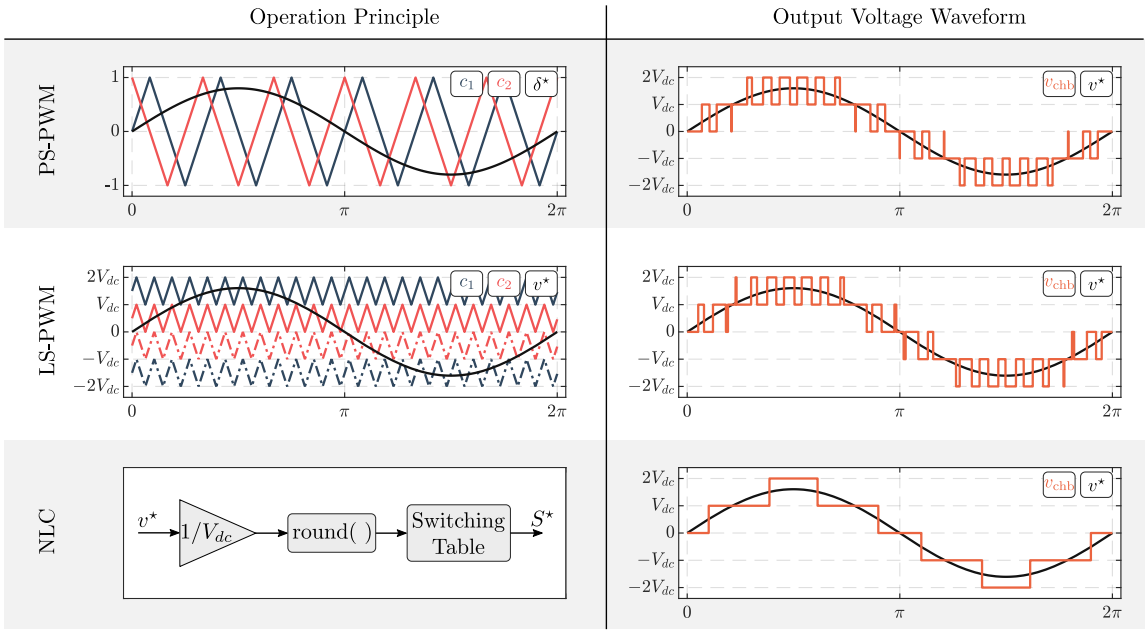


Figure 1.9: Conventional modulation strategies for cascaded multilevel converters applied to a single-phase CHB converter of 2 SMs.

The level-shifted PWM (LS-PWM) strategy can also be applied to cascaded converters. However, its conventional implementation is not preferred over the PS-PWM for the MMC and the CHB converter due to the uneven switching and conduction losses among SMs [71]. The LS-PWM method vertically distributes the triangular carriers and compares them with the arm voltage reference. Thus, only one SM can change its output voltage during the sampling period while the others remain in a fixed switching state. In this way, the switching SM changes every time the modulating voltage requires a different output voltage level or if the vertical alignment of the carriers is modified [73].

Finally, the nearest level voltage control (NLC) offers an alternative approach to reduce the switching losses of PWM strategies in cascaded multilevel converters. This method generates the switching states of the SMs using the rounded value of the arm reference voltage, leading to a constant on/off operation for each semiconductor device during every sampling period [71]. Consequently, NLC reduces the switching frequency at the expense of higher harmonic distortion and increased error in generating the output voltage reference, which reduces the applicability of this method for converters of a reduced number of SMs [74].

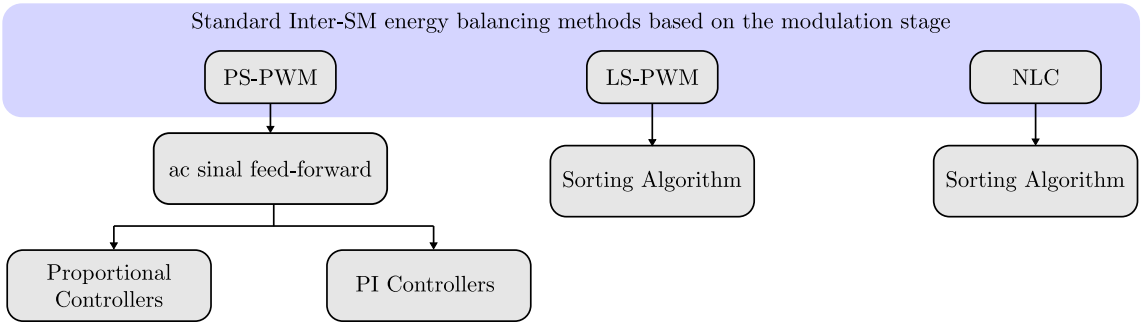


Figure 1.10: Standard inter-SM energy balancing strategies classification for cascaded multilevel converters based on the modulation scheme.

One of the first inter-SM SoC balancing control schemes for PS-PWM was introduced in [30] for the CHB converter and implemented in a 500 kW project [75]. Here, the arm modulating voltage references are obtained using the classical current control scheme in the rotating synchronous *dq*-frame. However, instead of applying equal modulating voltages to each SM, their voltage references are individually adjusted by an additional feed-forward term. This term is based on proportional controllers that regulate the inter-SM SoC balance. The feed-forward terms are fed with SoC error signals, calculated as the difference between the individual SoCs and the arm average SoC. The outputs of the proportional controllers are multiplied by a sinusoidal signal in phase with the arm modulating voltage, effectively modifying the active powers of each BP to correct SoC balance errors.

Following the same principle, additional works that add a fundamental frequency ac component to each SM modulating signal have been proposed [76]–[78]. In these works, the proportional controllers are used to obtain an SM power reference based on their SoC error, while PI regulators are used to track these references without steady-state errors.

One major problem with these techniques is that the controller gain selection becomes challenging when batteries exhibit different capacities. Furthermore, large SoC balance errors can result in SM voltage references that saturate the modulator or in high currents that break the safe power limits of some battery packs [70]. Therefore, these inter-SM control schemes may not be suitable for SL-BESS applications that present significant capacity and power rating differences among their BPs.

In [65] and [33], inter-SM SoC balancing strategies specially designed for SL-BESS based on the CHB converter with a PS-PWM stage have been recently introduced. In these techniques, power references for each SM are generated by a weighting factor policy

instead of using proportional controllers. In this way, the proposed techniques consider the SoC, capacity, and voltage of each BP to obtain the SM power references. Despite the fact that this weighing factor-based SoC control scheme can generate power references that always reduce the SoC balancing errors among SLBs, over-modulation in the PS-PWM stage due to large capacity differences among battery modules cannot always be avoided for the full range of SoC [33]. Moreover, the PI controllers used to regulate the active power of each SM also lack a mechanism to limit the SM powers without affecting the current control [70].

A different approach to achieve inter-SM energy balance is to use sorting methods [73], [79]–[81], which are usually implemented with an LS-PWM or NLC modulation stage. In the sorting SoC balancing control schemes, a priority list is created based on the SoC balancing error of each BP and the instantaneous arm current sign. Then, a voltage-matching algorithm is applied to meet the arm modulating voltage references while prioritizing the insertion of the SMs with the largest SoC imbalances. Conventional sorting SoC balancing techniques offer fast balancing speed. Nevertheless, they lack the ability to constrain the instantaneous power of each BP. Thus, these methods cannot guarantee that the SLB safe power limits are satisfied. Additionally, sorting algorithms can present scalability issues for converters with a large number of cells, as its implementation often requires a fast sampling frequency to modify the high-frequency switching pulses [82].

Finally, an additional challenge that affects the implementation of inter-SM SoC balancing control schemes in SL-BESS based on cascaded multilevel converters is related to the increased voltage harmonic distortion at the PWM carrier frequency and its multiples, which appears in the arm output voltage. This distortion arises when unbalanced power references among cells are imposed and/or when the batteries present different dc voltage levels, depending on the modulation strategy. As a consequence, new advanced modulation techniques, such as variable-angle PS-PWM strategies [83]–[85] are required to mitigate the low switching frequency harmonics that appear in the arm output voltage and deteriorate the output power quality of the converter.

1.2 Motivation and Research Vision

From the previous literature review, it is clear that the internal SoC balance in cascaded multilevel converters with batteries connected to the converter SMs adds several challenges for the converter control system. Furthermore, the standard control schemes proposed for CHB- or MMC-based BESS still present some considerable limitations by not taking into account the maximum modulation ranges, the battery module power constraints, the converter limitations to distribute the active power among SMs, and the adaptability required to consider battery aging effects over time. These issues are still more prominent for SL-BESS due to the significant differences that may be present in the BP parameters and the accelerated degradation that can be experienced for some of them [86]. Consequently, there is an opportunity to improve the CHB-based SL-BESS (CHB-SL-BESS) control schemes currently proposed in the state of the art.

During the last decades, MPC has emerged as a promising control alternative for governing energy storage systems and power converters due to its flexibility to include multiple control objectives and its ability to handle constraints [8], [51], [63]. In this control approach, the system model is used to predict the future behavior of the system state. This predicted behavior is included in an optimization problem, which is solved to obtain the best control action to achieve the control targets under consideration.

The existing battery models facilitate the real-time estimation of the SoC, battery capacity, and internal resistance [18]. As a consequence, applying proven battery models to an MPC strategy allows the control system to inherently consider the heterogeneity of SLBs in the formulation of the optimization problem. Furthermore, the operational constraints of both the converter and batteries can also be considered to compute optimal control inputs using an MPC scheme. Therefore, MPC strategies have the potential to fully exploit the multilevel converter capabilities for tracking the optimal SM power references in a CHB-SL-BESS while maintaining the safe operation of each SLB.

Motivated by the discussion above, the research vision for this thesis is focused on proposing novel MPC schemes that allow the optimal integration of SLBs directly connected to the power cells of CHB converters.

1.3 Research Proposal

This section presents a general overview of the key elements that support this research proposal. These elements include a general hypothesis, the main objective, and the specific objectives. Additionally, the major contributions of this thesis are also summarized in this section.

Hypothesis:

- An MPC scheme for a Δ-CHB converter-based SL-BESS can provide optimal SoC balancing, without deteriorating the output power quality of the converter and maintaining the BESS within its safe range of operation.

Objectives:

To prove or refute the proposed hypothesis for this research project, the main objective of this work is to develop a novel constrained MPC strategy for Δ-CHB converters that allows inter-arm and inter-SM energy balancing among SLBs directly connected in the converter SMs. Accordingly, the following specific objectives are considered:

1. To analyze the SoC dynamic model and the Δ-CHB converter capabilities to enable the inter-arm and inter-SM SoC balancing among its SMs.

2. To develop a new PS-PWM strategy that minimizes the harmonic distortion introduced by using heterogeneous BPs operating with different output powers and/or different voltage levels in a CHB converter arm with the BPs directly connected to the SMs.

3. To design and build an experimental setup with SLBs governed by the proposed MPC strategies. Success in this objective means the experimental demonstration of bidirectional power flow with the grid and active energy balancing between heterogeneous BPs, which provides a proof of concept of the proposed technology in a scaled-down prototype.

4. To implement and evaluate the performance of the proposed constrained MPC strategy for CHB converters with integrated SLBs. Success can be verified by evaluating the controller SoC balancing performance in the experimental setup.

1.4 Major Contributions of the Thesis

In this section, a list of the major contributions related to this research project is presented.

1. This thesis proposes a novel discrete-time dynamic model to predict the future behavior of the CHB converter output voltage switching harmonics, considering each PWM carrier PS-angle as a control input. The model is derived based on a frequency analysis of the CHB converter output voltage based on the Fourier Series, which reveals the cause of increased harmonic distortion in CHB-SL-BESS when the standard PS-PWM strategy is implemented.

2. This thesis uses the proposed harmonic distortion dynamic model to develop a predictive optimal variable angle PS-PWM (OVA-PS-PWM) strategy. The key novelty of this modulation strategy lies in the derivation of an analytic solution for an optimal PS-angle update rule, which can be applied to CHB converters of any number of SMs and minimize several harmonic components. The proposed optimal PS-angle update rule outperforms previously proposed variable angle PS-PWM strategies by providing optimal solutions for the complete operational range of the CHB converter. Moreover, it provides excellent harmonic performance even in operation scenarios with severe power imbalance among the converter SMs, maintaining the main benefits of PS-PWM for SL-BESS applications.

3. A Kalman filter (KF) harmonic compensator strategy is proposed in this thesis to eliminate the steady-state error and low-frequency current harmonic distortion in the Δ-CHB converter currents when applying optimal control strategies. The proposed KF strategy compensates for modeling errors caused by system parameter uncertainties and external disturbances. As a result, the proposed KF strategy allows the operation of the CHB-SL-BESS without requiring measurements of the SM capacitor voltages for the real-time control platform or fast communications with the BMS. Therefore, this KF strategy can reduce the hardware and communication complexity of CHB-SL-BESS.

4. Finally, this thesis proposes a dual-stage MPC (DS-MPC) SoC balancing strategy for CHB-SL-BESS. The proposed control strategy considers the coupling between the inter-arm and inter-SM energy power imbalance problems by obtaining an optimal circulating current reference and optimal modulating signals for each SM. Moreover, this proposed MPC scheme includes safety constraints for both SLBs and the power converter, and it can be directly implemented with the proposed OVA-PS-PWM and KF harmonic compensator. As a result, the proposed DS-MPC achieves optimal battery currents at each SM, which favors the rapid SoC balance among SLBs while operating the CHB-SL-BESS within its safe operation range at all times.

1.5 List of Publications

Published Journal Papers

1. **P. Poblete**, R. Cuzmar, R. P. Aguilera, J. Pereda, A. M. Alcaide, D. Lu, Y. P. Siwakoti, G. Konstantinou,"Dual-Stage MPC for SoC Balancing in Second-Life Battery Energy Storage Systems Based on Delta-Connected Cascaded H-Bridge Converters" in IEEE Trans. Power Electron., doi: 10.1109/TPEL.2024.3461749.

2. **P. Poblete**, R. P. Aguilera, J. Pereda, A. M. Alcaide, R. Cuzmar, D. Lu, Y. P. Siwakoti, P. Acuna, "Offset-Free Optimal Control of Cascaded H-Bridge Converters Based on a Kalman Filter Harmonic Compensator" in IEEE Trans. Power Electron., doi: 10.1109/TPEL.2024.3472451.

3. **P. Poblete**, J. Gajardo, R. Cuzmar, R. P. Aguilera, J. Pereda, D. Lu and A. M. Alcaide, "Predictive Optimal Variable-Angle PS-PWM Strategy for Cascaded H-Bridge Converters" in IEEE Trans. Ind. Electron., vol. 71, no. 11, pp. 13556-13566, Nov. 2024, doi: 10.1109/TIE.2024.3370998.

4. A. M. Alcaide, **P. Poblete**[1], S. Vasquez, R. P. Aguilera, J. I. Leon, S. Kouro and L. G. Franquelo, "Generalized Feed-Forward Sampling Method for Multilevel Cascaded H-Bridge Converters," in IEEE Trans. Ind. Electron., vol. 71, no. 8, pp. 8259-8267, Aug. 2024, doi: 10.1109/TIE.2023.3319737.

[1]Equal contribution between both first authors.

Conference Papers

1. **P. Poblete**, R. P. Aguilera, J. Pereda, R. H. Cuzmar, D. Lu, and Y. P. Siwakoti, "Instantaneous Circulating Current Reference Design Strategy for Inter-arm Power Imbalance Control in Delta-connected CHB Converters," 2024 IEEE 9th Southern Power Electronics Conference (SPEC), Brisbane, Australia, 2024, (Accepted Paper).

2. **P. Poblete**, R. P. Aguilera, A. M. Alcaide, R. H. Cuzmar, Y. P. Siwakoti, and D. Lu, "LQG Current Control Strategy for a CHB Converter-Based Second-Life Battery Energy Storage System without Steady-State Error," 2024 34th Australasian Universities Power Engineering Conference (AUPEC), Sydney, Australia, 2024, (Accepted Paper).

3. R. H. Cuzmar, **P. Poblete**, R. P. Aguilera, J. Pereda and D. Lu, "Power Balance of a Delta-Connected CHB Converter with MPC for Photovoltaic Systems," 2023 IEEE International Future Energy Electronics Conference (IFEEC), Sydney, Australia, 2023, pp. 305-310, doi: 10.1109/IFEEC58486.2023.10458456.

4. A. M. Alcaide. **P. Poblete**, S. Vazquez, R. P. Aguilera, S Kouro, J. I. Leon and L. G. Franquelo, "Feed-Forward Technique to Emulate Natural Sampling Method for Cascaded H-Bridge Converters," IECON 2023- 49th Annual Conference of the IEEE Industrial Electronics Society, Singapore, Singapore, 2023, pp. 1-7, doi: 10.1109/IECON51785.2023.10312396.

Contribution in Related Journal Papers

1. **P.Poblete**, S. Neira, R. P. Aguilera, J. Pereda and J. Pou, "Sequential Phase-Shifted Model Predictive Control for Modular Multilevel Converters," in IEEE Trans. Energy Convers., vol. 36, no. 4, pp. 2691-2702, Dec. 2021, doi: 10.1109/TEC.2021.3074863.

2. **P.Poblete**, G. Pizarro, G. Droguett, F. Núñez, P. D. Judge and J. Pereda, "Distributed Neural Network Observer for Submodule Capacitor Voltage Estimation in Modular Multilevel Converters," in IEEE Trans. Power Electron., vol. 37, no. 9, pp. 10306-10318, Sept. 2022, doi: 10.1109/TPEL.2022.3163395.

3. G. Pizarro, **P.Poblete**, G. Droguett, J. Pereda and F. Núñez, "Extended Kalman Filtering for Full-State Estimation and Sensor Reduction in Modular Multilevel Con-

verters," in IEEE Trans. Ind. Electron., vol. 70, no. 2, pp. 1927-1938, Feb. 2023, doi: 10.1109/TIE.2022.3165286.

4. R. H. Cuzmar, A. Mora, J. Pereda, **P. Poblete** and R. P. Aguilera, "Long-Horizon Sequential FCS-MPC Approaches for Modular Multilevel Matrix Converters," in IEEE Trans. Ind. Electron., vol. 71, no. 5, pp. 5137-5147, May 2024, doi: 10.1109/TIE.2023.3286013.

5. R. H. Cuzmar, A. Mora, J. Pereda, R. P. Aguilera, **P. Poblete** and S. Neira, "Computationally Efficient MPC for Modular Multilevel Matrix Converters Operating With Fixed Switching Frequency," in IEEE open j. Ind. Electron., vol. 4, pp. 748-761, 2023, doi: 10.1109/OJIES.2023.3347101.

6. S. Langarica, G. Pizarro, **P. Poblete**, F. Radrigán, J. Pereda, J. Rodriguez and F. Núñez "Denoising and Voltage Estimation in Modular Multilevel Converters Using Deep Neural-Networks," in IEEE Access, vol. 8, pp. 207973-207981, 2020, doi: 10.1109/ACCESS.2020.3038552.

Contribution in Related Conference Papers

1. [**Best Conf. Paper Award**] **P. Poblete**, Y. Syasegov, M. Farhangi, R. P. Aguilera, Y. P. Siwakoti, D. Lu and J. Pereda, "Optimal Switching Sequence Direct Power Control for AC/DC Converters with Enhanced Converter Model for Lower Switching Frequencies," 2022 32nd Australasian Universities Power Engineering Conference (AUPEC), Adelaide, Australia, 2022, pp. 1-6, doi: 10.1109/AUPEC58309.2022.10215587.

2. F. Rubio, J. Pereda, F. Rojas and **P. Poblete**, "Hybrid Sorting Strategy for Modular Multilevel Converters With Partially Integrated 2nd Life Battery Energy Storage Systems for fast EV charging," 2022 IEEE 7th Southern Power Electronics Conference (SPEC), Nadi, Fiji, 2022, pp. 1-7, doi: 10.1109/SPEC55080.2022.10058403.

3. S. Neira, **P. Poblete**, R. Cuzmar, J. Pereda and R. P. Aguilera, "Sequential Phase-Shifted Model Predictive Control for a Multilevel Converter with Integrated Battery Energy Storage," 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Dubrovnik, Croatia, 2020, pp. 29-34, doi: 10.1109/PEDG48541.2020.9244410.

4. T. Salvadores, J. Pereda and **P. Poblete**, "Inter-Cluster Power Control of Modular Multilevel Converters with Integrated Battery Energy Storage for Electric Vehicle Low Voltage Operation," 2022 IEEE 7th Southern Power Electronics Conference (SPEC), Nadi, Fiji, 2022, pp. 1-6, doi: 10.1109/SPEC55080.2022.10058272.

5. **P. Poblete**, S. Neira, R. Cuzmar, R. P. Aguilera, A. Mora and J. Pereda, "Closed-Loop Performance Improvement for MMCs Based on Optimal Reference Governor," 2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia), Singapore, 2021, pp. 2292-2297, doi:10.1109/ECCE-Asia49820.2021.9479378.

6. S. Neira, **P. Poblete**, J. Pereda and F. Nuñez, "Consensus-Based Distributed Control of a Multilevel Battery Energy Storage System," 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), Aalborg, Denmark, 2020, pp. 1-7, doi: 10.1109/COMPEL49091.2020.9265850.

7. **P. Poblete**, J. Pereda, F. Nuñez and R. P. Aguilera, "Distributed Current Control of Cascaded Multilevel Inverters," 2019 IEEE International Conference on Industrial Technology (ICIT), Melbourne, VIC, Australia, 2019, pp. 1509-1514, doi: 10.1109/ICIT.2019.8755239.

1.6 Thesis Structure

This thesis is structured into five chapters. The remaining chapters are summarized as follows:

- **Chapter 2** analyzes the limitations of using the conventional PS-PWM strategy and recent variable-angle PS-PWM techniques for the CHB converter in SL-BESS applications. A theoretical analysis is carried out to show that the inter-SM power imbalance results in undesired switching harmonic components appearing in the CHB converter output voltage. These harmonic components emerge at the double of the PWM carrier frequency and its multiples. Consequently, this chapter proposes an OVA-PS-PWM strategy to improve the CHB converter harmonic performance for SL-BESS applications. The proposed OVA-PS-PWM introduces a bilinear dynamic model that describes the impact of the PS-angles over the CHB output voltage harmonics. This model is then employed to formulate an optimal control problem that

minimizes the output voltage harmonic distortion. An analytical optimal solution for a PS-angle update rule that applies to CHB converters of any number of cells is derived. As a result, the proposed OVA-PS-PWM updates each PS-angle at every sampling instant, significantly improving the harmonic content of the CHB output voltage even under severely unbalanced operation scenarios. Simulation results are provided to assess the performance of the proposed OVA-PS-PWM against existing variable-angle PS-PWM strategies. Moreover, experimental results verify the effectiveness of the proposed optimal modulation strategy with a single-phase CHB converter with nine SMs.

- **Chapter 3** analyzes one of the major challenges of implementing optimal control strategies for the CHB converter in practical applications, which is dealing with parameter uncertainty and external disturbances. Indeed, the steady-state performance of these control strategies deteriorates if the CHB converter model has parameter mismatches and/or SM capacitor voltage ripples are not measured. Moreover, these issues can be exacerbated in SL-BESS due to changes in their model parameters due to battery aging. Accordingly, this chapter presents the proposed KF harmonic compensator to eliminate the steady-state error and undesired low-frequency harmonic components in the CHB converter currents. The proposed KF strategy estimates the instantaneous arm voltage harmonics representing the converter modeling errors and unaccounted disturbances. Then, these estimated voltage harmonics are used to improve the arm current predictions and obtain a compensation term for the steady-state arm voltage references to be used by the optimal control strategy. Experimental results for three different optimal control schemes are provided for a three-phase CHB-SL-BESS prototype with nine SMs to confirm the effectiveness of the proposed KF strategy.

- **Chapter 4** reviews the SoC dynamic model of BPs directly connected to the CHB converter SMs. The dynamic model is analyzed and represented by transforming the arm current and modulating signals into the single-phase rotating synchronous dq-frame. As a result, the coupling between the inter-arm and inter-SM power imbalances becomes explicit in the resulting SoC dynamic model. In addition, the proposed DS-MPC strategy for SoC balancing in a three-phase CHB-SL-BESS is

presented in this chapter. The proposed DS-MPC scheme obtains optimal charge and discharge currents for each SLB-SM by manipulating the SM modulating signals and the Δ-CHB circulating current reference in the rotating synchronous dq-frame. Moreover, the proposed DS-MPC strategy incorporates maximum current ratings and the converter modulation constraints in its formulation, ensuring the safe operation of the SL-BESS. Guidelines on how to design the proposed DS-MPC strategy are provided. Additionally, experimental results are presented to verify the effectiveness of the combined implementation of the proposed OVA-PS-PWM, KF harmonic compensator, and DS-MPC strategy for the CHB-SL-BESS prototype composed of Lithium-ion SLB packs of different capacities.

- **Chapter 5** summarizes the findings of the work at hand and presents the conclusions and achievements of this doctoral thesis. Additionally, directions for future research are suggested.

Finally, given the summary above of each chapter, the correlation between them, the journal publications, and the contributions of this thesis are presented in Table 1.1.

Table 1.1: Correlation between publications, chapters, and contributions.

Publication	Chapter	Description	Contribution			
			1	2	3	4
TIE.2024.3370998	2	Predictive OVA-PS-PWM	✓	✓		
TPEL.2024.3472451	3	KF harmonic compensator for SL-BESS			✓	
TPEL.2024.3461749	4	DS-MPC for SoC balance in SL-BESS				✓

Chapter 2

Optimal Variable-Angle PS-PWM Strategy for CHB Converters Operating with Inter-SM Power Imbalance

2.1 Introduction

As mentioned in chapter 1, several modulation techniques have been proposed for the CHB converter, including the PS-PWM, the level-shifted PWM [87], NLC modulation [79], and also space-vector PWM strategies [88]. However, PS-PWM is typically chosen as the preferred modulation method for the CHB converter [74].

The advantages of the PS-PWM technique include its superior harmonic performance due to a multiplicative effect in the converter output voltage and current switching frequency. Accordingly, for SMs operated with the same dc voltage and power, and a carrier frequency of f_c, the converter output waveforms will exhibit an apparent switching frequency equal to $2nf_c$, with n the total number of series-connected SMs.

The basic working principle of PS-PWM for the CHB converter is shown in Fig. 2.1. This modulation technique applies the unipolar PWM with triangular carriers to each H-Bridge SM. In addition, a PS-angle is applied to each carrier with respect to the first carrier in order to increase the output voltage apparent switching frequency. The conventional

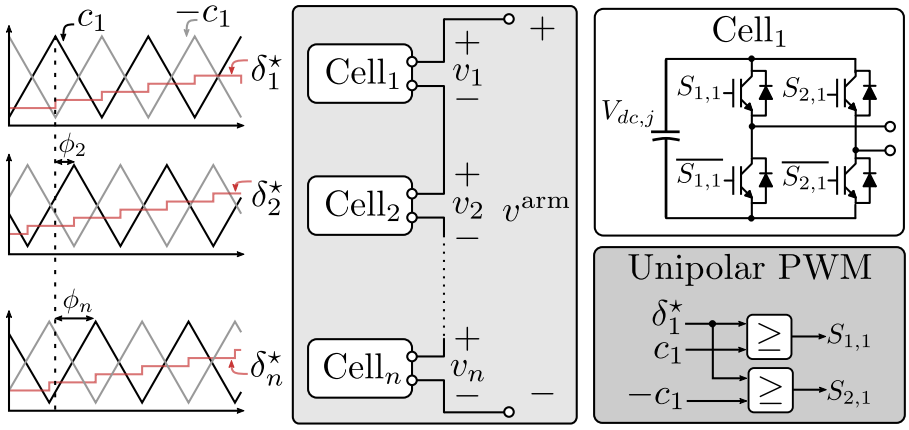


Figure 2.1: CHB converter arm with n SMs using PS-PWM with unipolar modulation.

PS-PWM method imposes fixed carrier PS-angles given by:

$$\phi_j = (j-1)\frac{\pi}{n}, \quad \forall \ j \in \{1, \ldots, n\}. \tag{2.1}$$

In CHB-SL-BESS [65], and in solar PV systems operating under partial shading [32], [89], an unbalanced operation among the H-bridge SMs for extended periods of time is required. This means that certain SMs must operate with unequal dc-voltages and/or different ac-voltage references. In solar PV systems, this inter-SM power imbalance is often necessary to achieve independent maximum power point tracking for each PV string connected to its respective power SM [89]. In the case of SL-BESS, an unbalanced operation is required to balance the SoC among individual BPs or due to disparities in the nominal voltage of these packs.

However, the conventional PS-PWM technique loses its multiplicative effect over the apparent switching frequency of the output voltage when the CHB converter operates under unbalanced conditions. In fact, significant harmonic distortion appears in the CHB converter output voltage at twice the carrier frequency and its multiples [90], negatively impacting its output power quality.

As a consequence, several modified PS-PWM techniques have been proposed to eliminate the harmonic distortion at $2f_c$ for three-SM CHB converters that must operate with an inter-SM power imbalance. In [91], a complete fundamental period of the CHB output voltage is analyzed using a Double Fourier Transform to compute constant PS-angles that reduce the weighted total harmonic distortion (WTHD). Nevertheless, this approach

only considers unequal dc-link voltages without analyzing the case of different ac-voltage references for the H-bridge SMs. This case is considered in [92], using a similar modeling framework. The experimental results show that fixed PS-angles cannot completely eliminate side harmonic bands at $2f_c$ if different ac modulating voltages are required for some SMs.

An alternative approach based on an analytic solution to a non-linear system of equations derived from the Fourier Series is proposed in [83], introducing a variable-angle PS-PWM (VA-PS-PWM) technique. This proposal is compared with previous ones in [93], achieving the smallest WTHD in the output voltage waveform. However, the analytic solution related to this method only exists for certain imbalance levels among SMs, in which the distortion at $2f_c$ can be completely eliminated. Therefore, this method cannot cover the complete operational range of the converter as the PS-angle solutions become undetermined under highly unbalanced operation scenarios.

Finding an analytical solution to cancel the low-frequency switching harmonics becomes substantially complex for CHB converters with a larger number of SMs [94]. Consequently, iterative search algorithms for PS-angles are preferred for converters with more than three SMs [90]. In [95], an offline particle swarm optimization is applied to find fixed PS-angles for SMs with different dc-voltages but similar ac-modulating voltages. Nevertheless, the computational complexity of this method and memory requirements limit its real-time implementation. A genetic algorithm to search for fixed PS-angles for a generic CHB converter is proposed in [85]. This algorithm is experimentally tested in a CHB converter of four, five, and six SMs. Although this method can be implemented in real-time using a dual-core control platform, its performance is not optimal, as fixed PS-angles cannot completely mitigate harmonic sidebands, and they limit the dynamic performance of the method to the output voltage fundamental frequency. Finally, an extension to the VA-PS-PWM for CHB converters with more than three SMs is introduced in [84]. This method imposes some conditions for the PS-angles to simplify the non-linear equation system and, thus, apply an analytical solution similar to [83]. In this sense, the H-bridge SMs are sorted into small groups of three or four SMs. Then, the solution for PS-angles for every possible group combination is evaluated, and the combination that provides the best results is kept. Despite higher-order switching harmonics can be reduced for some group combinations, this method is formulated to eliminate the harmonic distortion located only at $2f_c$. Besides,

its dynamic performance depends on the time required to find the best group combination among all the possible solutions.

In order to provide a suitable PS-PWM technique for CHB-SL-BESS applications that can contain heterogeneous BPs connected to its SMs, this chapter proposes a novel predictive optimal variable-angle PS-PWM (OVA-PS-PWM) strategy. The proposed OVA-PS-PWM strategy mitigates the low-frequency switching harmonic distortion in the CHB converter output voltage, even when the converter is operating under highly unbalanced conditions. In this way, the proposed OVA-PS-PWM provides excellent harmonic performance without the need to increase the PS-PWM carrier frequency in SL-BESS applications.

Firstly in this chapter, a discrete-time dynamic model is derived to predict the future behavior of the converter output voltage harmonics, considering the PS-angle variations as the control input. Then, this model is used to formulate a quadratic optimization problem to minimize the harmonic distortion of the CHB converter output voltage. As a result, an analytical unconstrained solution for an optimal PS-angle update rule is obtained. Notably, this unconstrained solution simplifies the implementation of the predictive OVA-PS-PWM by avoiding complex calculations to search for suitable PS-angles, even for CHB converters with a large number of SMs. Furthermore, this solution extends beyond merely canceling a single harmonic component at $2f_c$, since the optimal problem is formulated to minimize harmonic components up to $2(n-1)f_c$. Finally, the proposed predictive OVA-PS-PWM can provide feasible PS-angle solutions across the entire operational range of the converter, significantly enhancing its output voltage WTHD even in cases of severe inter-SM power imbalances.

2.2 Frequency Analysis of the CHB Converter Output Voltage Switching Harmonic Components

To analyze the switching harmonic distortion at the CHB converter output voltage, firstly, the output voltage of the j-st SM is represented with the Fourier Series as follows:

$$v_j(t) = \frac{a_{0j}(t)}{2} + \sum_{h=1}^{\infty} v_{hj}(t), \tag{2.2}$$

$$v_{hj}(t) = a_{hj}(t)\cos(h\omega t + h\phi_j) + b_{hj}(t)\sin(h\omega t + h\phi_j), \tag{2.3}$$

where the fundamental frequency ω is equal to $2\pi 2f_c$ due to the unipolar modulation of the H-bridge SMs. Additionally, a_{hj}, and b_{hj} are the Fourier coefficients of each harmonic component, and ϕ_j is the PS-angle of the PWM carrier of the SM-j in relation to the reference PWM carrier, which in this work is considered to be associated to the SM-1.

Assuming even symmetry to compute the Fourier coefficients, $b_{hj} = 0$, whereas a_{0j} and a_{hj} are given by:

$$a_{0j}(t) = \frac{1}{T_c}\int_{\frac{-T_c}{2}}^{\frac{T_c}{2}} v_j(t)dt = 2V_{dc,j}\delta_j^{\star}(t), \tag{2.4}$$

$$a_{hj}(t) = \frac{1}{T_c}\int_{\frac{-T_c}{2}}^{\frac{T_c}{2}} v_j(t)\cos(h\omega t)dt = \frac{2V_{dc,j}}{h\pi}\sin(h\pi\delta_j^{\star}(t)), \tag{2.5}$$

respectively, with $\delta_j^{\star}(t) \in [-1, 1]$ the ac-modulating signal of the H-bridge SM-j. Note that since the fundamental frequency considered in this analysis is the equivalent output switching frequency of an H-bridge SM, $2f_c$, (2.4) is related to the desired ac-voltage reference of the SM, while (2.5) is related to the switching harmonic components that can increase the harmonic distortion of the CHB converter output voltage.

As a consequence, the harmonic distortion in the output voltage of the CHB converter with n SMs connected in series can be determined for each frequency component as:

$$v_h^{\text{arm}}(t) = \sum_{j=1}^{n} v_{hj}(t). \tag{2.6}$$

The conventional PS-PWM is designed to operate the converter under balanced conditions. Thus, $a_{hj}(t) = a_h(t)\ \forall\ j$. In this way, by using the conventional fixed PS-angle def-

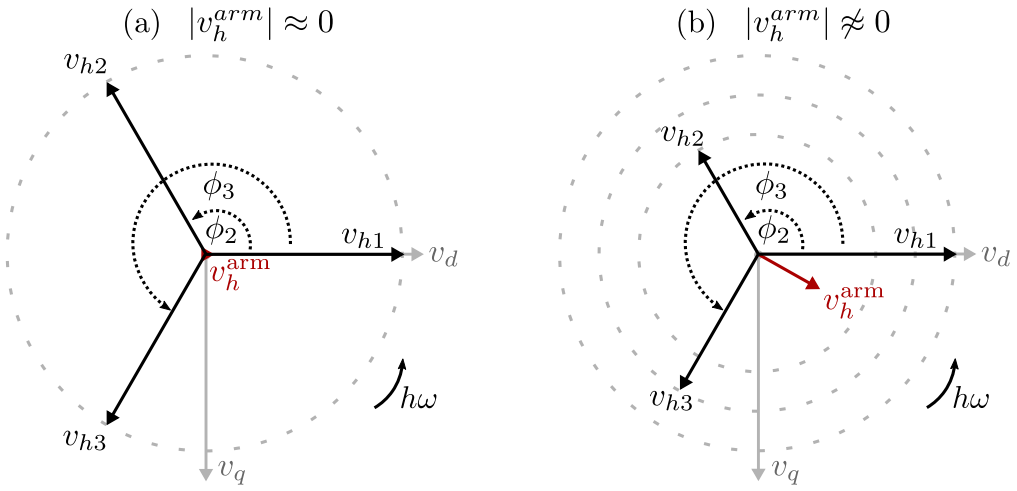


Figure 2.2: Representation of the h-st output voltage harmonic component for a 3-SM CHB converter in the rotating synchronous dq-frame for conventional PS-angles. (a) balanced operation, (b) unbalanced operation.

inition (2.1), the switching harmonic distortion $v_h^{\text{arm}}(t) = 0 \; \forall \; h \in \{1, 2, \ldots, n-1\}$. Therefore, the conventional PS-PWM exhibits a multiplicative effect in the apparent switching frequency for the CHB converter output voltage.

Nevertheless, this harmonic cancellation benefit is lost in CHB-SL-BESS applications if the converter works under an unbalanced operation. In such cases, the dc-voltages and/or ac-modulating signals of SMs differ, resulting in unequal values for $a_{hj}(t)$. As a result, the conventional PS-angles cannot achieve the cancellation of the first $(n-1)$ switching harmonic components in the CHB converter output voltage. This issue is illustrated in Fig. 2.2 by representing the h-st harmonic component of the output voltage of each SM as voltage vectors in the rotating synchronous dq-frame for a CHB converter of three SMs.

Considering the aforementioned points, the main goal of VA-PS-PWM strategies is to reduce the arm output voltage harmonic distortion at the lower switching frequencies by searching for suitable PS-angles for each SM. In this sense, PS-angles can be modified at each sampling instant to rotate the harmonic voltage vectors of each SM shown in Fig. 2.2, compensating for the magnitude differences of these harmonic components.

2.3 Proposed Predictive Optimal VA-PS-PWM

This section introduces the proposed predictive OVA-PS-PWM, which improves the harmonic distortion of the CHB converter output voltage under unbalanced operation conditions. The proposed modulation strategy achieves this objective by finding the optimal PS-angles updates that minimize the weighted harmonic components of the CHB converter output voltage in the synchronous dq-frame.

2.3.1 Continuous-time Dynamic Model of the CHB Converter Switching Harmonic Components in the Synchronous dq-Frame

Based on (2.3) and considering that the Fourier coefficients b_{hj} are zero, the h-th voltage harmonic component of the SM-j in the single-phase $\alpha\beta$-frame is given by:

$$v_{hj}^{\alpha}(t) = a_{hj}(t)\cos(h\omega t + h\phi_j), \tag{2.7}$$

$$v_{hj}^{\beta}(t) = a_{hj}(t)\sin(h\omega t + h\phi_j). \tag{2.8}$$

These voltages can be transformed into the synchronous dq-frame by assuming the output voltage of SM-1 as the reference rotating voltage. In this way, applying the Park's transform and assuming the phase displacement angle $\phi_1 = 0$ leads to:

$$\begin{aligned} v_{hj}^{d}(t) &= -a_{hj}(t)\sin(h\phi_j), \\ v_{hj}^{q}(t) &= a_{hj}(t)\cos(h\phi_j). \end{aligned} \tag{2.9}$$

Therefore, the amplitude of the arm output voltage h-th harmonic component can be computed as follows:

$$(v_h^{\text{arm}}(t))^2 = (v_h^{d,\text{arm}}(t))^2 + (v_h^{q,\text{arm}}(t))^2, \tag{2.10}$$

with

$$v_h^{d,\text{arm}}(t) = \sum_{j=1}^{n} v_{hj}^{d}(t), \quad v_h^{q,\text{arm}}(t) = \sum_{j=1}^{n} v_{hj}^{q}(t). \tag{2.11}$$

Minimizing (2.10) for $h \in \{1, \ldots, n-1\}$ improves the voltage total harmonic distortion

(THD). However, considering this continuous-time model to find suitable PS-angles requires solving a non-linear system of equations, which becomes challenging for more than three SMs [94]. The following section introduces a novel bilinear discrete-time dynamic model to solve this issue as an optimal quadratic problem.

2.3.2 Proposed Discrete-time Dynamic Model for PS-angle Updates

The proposed OVA-PS-PWM is designed to be implemented using a digital modulation stage. As a consequence, the PS-angles and the ac-modulating signals are updated at a fixed frequency and remain constant within sampling instants. Thus, the discrete-time representation of (2.9) with a variable PS-angle can be expressed via:

$$v_{hj}^{d}(k) = -a_{hj}(k)\sin(h\phi_j(k)), \tag{2.12}$$

$$v_{hj}^{q}(k) = a_{hj}(k)\cos(h\phi_j(k)). \tag{2.13}$$

When the angle of a given SM-j, $\phi_j(k)$ is modified, so does the harmonic components $v_{hj}^{d}(k)$ and $v_{hj}^{q}(k)$. In this sense, the future values for the SM harmonic components can be represented by adding an angle variation $\Delta\phi_j(k)$ to $\phi_j(k)$. This PS-angle update can be represented by the following discrete-time dynamic model:

$$v_{hj}^{d}(k+1) = -a_{hj}(k)\sin(h\phi_j(k) + h\Delta\phi_j(k)), \tag{2.14}$$

$$v_{hj}^{q}(k+1) = a_{hj}(k)\cos(h\phi_j(k) + h\Delta\phi_j(k)). \tag{2.15}$$

These equations can be expanded by invoking the angle addition trigonometry identity. Taking $v_{hj}^{d}(k+1)$ as example leads to:

$$\begin{aligned} v_{hj}^{d}(k+1) = &- a_{hj}(k)\sin(h\phi_j(k))\cos(h\Delta\phi_j(k)) \\ &- a_{hj}(k)\cos(h\phi_j(k))\sin(h\Delta\phi_j(k)), \end{aligned} \tag{2.16}$$

Replacing (2.12)-(2.13) into (2.16), and following the same procedure for $v_{hj}^{q}(k+1)$

allows one to express the discrete-time dynamic model as

$$v_{hj}^{d}(k+1) = v_{hj}^{d}(k)\cos(h\Delta\phi_j(k)) - v_{hj}^{q}(k)\sin(h\Delta\phi_j(k)), \tag{2.17}$$

$$v_{hj}^{q}(k+1) = v_{hj}^{q}(k)\cos(h\Delta\phi_j(k)) + v_{hj}^{d}(k)\sin(h\Delta\phi_j(k)). \tag{2.18}$$

At every sampling instant, the H-bridge ac-modulating signal or dc-voltage can be modified, and new PS-angles might be required to mitigate the arm voltage harmonic distortion. However, when the CHB converter operates in steady-state, only minor angle variations are usually needed between two consecutive sampling instants, as both dc-voltages and ac-modulating signals do not change drastically during this time interval.

Accordingly, if the angle update $\Delta\phi_j(k)$ is relatively small, the small angle approximation $\sin(h\Delta\phi_j(k)) \approx h\Delta\phi_j(k)$ and $\cos(h\Delta\phi_j(k)) \approx 1$ can be used to linearize (2.17) and (2.18) without a significant loss of accuracy. Replacing this approximation into (2.17) and (2.18) leads to the following expressions to describe the PS-angle update of the h-th harmonic component of SM-j:

$$\boldsymbol{v}_{hj}^{dq}(k+1) = \boldsymbol{v}_{hj}^{dq}(k) + h\boldsymbol{M}\boldsymbol{v}_{hj}^{dq}(k)\Delta\phi_j(k), \tag{2.19}$$

$$\boldsymbol{v}_{hj}^{dq}(k) = \begin{bmatrix} v_{hj}^{d}(k) \\ v_{hj}^{q}(k) \end{bmatrix}, \quad \boldsymbol{M} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}. \tag{2.20}$$

As follows, (2.19) can be used to create a bilinear discrete-time model that describes the effect of updating the PS-angle of SM-j over the h-th harmonic component of the CHB converter output voltage:

$$\boldsymbol{x}_h(k+1) = \boldsymbol{x}_h(k) + \boldsymbol{B}_h(\boldsymbol{x}_{hj}(k))\Delta\phi_j(k), \tag{2.21}$$

with

$$\boldsymbol{x}_h(k) = \boldsymbol{v}_h^{dq,\mathrm{arm}}(k) = \begin{bmatrix} \sum_{i=2}^{n} v_{hi}^{d}(k) & a_{h1}(k) + \sum_{i=2}^{n} v_{hi}^{q}(k) \end{bmatrix}^T,$$

$$\boldsymbol{B}_h(\boldsymbol{x}_{hj}(k)) = h\boldsymbol{M}\boldsymbol{v}_{hj}^{dq}(k) \in \mathbb{R}^2.$$

Then, (2.21) can be used to define an augmented state vector $\boldsymbol{x}(k) = \begin{bmatrix} \boldsymbol{x}_1^T(k) & \dots & \boldsymbol{x}_{n-1}^T(k) \end{bmatrix}^T \in$

$\mathbb{R}^{2(n-1)}$ that includes the first $n-1$ switching harmonic components of the CHB converter output voltage. In this way, the dynamic model for this augmented state vector is given by:

$$\boldsymbol{x}(k+1) = \boldsymbol{x}(k) + \boldsymbol{B}(\boldsymbol{x}_j(k))\Delta\phi_j(k), \tag{2.22}$$

where,

$$\boldsymbol{B}(\boldsymbol{x}_j(k)) = \begin{bmatrix} (\boldsymbol{B}_1(\boldsymbol{x}_{1j}))^T & \dots & (\boldsymbol{B}_{(n-1)}(\boldsymbol{x}_{(n-1)j}))^T \end{bmatrix}^T \in \mathbb{R}^{2(n-1)} \tag{2.23}$$

The model (2.22) resembles a standard discrete-time dynamic model that can be used to obtain future predictions of the first $n-1$ voltage harmonic components, based on the influence of individual angle variations, $\Delta\phi_j(k)$. The next section introduces the proposed sequential predictive optimal control problem that allows the calculation of PS-angle updates for each SM carrier by using this model.

2.3.3 Sequential Optimal Control Problem

In this section, the associated optimal predictive control problem of the OVA-PS-PWM is formulated to minimize the undesired switching harmonic components in the CHB converter output voltage. In order to tackle this control objective, a standard quadratic cost function for a predictive controller is introduced:

$$J_j(k) = \underbrace{\boldsymbol{x}^T(k+1)\boldsymbol{Q}\boldsymbol{x}(k+1)}_{J_{\lambda\text{THD}}(k)} + \lambda_u \Delta\phi_j(k)^2, \tag{2.24}$$

where $\boldsymbol{Q} = \text{diag}(\lambda_1 \boldsymbol{I}_2, \dots, \lambda_{n-1}\boldsymbol{I}_2)$, is the weighing matrix to penalize the switching harmonic distortion of the CHB output voltage. Besides, note that $J_{\lambda\text{THD}}(k)$ is equivalent to the following WTHD cost function:

$$J_{\lambda\text{THD}}(k) = \sum_{h=1}^{n-1} \lambda_h ((v_h^{d,\text{arm}}(k+1))^2 + (v_h^{q,\text{arm}}(k+1)^2)). \tag{2.25}$$

In this way, the weighing factors λ_h can be used to prioritize mitigating specific switching harmonic components in the CHB output voltage. For instance, selecting $\lambda_h = \frac{1}{h}$, with $h =$

$\{1,\ldots,n{-}1\}$, favors the minimization of the lower harmonics over higher order harmonics.

Similarly to a standard predictive control strategy, the weighing factor λ_u penalizes the step changes in the PS-angle. Thus, λ_u regulates how aggressively the PS-angle can change at each sampling instant to reduce the undesired harmonic distortion. As a result, this weighing factor can be used to enforce that $\Delta\phi_j$ remains small, maintaining the accuracy of the linearized prediction model.

The optimal PS-angle update for SM-j is the one that minimizes the cost function (2.24), i.e.:

$$\Delta\phi_j^{\text{opt}}(k) = \arg\left\{\min_{\Delta\phi_j(k)\in\mathbb{R}} J_j(k)\right\}. \tag{2.26}$$

Then, the unconstrained solution to this problem can be obtained directly by simply performing the derivative $\frac{dJ_j(k)}{d\Delta\phi_j(k)} = 0$, which leads to the following expression:

$$\Delta\phi_{j,\text{unc}}^{\text{opt}}(k) = -(\boldsymbol{H}(k))^{-1}\boldsymbol{F}(k), \tag{2.27}$$

with

$$\begin{aligned}\boldsymbol{H}(k) &= \boldsymbol{B}^T(\boldsymbol{x}_j(k))\boldsymbol{Q}\boldsymbol{B}(\boldsymbol{x}_j(k)) + \lambda_u,\\ \boldsymbol{F}(k) &= \boldsymbol{B}^T(\boldsymbol{x}_j(k))\boldsymbol{Q}\boldsymbol{x}(k).\end{aligned} \tag{2.28}$$

Moreover, by replacing (2.28) into (2.27), the following analytic solution for the optimal update of the j-st PS-angle of a generic CHB converter with n SMs is obtained:

$$\Delta\phi_{j,\text{unc}}^{\text{opt}}(k) = \frac{\sum_{h=1}^{n-1} h\lambda_h a_{hj}(k)\left(d_{hj}^d(k)\cos(h\phi_j(k)) + d_{hj}^q(k)\sin(h\phi_j(k))\right)}{\lambda_u + \sum_{h=1}^{n-1}\lambda_h(ha_{hj}(k))^2}, \tag{2.29}$$

and

$$d_{hj}^d(k) = \sum_{\substack{i=2\\ i\neq j}}^{n} v_{hi}^d(k), \quad d_{hj}^q(k) = a_{h1}(k) + \sum_{\substack{i=2\\ i\neq j}}^{n} v_{hi}^q(k). \tag{2.30}$$

As shown in the cost function (2.24), the proposed predictive OVA-PS-PWM must consider only one step as the prediction horizon to have an analytic unconstrained solution.

This requirement arises from the bilinear nature of the prediction model (2.22). Accordingly, longer prediction horizons would require a numeric optimization solver to determine the optimal solution, which significantly increases the complexity of the optimal PS-angle search.

The proposed model (2.22) used to obtain this solution was derived assuming small changes in the PS-angles. As a consequence, when the solution (2.29) violates this assumption, simple scalar saturation of $\Delta\phi^{\text{opt}}_{j,\text{unc}}(k)$ is considered in this work, with a maximum PS-angle step of 10°, i.e.:

$$\Delta\phi^{\text{opt}}_{j,\text{sat}}(k) = \max\left\{\min\left\{\Delta\phi^{\text{opt}}_{j,\text{unc}}(k), \frac{10\pi}{180}\right\}, -\frac{10\pi}{180}\right\}. \tag{2.31}$$

Accordingly, (2.31) can be sequentially computed to update each SM PS-angle, improving the CHB converter harmonic distortion after each evaluation.

It is important to highlight that if the unconstrained optimal solution (2.27) is within ±10°, the unconstrained solution (2.27) is in fact the optimal solution. This result is usually obtained during steady-state operation, in which the PS-angles exhibit a small variation between consecutive sampling instants.

On the other hand, when the power references of each CHB converter SM are modified, a significant change in the carrier angles might be required. In this case, a saturation of the PS-angles might occur until these angles become closer to the optimal values. Favorably, this does not significantly affect the converter power quality performance. The reason for this is twofold – the proposed predictive OVA-PS-PWM takes only a few sampling instants to converge to the optimal angles, and harmonic distortion is not defined during transients. Moreover, changing the PS-angles does not affect the current control if the VA-PWM strategy is implemented with the sampling technique [72].

Due to the small angle approximation applied to derive the proposed discrete-time dynamic model, the optimal PS-angle update rule cannot offer global optimality guarantees. Besides, the global optimal PS-angles solution that minimizes the arm switching harmonic distortion is not unique. For instance, swapping the PS-angles of cell-2 and cell-3 in Fig. 2.2(a) would also cancel the individual h-st voltage harmonic components in the resulting arm output voltage. In this sense, the weighing factor λ_u plays a crucial role in the stability of the proposed predictive OVA-PS-PWM, avoiding the recurrent saturation of the

PS-angle updates and the oscillation of the optimal PS-angles between local minimums.

2.3.4 Proposed predictive OVA-PS-PWM Algorithm

The proposed predictive OVA-PS-PWM is detailed in Algorithm 1. This algorithm is divided into two main steps. The first step considers each H-bridge dc-voltage and ac-modulating signal to compute the Fourier coefficients for each harmonic component that needs to be minimized. The second step is to use these Fourier coefficients to compute the optimal PS-angle updates, evaluating the previously derived analytic solution sequentially for each SM. This step can then be repeated for a given number of iterations, n_{iter}, to allow the PS-angles to update multiple times. In this way, the PS-angles can converge to optimal angles that might require updates larger than 10° at every sampling instant.

Finally, note that ϕ_j represents the phase displacement between the carriers of SM-j and SM-1. Consequently, the PS-angles must be divided by two before applying them to a modulator operating in double-update mode.

Algorithm 1: OVA-PS-PWM

1) Compute the Fourier Coefficients
for j = *1:n* **do**
  for h = *1:n-1* **do**
    $a_{hj} \leftarrow \frac{2V_{dc,j}}{h\pi}\sin(h\pi\delta_j^{\star})$;
  end
end
2) Iteratate to compute optimal PS-angles sequentially **while** *counter* <= n_{iter} **do**
  for j = *2:n* **do**
    2.1) Compute latest values for d_{hj}^{d} and d_{hj}^{q}
    for h = *1:n-1* **do**
      $d_{hj}^{d} = \sum_{\substack{i=2 \\ i\neq j}}^{n} v_{hi}^{d}; \quad d_{h}^{qj} = a_{h1} + \sum_{\substack{i=2 \\ i\neq j}}^{n} v_{hi}^{q};$
    end
    2.2) Compute the optimal PS-angle update
    $\Delta\phi_{j,\text{unc}}^{\text{opt}} \leftarrow$ as per (28);
    $\Delta\phi_{j,\text{sat}}^{\text{opt}} \leftarrow \max(\min(\Delta\phi_{j,\text{unc}}^{\text{opt}}, \frac{10\pi}{180}), -\frac{10\pi}{180})$;
    2.3) Update the corresponding PS-angle
    $\phi_j \leftarrow \phi_j + \Delta\phi_{j,\text{sat}}^{\text{opt}}$;
  end
  $counter \leftarrow counter + 1$
end

2.4 Simulation Results and Benchmarking

A simulation study for a three-SM CHB converter is carried out in this section to assess the performance of the proposed predictive OVA-PS-PWM against the VA-PS-PWM strategy [83]. The latter achieves optimal PS-angles to cancel the harmonic distortion around $2f_c$ and exhibits the lowest WTHD among VA-PS-PWM techniques for three-SM CHB converters [93]. However, this method cannot cover the complete operational range of the converter, as its solution is undetermined when a large unbalance among SMs is required [83]. The OVA-PS-PWM was implemented with only three iterations. Besides, the weighing factors λ_1 and λ_u were set equal to one, whereas λ_2 was set equal to zero to prioritize only the minimization of the harmonic distortion at $2f_c$. Table 2.1 outlines the key parameters used for the simulated OVA-PS-PWM strategy, while Table 2.2 summarizes the operation conditions for each simulated case.

Table 2.1: Single-phase CHB converter and controller main parameters for the simulation results.

Description	Variable	Value
Number of H-Bridge SMs	n	3
Carrier frequency	f_c	750 Hz
Sampling frequency	f_s	1.5 kHz
Number of iterations	n_{iter}	3
Weighing factors	λ_u, λ_1, λ_2	1, 1, 0

Table 2.2: Operation conditions for the simulation results.

Case	Description	DC Voltages [V]			Modulation indexes		
		Cell_1	Cell_2	Cell_3	Cell_1	Cell_2	Cell_3
1	Unbalanced	150	165	130	0.75	0.85	0.90
2	Highly unbalanced	200	120	130	0.30	0.95	0.85
3	Clamping SM-1	140	150	150	0.75	0.90	0.85

The results for the first case are shown in Fig. 2.3(a)-(i). The proposed predictive OVA-PS-PWM converges to the same optimal solution provided by the VA-PS-PWM [83].

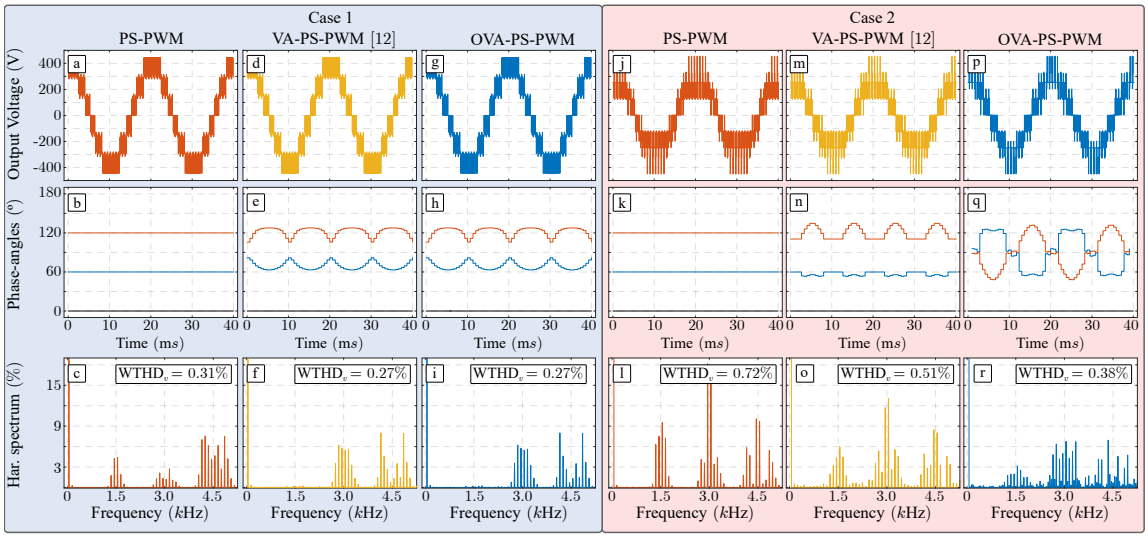


Figure 2.3: CHB output voltage, PS-angles, and voltage harmonic spectra for the simulated cases 1 and 2.

As a result, the harmonic distortion around $2f_c$ is completely mitigated, and the WTHD[1] is reduced when compared with the conventional PS-PWM.

Figure 2.3(j)-(r) shows the result for a second case, which considers a greater imbalance regarding the dc voltages and modulation indexes. Consequently, it is not feasible to fully eliminate the low switching frequency harmonic distortion for this case. However, the proposed predictive OVA-PS-PWM still provides the optimal PS-angles that minimize the harmonic content at $2f_c$, leading to a reduced voltage WTHD of 0.38%, compared with the 0.72% and 0.51% obtained by the conventional PS-PWM and the VA-PS-PWM, respectively. This result represents a clear advantage of the proposed predictive OVA-PS-PWM over the VA-PS-PWM [83], in which the obtained PS-angles must be kept constant for several sampling instants as its PS-angle solutions become undetermined due to the large SM imbalance.

A third case considering a discontinuous PWM technique that clamps the ac modulating signal of one SM [96] is also included in this benchmark. Accordingly, the performance of the proposed OVA-PS-PWM is tested when the modulator is saturated. Fig. 2.4 shows the obtained results for this case. Here, it can be seen that a 90° angle is applied between the carriers of SM-2 and SM-3 during the time interval in which the output voltage of

[1]In this chapter, the WTHD was measured considering harmonics up to 20 kHz, accounting for the high-frequency harmonic components introduced by the modulation stage.

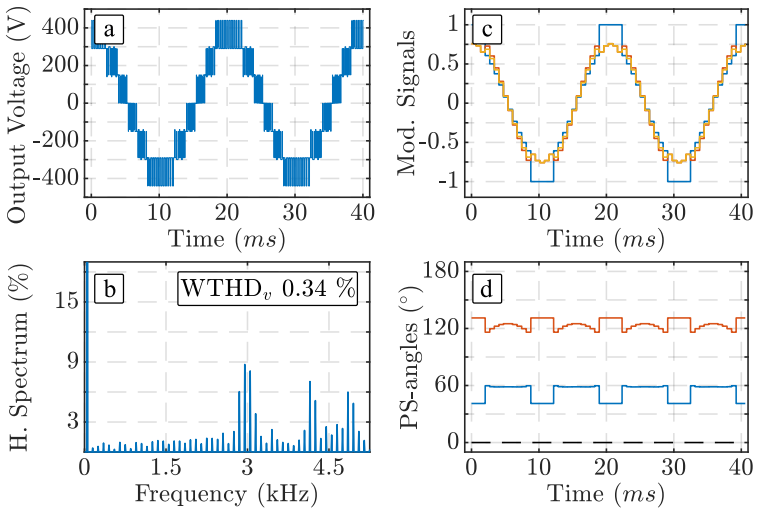


Figure 2.4: Simulation results for the proposed OVA-PS-PWM working as a discontinuous PWM technique. (a) CHB output voltage, (b) voltage harmonic spectra, (c) ac modulating signals, and (d) PS-angles.

SM-1 is being clamped. This result is consistent with [97], which shows that this phase displacement among the remaining two SMs improves the voltage WTHD when using the discontinuous PWM technique [96]. As a result, the proposed OVA-PS-PWM mitigates the low-frequency harmonic distortion at $2f_c$, showing that the proposed technique can be effectively applied to discontinuous PWM strategies.

In conclusion, the formulation of the proposed predictive OVA-PS-PWM as a model predictive control problem that minimizes the WTHD allows the calculation of optimal PS-angles for the complete operational range of the CHB converter. As a result, the proposed OVA-PS-PWM can outperform the VA-PS-PWM technique [83] when applied to CHB converters working with severe SM imbalances. Moreover, the proposed OVA-PS-PWM correctly handles the saturation of modulating signals. Thus, it can be applied to discontinuous PWM strategies.

2.5 Experimental Verification

2.5.1 Experimental Setup

Experimental results have been carried out to analyze the performance of the proposed predictive OVA-PS-PWM strategy. The experimental setup shown in Fig. 2.5 has been

used. This setup comprises a single-phase nine-SM CHB converter connected to an RL load. Isolated dc-power supplies are used to feed each H-bridge SM by connecting them directly to the SM capacitor. In particular, three SMs are fed with the EA-PSI-9750-12 variable voltage power supplies to enforce uneven dc-voltages, while the other six SMs are connected to the RSP-500-48 dc-power supplies operating at 50 V.

The proposed predictive OVA-PS-PWM was implemented on an OPAL-RT OP4510 system based on an Intel Xeon E3 v5 CPU and two Kintex-7 FPGAs. Only one CPU core was considered to implement the proposed algorithm and a current control loop, while the FPGAs were used to generate the PWM pulses. Besides, the generalized feed-forward sampling method [72] was used to implement the proposed OVA-PS-PWM with a fixed sampling frequency of 1.5 kHz. This sampling technique effectively implements variable-angle PS-PWM strategies, avoiding potential implementation problems in the microprocessor control board, such as delays and interrupt overruns. Moreover, this technique imposes a fixed sampling frequency equal to $T_c/2$, outperforming the conventional PS-PWM regarding computational burden [72]. The main parameters of the experimental setup are presented in Table 2.3.

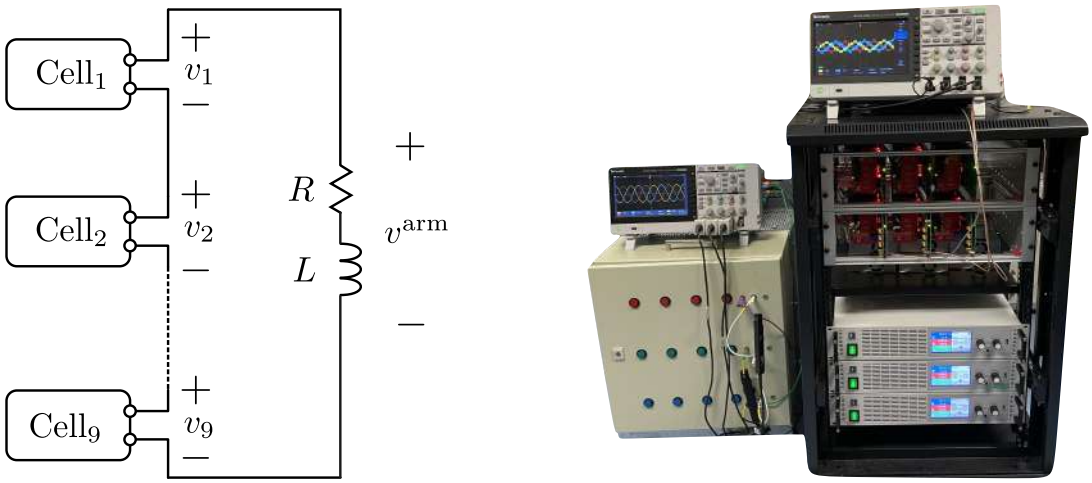


Figure 2.5: Experimental setup. (a) circuit diagram, (b) experimental setup including the single-phase nine-cell CHB converter with isolated dc power supplies to feed the dc voltages of the SMs.

Table 2.3: Single-phase CHB converter and controller main parameters for the proposed OVA-PS-PWM experimental verification.

Description	Variable	Value
Number of H-Bridge SMs	n	9
Load inductance	L	1 mH
Load resistance	R	36 Ω
Nominal SM DC-link voltage	V_{DC}	50 V
HB-SM capacitance	C	400 μF
Carrier frequency	f_c	750 Hz
Sampling frequency	f_s	1.5 kHz
Number of iterations	n_{iter}	8
Weighing factors	λ_u, λ_h	100, $\frac{1}{h}$

2.5.2 Selection of the Number of Iterations of the Proposed OVA-PS-PWM Algorithm

With an increase in the number of iterations for the proposed OVA-PS-PWM algorithm, the range in which the PS-angles can move towards a better solution also expands. This allows the proposed OVA-PS-PWM to eventually converge to a solution that does not saturate any PS-angle, which is the optimal solution to each sequential optimization problem. As previously mentioned, this optimal solution cannot guarantee global optimality, as the bilinear nature of the proposed prediction model in (2.22) leads to a non-convex optimization problem. Nevertheless, local minimum solutions can still offer excellent harmonic performance, as demonstrated in the experimental results section presented later in this chapter.

A simulation of the experimental setup was conducted to verify the impact of increasing the number of iterations of the proposed predictive OVA-PS-PWM in the CHB converter output voltage WTHD. The simulation results are shown in Fig. 2.6, confirming that the PS-angle solutions can improve by increasing the number of iterations. However, after eight iterations, the proposed PS-angle update rule converges to the optimal solution. Thus, doing more than eight iterations does not further improve the harmonic distortion. Therefore, $n_{\text{iter}} = 8$ was set for the experimental results presented in section 2.5.4.

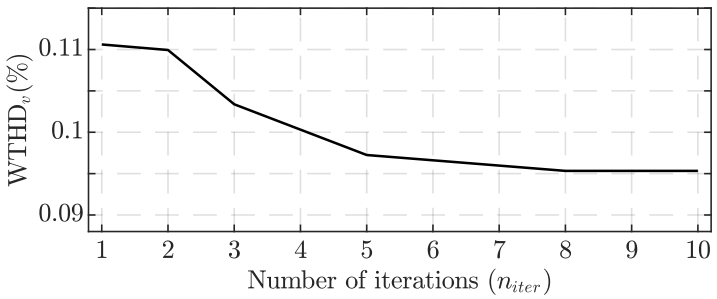


Figure 2.6: Simulation results for the impact of the number of iterations of the OVA-PS-PWM algorithm in the CHB output voltage WTHD.

2.5.3 Computational Burden

The computational cost of the proposed OVA-PS-PWM was quantified by measuring its execution time in the real-time control platform. Several experiments were conducted, varying the number of SMs and the number of iterations computed by the algorithm. Figure 2.7(a) shows the execution time in percentage of the sampling interval as a function of the number of SMs and the number of iterations. Additionally, Fig. 2.7(b) shows the increment in the execution time for eight iterations as the number of SMs increases. The execution time requirement exhibited a linear relationship for the CPU load as the number of iterations increased. Nonetheless, it showed exponential growth with the increase in the number of SMs. This behavior poses a limitation for the OVA-PS-PWM aggravated for three-phase CHB converters, which need the implementation of three independent OVA-PS-PWM algorithms[2]. However, it is important to remark that the proposed OVA-PS-PWM still provides a significant WTHD reduction even with only one iteration compared to the conventional PS-PWM fixed angles. In fact, Fig. 2.6 shows that increasing the number of iterations from one to eight only improved the output voltage WTHD by 0.015%. Thus, if necessary, the number of iterations can be diminished to reduce the computational burden of the proposed algorithm at the expense of a slightly higher WTHD.

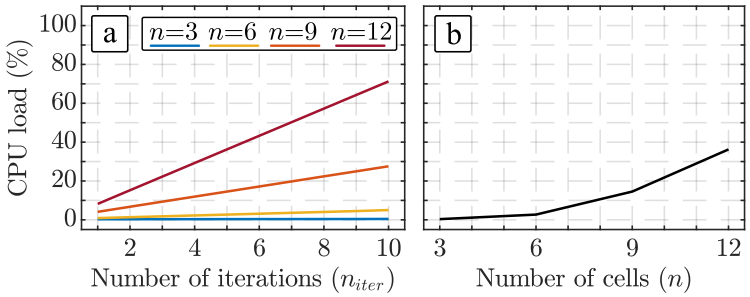


Figure 2.7: Execution time of the proposed OVA-PS-PWM in percentages of the total available time. (a) CPU load for different number of SMs and iterations, (b) CPU load for 8 iterations for different number of SMs.

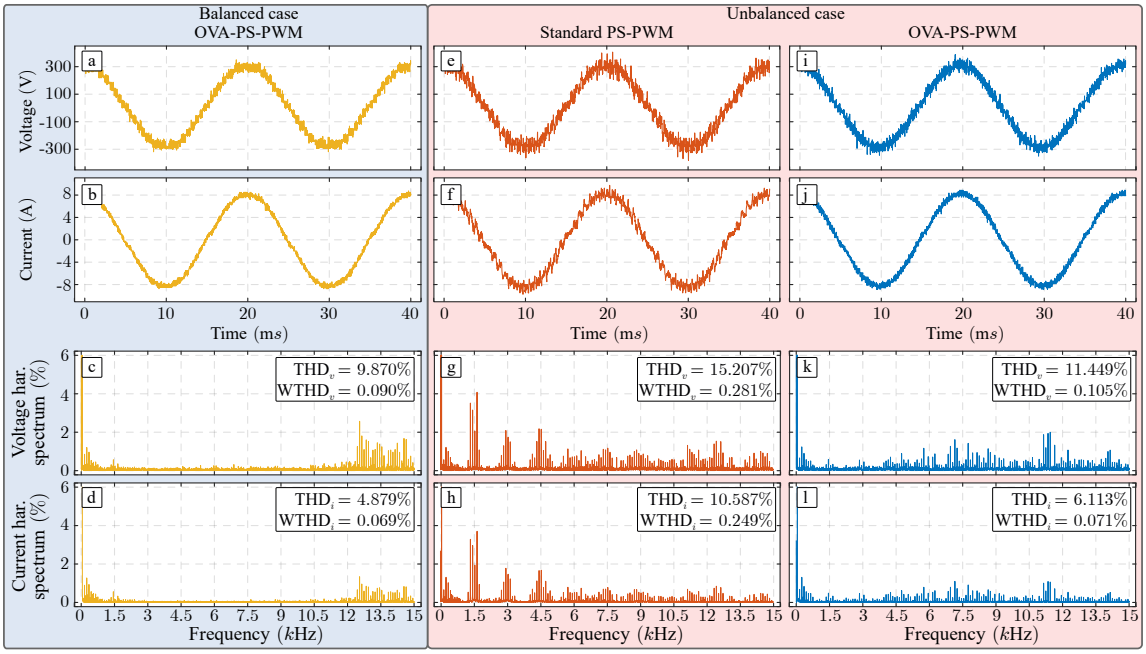


Figure 2.8: CHB output voltage and current waveforms with their corresponding harmonic spectra for three experimental tests. The left column (a, b, c and d) shows the case with balanced operation conditions for the OVA-PS-PWM, the middle column (e, f, g and h) shows the conventional PS-PWM under unbalanced operation conditions, and the right column (i, j, k and f), shows the performance of the OVA-PS-PWM for the same unbalanced operation conditions.

Table 2.4: dc-voltages for the unbalanced operation of the nine-SM CHB converter.

H-Bridge SM	1-3	4	5	6	7-9
$V_{dc,x}$ [V]	50	60	70	55	50

2.5.4 Experimental Results

Performance Under Balanced Operation Conditions

In this test, the CHB converter SMs were operated with the same dc-voltages and ac-modulating signals. Besides, the output current reference was set to 8 A. Fig. 2.8(a)-(d) shows the CHB converter output voltage and current with their respective harmonic spectrum. The proposed predictive OVA-PS-PWM mitigates the first $(n-1)$ switching harmonic components, leading to an apparent output switching frequency of $2nf_c$. Hence, the proposed OVA-PS-PWM performs similarly to the conventional PS-PWM under balanced operation conditions. In fact, the PS-angles converged to the conventional fixed PS-angles (2.1) as shown in Fig. 2.9(b), which are the known optimal PS-angles solution for the specific case of balanced operation among SMs. Furthermore, Fig. 2.9(a)-(b) shows an experiment with the PS-angles wrongly initialized at 90°, before enabling the OVA-PS-PWM algorithm at 10 ms. This test was conducted to assess the convergence speed of the proposed OVA-PS-PWM. As a result, the PS-angles reach the optimal solution after five executions of the proposed algorithm. Therefore, the proposed OVA-PS-PWM can reach optimal PS-angles with a fast dynamic response.

Performance Under Unbalanced Operation Conditions

Two experiments were conducted to compare the unbalanced operation of the CHB converter with the proposed predictive OVA-PS-PWM strategy and the conventional PS-PWM. The unbalanced operation was given by maintaining the same 8 A current reference, but applying different modulating indexes to each SM. Moreover, the dc-power supply voltages were set as shown in Table 2.4. Accordingly, this operating scenario emulated the operation of a single-phase CHB-SL-BESS with different voltage levels and inter-SM power imbalance.

[2]Note that in a three-phase converter, if the lower switching harmonics at each arm are mitigated, the corresponding harmonic distortion is also absent in the phase-to-phase output voltages.

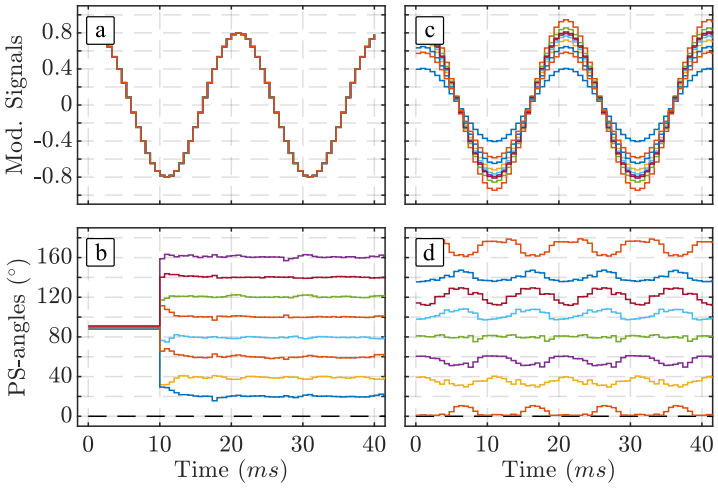


Figure 2.9: PS-angles and modulating signals for the experimental results. (a)-(b) shows the convergence of the proposed OVA-PS-PWM for the balanced case. (c)-(d) shows the steady-state signals for the unbalanced case.

Fig 2.8(e)-(h) shows the performance of conventional PS-PWM with fixed PS-angles. Despite the 19 output voltage levels of the CHB converter used in this experiment, significant voltage harmonic distortion emerged at $2f_c$, $4f_c$, and $6f_c$ due to the power imbalance within the arm. Moreover, the output inductor cannot properly filter these harmonic components (see Fig. 2.8(h)), leading to a noticeable increase in the output current ripple shown in Fig. 2.8(f).

The performance of the proposed predictive OVA-PS-PWM for the same unbalanced operation conditions is shown in Fig. 2.8(i)-(l), while the computed optimal PS-angles and modulating signals are shown in Fig. 2.9(c)-(d). In contrast with the conventional PS-PWM, the first three switching harmonic components exhibit a magnitude smaller than 1% (see Fig. 2.8(k)). In this way, it is clear that the selected weighing factors, $\lambda_h = \frac{1}{h}$, prioritize the mitigation of lower frequency harmonics over higher frequency switching components.

Furthermore, the arm output voltage THD fell by 3.758%, and the WTHD by 0.176% for the proposed OVA-PS-PWM compared to the conventional PS-PWM. As the output inductor provides major attenuation for the higher frequency harmonic components, this lower voltage harmonic distortion reduced the current WTHD by 3.5 times for the proposed OVA-PS-PWM compared to the results obtained with the conventional PS-PWM. Consequently, these results evidence the benefits of minimizing the lower frequency volt-

age harmonic components when the CHB converter SMs operate unbalanced, which might translate into a size reduction of the converter output filter [72]. Indeed, when comparing the output current harmonic distortion of the proposed OVA-PS-PWM between the balanced and the unbalanced cases, the current WTHD showed a slight increment of only 0.002%.

Transient Performance

Transient tests were carried out to verify that the proposed predictive OVA-PS-PWM does not impact the dynamic response of the converter. These results are shown in Fig. 2.10. The unbalanced dc-voltages and ac-modulating indexes of the previous experiment were maintained to impose an unbalanced operation among SMs. The output current reference was initially set at 8 A, and the OVA-PS-PWM algorithm was disabled during the first 40 ms of the experiment. As shown in Fig. 2.10(b), the current waveform is improved due to the reduction of low frequency switching ripple after the proposed OVA-PS-PWM becomes active. Moreover, this reduction of harmonic distortion is confirmed by the instantaneous cost function value $J_{\lambda\mathrm{THD}}(k)$, illustrated in Fig. 2.10(c).

Finally, step changes in the output current reference are introduced at 80 ms and 120 ms, by reducing the output current to 4 A and then increasing it again to 8 A. As shown in Fig. 2.10(a)-(b), the proposed predictive OVA-PS-PWM does not interfere with the current control. Moreover, the fast convergence to optimal PS-angles maintains a reduced value of $J_{\lambda\mathrm{THD}}(k)$ even when the operation point of the converter is modified.

In conclusion, the proposed OVA-PS-PWM can obtain excellent harmonic performance, even for unbalanced operation conditions. Moreover, the optimal PS-angle update rule can minimize several switching harmonic distortion components in the CHB output voltage. This result represents an advantage regarding previous VA-PS-PWM proposals for CHB converters with more than three-SMs [83], [84], focused on completely mitigating the harmonic content mainly at $2f_c$. Moreover, the experiments showed that the proposed predictive OVA-PS-PWM provides a fast dynamic response by requiring only a few executions to reach the optimal solution and maintaining a reduced value for the instantaneous cost function $J_{\lambda\mathrm{THD}}(k)$ even during transients.

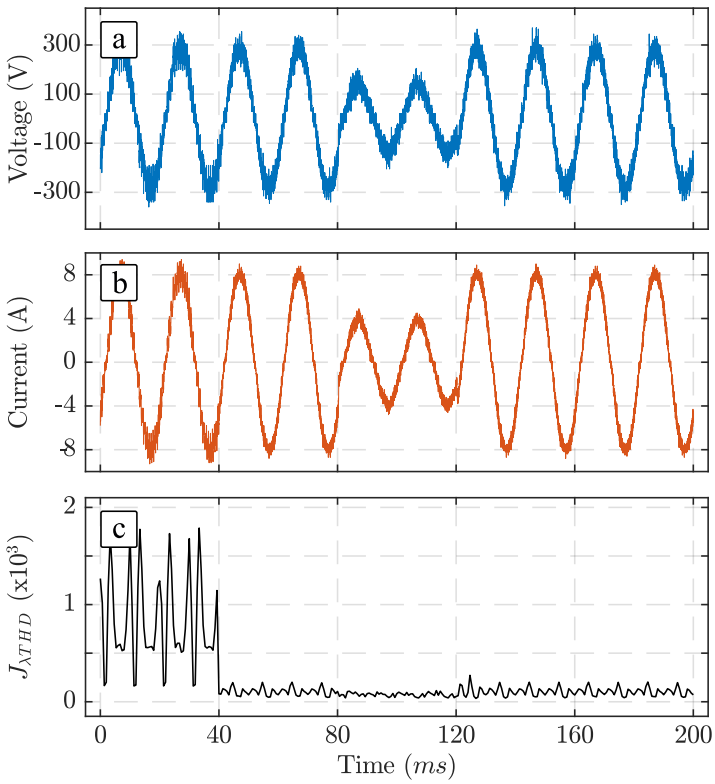


Figure 2.10: Transient response of the proposed OVA-PS-PWM after enabled at 40 ms. (a) CHB output voltage, (b) output current, (c) instantaneous cost function $J_{\lambda\text{THD}}(k)$ value.

2.6 Conclusions

In this chapter, a predictive OVA-PS-PWM strategy for CHB converters has been proposed. To obtain future predictions of the harmonic distortion, a novel discrete-time dynamic model based on the Fourier analysis of the converter output voltage in the synchronous dq-frame was derived. This model is used to formulate an optimal control problem with an analytic solution that can be applied to find optimal PS-angles for CHB converters of any number of SMs and for the complete operational range of the converter.

Simulation tests for a three-SM CHB converter were carried out to compare the performance of the proposed OVA-PS-PWM and the VA-PS-PWM [83]. The results showed that for moderate SM power imbalances, both techniques converge to the same optimal solution, completely eliminating the harmonic distortion at $2f_c$. However, under severe power imbalance among SMs, the proposed OVA-PS-PWM outperforms [83] by minimizing the CHB converter output voltage WTHD at every sampling instant, including the operating

points in which the VA-PS-PWM provides undetermined PS-angle solutions.

Experimental results have also verified the effectiveness of the proposed OVA-PS-PWM under an inter-SM power imbalance operation scenario, including different SM dc-voltages and ac-voltage references for a nine-SM CHB converter. The proposed predictive OVA-PS-PWM significantly reduced the undesired switching harmonic components, compared with the conventional PS-PWM. In fact, harmonics up to $6f_c$ were minimized to less than 1%. Moreover, the obtained current waveforms and harmonic spectra showed that only a small increase of current THD and WTHD is obtained by operating the converter under highly unbalanced scenarios in relation to its balance operation for the same output current reference. Therefore, the proposed OVA-PS-PWM can extend the excellent harmonic performance of PS-PWM for unbalanced operation scenarios, allowing the reduction of the size of the output filter. Accordingly, the proposed OVA-PS-PWM can be a promising modulation alternative for CHB-SL-BESS applications, which require the unbalanced operation of the converter for extended periods of time.

Chapter 3

Offset-Free Optimal Control of CHB-SL-BESS Based on a Kalman Filter Harmonic Compensator

3.1 Introduction

As discussed in the thesis introduction, several control strategies have been proposed to govern the CHB converter currents based on the well-known voltage oriented control schemes. Within these strategies, classical controllers, e.g., PI regulators designed using the synchronous dq-frame or PR controllers, are often combined with a suitable modulation stage, such as a conventional PS-PWM or a level-shift PWM [87], [98]–[100]. Nevertheless, due to recent advances in digital control platforms, model predictive control (MPC) schemes have emerged as promising control alternatives for power converters. In general, MPC strategies may outperform standard PWM-based controllers by offering several advantages, such as a simple design process, high dynamic performance, and the ability to include multiple control inputs and outputs, constraints, and nonlinearities [101].

Among the MPC strategies, the finite-control-set MPC (FCS-MPC) is considered the most popular MPC scheme for power converters in the current literature [101], even though it has not been widely adopted in industrial applications. Several FCS-MPC strategies have been proposed for the CHB converter [102]–[106]. This control strategy avoids an external modulation stage by directly considering the power switches' state (or voltage

levels) as input constraints in the optimization problem. Accordingly, all the allowed switching combinations can be evaluated in a cost function, finding the optimal control input at every sampling instant. FCS-MPC strategies are characterized by providing a fast transient response. However, this control scheme faces challenges related to the high computational effort required to evaluate the switching combinations in converters with a large number of SMs, variable switching frequency, and steady-state error [101].

Indirect MPC schemes for multilevel converters have been proposed to mitigate some of the issues of FCS-MPC strategies while maintaining a fast dynamic response. In indirect MPC approaches, a PWM stage is considered at the converter model instead of directly evaluating the discrete combinations of switch positions. As a consequence, the optimization problem in these MPC strategies is formulated to compute optimal modulating signals or duty cycles. Some examples of recent indirect MPC strategies for the CHB converter, including the modulated MPC (M^2PC) technique and the sequential PS-PWM MPC, can be found in [78], [89], [107]–[109].

One of the major challenges of implementing optimal control strategies for power converters in practical applications is dealing with parameter uncertainty and unaccounted disturbances that might affect the control system [110]. Indeed, the steady-state performance of optimal control methods for the CHB converter is highly dependent on the accuracy of their prediction models [103]. In this sense, parameter mismatch in the converter model, measurement errors, and discretization approximations, can drastically deteriorate the performance of these optimal control strategies[1]. Consequently, several methods have been proposed to improve the steady-state performance of optimal control strategies for the CHB converter.

A hybrid FCS-MPC strategy that combines a PR controller working in parallel with the predictive controller is proposed in [106]. The PR controller obtains an average arm voltage reference based on the current tracking error. This reference computes the equivalent switching patterns resulting from feeding the average voltage reference into a conventional PWM stage. Then, these patterns are employed to calculate the switching state reference at the FCS-MPC cost function, improving the steady-state performance and reducing the switching frequency. As the PR controller works in parallel with the FCS-MPC strategy,

[1]The theoretical impact of each of these factors on the accuracy of the prediction model is analyzed in detail in [102].

its settling time must be significantly slower than the sampling frequency, limiting the dynamic response of this steady-state error compensation strategy.

In [103], a PR controller is also combined with an FCS-MPC strategy. Nevertheless, the output voltage of the PR controller is used to compute a compensation voltage, which is included in the CHB converter current prediction model. Following a similar approach in [109], a sinusoidal steady-state compensation term is proposed for an M^2PC strategy to account for the model parameters uncertainty in an MMC. These methods effectively compensate for current tracking errors at the fundamental frequency. However, the PR controller cannot properly compensate for higher-order voltage harmonic disturbances.

A hierarchical multifactorial prediction error correction method is proposed in [102] to improve the CHB converter steady-state performance for an FCS-MPC scheme. This method manipulates the arm current prediction by applying a correction stage derived from an analytic analysis of the potential causes of the steady-state errors. Although this method improves the current THD under converter parameters mismatch, it cannot compensate for the third harmonic disturbance component introduced by the SM capacitor voltage ripples in the converter output currents.

The causes of steady-state error are analyzed for the MMC considering a deadbeat control scheme in [111], including the effect of the SM capacitor voltage ripples. The theoretical analysis confirms that higher-order harmonic components appear in the MMC circulating current if the instantaneous SM capacitor voltage ripples are not measured accurately. Accordingly, a feed-forward compensation loop that normalizes the SM voltage references with the SM capacitor voltage measurements, combined with an online inductance estimation method, is proposed to reduce the steady-state error at the converter currents. However, the feed-forward compensation term proposed in this method requires a fast sampling frequency, and it is sensitive to noise and lag in the SM capacitor voltage measurements.

In CHB-SL-BESS, the model parameter uncertainty issue can be exacerbated as the internal resistance and capacity of the battery change over time due to battery aging. Moreover, significant changes in internal resistance can be observed even during a full charge/discharge cycle, as this parameter can vary regarding the battery SoC and temperature [18]. As a consequence, online internal resistance or efficiency estimation methods are often implemented in CHB-SL-BESS control strategies, in order to achieve the inter-SM

power imbalance without steady-state errors [33], [112]. However, including these algorithms to compensate for the steady-state errors in the CHB converter control not only increases the control complexity but also requires redundant current and voltage measurements for the BP or complex communication networks to acquire these measurements from each BP BMS at the current controller sampling frequency.

Motivated by the above, this chapter proposes a Kalman Filter (KF) harmonic compensator strategy to mitigate the steady-state errors in the output currents of CHB converters governed by direct or indirect optimal control schemes. The proposed KF strategy considers an augmented state space model in which the arm currents and voltage harmonic disturbances are included in the system state. In this way, the additional arm voltage harmonic states are used to represent the equivalent voltage drops related to converter modeling errors and unmeasured disturbances. A steady-state KF observer [113] is designed to estimate the instantaneous voltage disturbances from the CHB converter current measurements. Then, the resulting voltage disturbance estimates are used to improve the arm currents predictions and the steady-state arm voltage references.

The main advantage of the proposed KF strategy is that the arm voltage disturbance estimates can include several harmonic components. Therefore, the proposed strategy improves the CHB converter output currents THD by effectively rejecting disturbances at the fundamental frequency due to model parameters mismatch, and higher-order harmonic disturbances introduced by the SM capacitor voltage ripples. Moreover, the proposed KF harmonic compensator only requires the average SM capacitor voltage measurements, which can be sampled at a lower frequency rate, using the existing BMS hardware at each BP.

To verify the effectiveness of the proposed KF-based strategy, experimental results on a Δ-CHB converter based SL-BESS prototype with severe parameter mismatch and errors in the SM capacitor voltage measurements are provided for three different optimal control strategies.

3.2 CHB Converter Model and Standard Optimal Control

Figure 3.1 illustrates the Δ-CHB converter topology under analysis in this work. This power converter consists of three phase arms in a delta configuration. The arms are formed

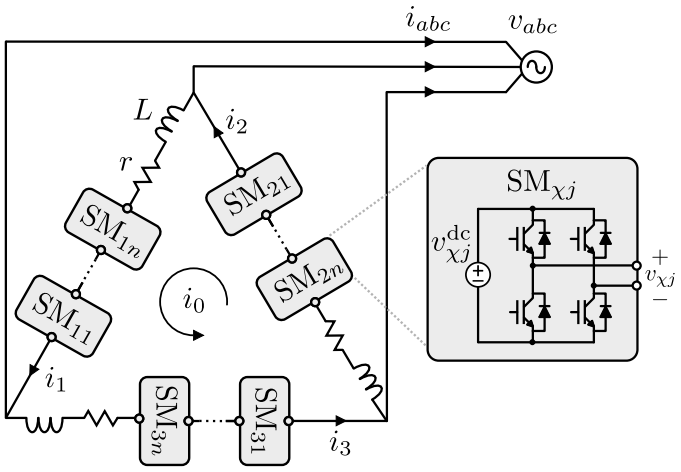


Figure 3.1: Delta-connected CHB converter with n power cells.

by the series connection of n H-bridge SMs (HB-SMs) with an arm filter of inductance L and an arm equivalent resistance r. The dc side of the HB-SMs consists of a floating capacitor, which can be utilized independently or connected to batteries or a dc-dc conversion stage, depending on the application of the Δ-CHB converter [114]. The ac side of the HB-SMs has two pairs of power switches, which allows the generation of three different output voltage levels. Each ac terminal of the Δ-CHB converter is connected to one phase of the point of common coupling (PCC).

3.2.1 Continuous-Time Dynamic Model

To describe the CHB converter current dynamics, the arm currents can be considered as the system state, i.e.:

$$\boldsymbol{x}(t) = \begin{bmatrix} i_1(t) & i_2(t) & i_3(t) \end{bmatrix}^T. \tag{3.1}$$

Based on the CHB converter topology depicted in Fig. 3.1, the following continuous-time state-space model can be obtained:

$$\frac{d\boldsymbol{x}(t)}{dt} = \boldsymbol{A}_c\boldsymbol{x}(t) + \boldsymbol{B}_c\boldsymbol{u}(t) + \boldsymbol{M}_c\boldsymbol{v}_g(t), \tag{3.2}$$

where is $\boldsymbol{u}(t) = \begin{bmatrix} v_1(t) & v_2(t) & v_3(t) \end{bmatrix}^T$ is the control input formed by the CHB arm out-

put voltages, $v_\chi(t)$, and $\boldsymbol{v}_g(t) = \begin{bmatrix} v_a(t) & v_b(t) & v_c(t) \end{bmatrix}^T$ is the vector containing the PCC voltages. Besides[2],

$$\boldsymbol{A}_c = -\frac{r}{L}\boldsymbol{I}_3,\ \boldsymbol{B}_c = \frac{1}{L}\boldsymbol{I}_3,\ \boldsymbol{M}_c = -\frac{1}{L}\begin{bmatrix} -1 & 1 & 0 \\ 0 & -1 & 1 \\ 1 & 0 & -1 \end{bmatrix}. \tag{3.3}$$

For a generic n-cell CHB converter arm, the total output voltage can be expressed as the sum of the individual output voltage at each HB-SM, $v_{\chi j}(t)$, as

$$v_\chi(t) = \sum_{j=1}^{n} v_{\chi j}(t),\ \ \forall\, \chi \in \{1, 2, 3\}. \tag{3.4}$$

In the Δ-CHB converter, a circulating current, $i_0(t)$, can be injected into the arm currents without affecting the grid currents. As previously discussed in the first chapter, this circulating current allows the control of the inter-arm power imbalance, achieving different power references at each arm while maintaining balanced ac currents at the converter output [107]. The relationships between the arm currents, the grid currents, and the circulating current can be expressed via:

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_0(t) \end{bmatrix} = \boldsymbol{\Psi}\boldsymbol{x}(t), \quad \boldsymbol{\Psi} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix}, \tag{3.5}$$

and $i_c(t) = -i_a(t) - i_b(t)$.

3.2.2 Discrete-Time Dynamic Model

A discrete-time dynamic model for the CHB converter arm currents is often required to implement optimal control strategies in digital control platforms. In this sense, a discrete-time state-space model can be obtained by applying the zero-order hold (ZOH) discretiza-

[2]Note that $\boldsymbol{I}_n$ refers to the identity matrix of dimension n.

tion to (3.2), with a sampling period of T_s, leading to:

$$\boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}\boldsymbol{u}(k) + \boldsymbol{M}\boldsymbol{v}_g(k), \tag{3.6}$$

with

$$\boldsymbol{A} = e^{\boldsymbol{A}_c T_s}, \tag{3.7}$$

$$\boldsymbol{B} = \boldsymbol{A}_c^{-1}(\boldsymbol{A} - \boldsymbol{I}_3)\boldsymbol{B}_c, \tag{3.8}$$

$$\boldsymbol{M} = \boldsymbol{A}_c^{-1}(\boldsymbol{A} - \boldsymbol{I}_3)\boldsymbol{M}_c. \tag{3.9}$$

Furthermore, at each sampling instant, the arm output voltages can be expressed as $v_\chi(k) = \sum_{j=1}^{n} v_{\chi j}(k)$. Consequently, the optimal control strategy chosen to govern the CHB converter defines the range of values allowed for the arm voltages as control inputs. For instance, in FCS-MPC strategies, the control input is often considered as the discrete set of voltage levels that can be obtained at the arm output voltage, i.e., $v_\chi(k) = v_{dc}^{\star} v_{l\chi}(k)$, with $v_{l\chi}(k) \in \{-n, -n+1, \ldots, 0, \ldots, n+1, n\}$. Conversely, in optimal control strategies that consider a modulation stage, the possible arm output voltages are given by a continuous set of values, defined as $v_\chi(k) \in [-nv_{dc}^{\star}, nv_{dc}^{\star}]$. In any case, (3.6) can be used as the converter prediction model in standard optimal control strategies for the CHB converter.

3.2.3 Optimal Control Problem and Steady-State Control Input Reference Design

Several standard FCS-MPC and indirect MPC strategies [78], [89], [105]–[107] are based on computing the optimal control input, $\boldsymbol{u}^{\text{opt}}(k)$, that minimizes the following cost function:

$$J(k) = \|\boldsymbol{x}(k+1) - \boldsymbol{x}^{\star}(k+1)\|_2^2 + \lambda_u \|\boldsymbol{u}(k) - \boldsymbol{u}^{\star}(k)\|_2^2, \tag{3.10}$$

where $\boldsymbol{u}^{\star}(k)$ is the required CHB output voltage to maintain the arm currents at the desired steady-state operation conditions. Accordingly, the weighting factor λ_u allows the designer to regulate the controller closed-loop performance [115].

It is important to remark that when the system state approaches its reference, i.e., $\boldsymbol{x}(k) \approx \boldsymbol{x}^{\star}(k)$, the first term of the cost function (3.10) is almost zero. As a consequence,

the second term becomes the dominant one, and $\boldsymbol{u}^{\text{opt}}(k)$ tracks $\boldsymbol{u}^{\star}(k)$ in steady-state. In this sense, appropriate steady-state reference voltages for the CHB converter arms can be found simply by replacing the system state reference in the dynamic model (3.6), and solving the equation system for $\boldsymbol{u}(k)$, as follows:

$$\boldsymbol{u}^{\star}(k) = \boldsymbol{B}^{-1}\left(\boldsymbol{x}^{\star}(k+1) - \boldsymbol{A}\boldsymbol{x}^{\star}(k) - \boldsymbol{M}\boldsymbol{v}_g(k)\right). \tag{3.11}$$

Replacing the model matrices (3.7), (3.8) and (3.9) into (3.11) yields to:

$$\boldsymbol{u}^{\star}(k) = r\boldsymbol{x}^{\star}(k) + \frac{r}{\sigma}\left(\boldsymbol{x}^{\star}(k+1) - \boldsymbol{x}^{\star}(k)\right) - L\boldsymbol{M}_c\boldsymbol{v}_g(k), \tag{3.12}$$

with $\sigma = e^{T_s L/r} - 1$. Moreover, the arm current references can be computed considering the grid current references and the circulating current reference as:

$$\boldsymbol{x}^{\star}(k) = \boldsymbol{\Psi}^{-1}\begin{bmatrix} i_a^{\star}(k) & i_b^{\star}(k) & i_0^{\star}(k) \end{bmatrix}^T, \tag{3.13}$$

in which the grid current references can be obtained according to the conventional $p-q$ Theory [116], and the circulating current reference can be obtained following the inter-arm active power balance strategy proposed in [32].

Ideally, (3.12) should perfectly track the desired steady-state arm current references. However, in practical applications, the steady-state currents can drift from their references due to prediction model errors affecting $\boldsymbol{u}^{\star}(k)$. These errors can originate from model parameter uncertainties, measurement errors, and discretization approximations [102]. Consequently, the proposed KF strategy is designed to compensate for these errors in the CHB converter dynamic model, improving the current predictions and the steady-state control input reference used in standard optimal control schemes.

3.2.4 Effect of Unmeasured SM Capacitor Voltage Ripples

It is clear from (3.12) that parameter errors in r and L, and measurement errors at the PCC voltages, directly affect the steady-state control input reference. Nevertheless, the SM capacitor voltage ripples are also an additional cause for steady-state error, depending on how $\boldsymbol{u}^{\text{opt}}(k)$ is applied to the converter SMs.

In some conventional optimal control strategies for the CHB converter, the SM capac-

itor voltage ripples are neglected when considering the possible arm output voltage levels [104], [105] or at the modulation stage [108], for FCS-MPC and indirect MPC strategies, respectively. As a result, steady-state errors, proportional to the sum of the SM capacitor voltage ripple amplitudes, appear in the arm output voltages, as analyzed as follows.

Assuming that the arm voltage is divided equally among the SMs and that the SM capacitor voltages are equal to the average BP voltage for a CHB-BESS with balanced SoC, the actual steady-state output voltage of each HB-SM is given by:

$$v_{\chi j}(t) = \frac{v_{\chi}^{\star}(t)}{n} \frac{v_{\chi j}^{\mathrm{dc}}(t)}{v_{\mathrm{dc}}^{\star}}, \tag{3.14}$$

with $v_{\chi j}^{\mathrm{dc}}(t)$, the instantaneous SM capacitor voltage of the SM-χj, and $v_{dc}^{\star}$ is the average BP voltage, which is assumed to be equal for each SM in this particular analysis. Therefore, by replacing (3.14) into (3.4), the resulting arm output voltage can be written as:

$$v_{\chi}(t) = \frac{v_{\chi}^{\star}(t)}{n v_{\mathrm{dc}}^{\star}} \sum_{j=1}^{n} v_{\chi j}^{\mathrm{dc}}(t). \tag{3.15}$$

Considering that the balanced SM capacitor voltages are composed of the dc voltage value, and the SM capacitor ripple, i.e., $v_{\chi j}^{\mathrm{dc}}(t) = v_{\mathrm{dc}}^{\star} + \tilde{v}_{\chi j}(t)$, and replacing this expression into (3.15), leads to:

$$v_{\chi}(t) = v_{\chi}^{\star}(k) + \tilde{v}_{\chi}(t), \quad \tilde{v}_{\chi}(t) = \frac{v_{\chi}^{\star}(t)}{n v_{\mathrm{dc}}^{\star}} \sum_{j=1}^{n} \tilde{v}_{\chi j}(t), \tag{3.16}$$

where $\tilde{v}_{\chi}(t)$, accounts for the arm output voltage error introduced by the sum of the SM capacitor voltage ripples.

Due to the single-phase nature of the CHB converter arms, the SM capacitor voltage ripples inherently contain oscillations at twice the fundamental frequency, ω, and its multiples. However, harmonics higher than fourth-order generally can be neglected in the SM capacitor voltage ripples. In this way, the sum of the SM capacitor voltage ripples can be approximated as follows:

$$\sum_{j=1}^{n} \tilde{v}_{\chi j}(t) \approx \tilde{V}_{\chi}^{2\omega} \sin(2\omega t + \phi_{2\omega}) + \tilde{V}_{\chi}^{4\omega} \sin(4\omega t + \phi_{4\omega}). \tag{3.17}$$

Moreover, replacing (3.17) into (3.16) leads to the following approximation for the instantaneous arm output voltage error:

$$\begin{aligned}\tilde{v}_\chi(t) \approx\ & m_a \sin(\omega t + \phi_{v\chi}) \tilde{V}_\chi^{2\omega} \sin(2\omega t + \phi_{2\omega}) \\ & + m_a \sin(\omega t + \phi_{v\chi}) \tilde{V}_\chi^{4\omega} \sin(4\omega t + \phi_{4\omega}),\end{aligned} \tag{3.18}$$

with $m_a \sin(\omega t + \phi_{v\chi}) = \frac{v_\chi^\star(t)}{n v_{\mathrm{dc}}^\star}$. Finally, expanding (3.18) by using the sine product to sum trigonometric identity leads to[3]:

$$\begin{aligned}\tilde{v}_\chi(t) \approx\ & \frac{m_a \tilde{V}_\chi^{2\omega}}{2} \left(\cos(\omega t + \phi_{2\omega - v\chi}) - \cos(3\omega t + \phi_{2\omega + v\chi})\right) \\ & + \frac{m_a \tilde{V}_\chi^{4\omega}}{2} \left(\cos(3\omega t + \phi_{4\omega - v\chi}) - \cos(5\omega t + \phi_{4\omega + v\chi})\right).\end{aligned} \tag{3.19}$$

Therefore, neglecting the SM capacitor voltage ripples when applying the CHB optimal control inputs results in a voltage error that can be decomposed into a first, third, and fifth predominant harmonic components. This voltage error propagates through the CHB arm currents, increasing their THD and affecting the steady-state performance of the converter.

Although the BMS measures the BP cell voltages for safety concerns, the sampling time of this embedded system is usually around 1 Hz, and its measurements usually involve low pass filtering stages [18]. As a consequence, these measurements cannot be effectively used by the Δ-CHB converter current controller, and additional SM capacitor voltage sensors are required in order to compensate for the SM capacitor voltage ripples using a feed-forward term similar to [111], which increases the converter hardware complexity and costs.

3.3 Proposed KF-based Steady-State Error Compensation Strategy

This section introduces the proposed KF harmonic compensator for the offset-free optimal control of the CHB converter currents. The proposed KF strategy achieves this objective by estimating the voltage drops in the converter arms, which the standard converter dynamic model (3.6) cannot describe. Accordingly, the estimated voltages can be used to enhance the steady-state control input reference used by optimal control schemes

[3]Consider that the notation $\phi_{a\pm b} = \phi_a \pm \phi_b$ is assumed in (3.19).

and to improve the current predictions, eliminating the current steady-state error even if the SM capacitor ripples are not measured.

3.3.1 Proposed Augmented State-Space Dynamic Model

The key idea behind the proposed KF steady-state error compensation strategy is to include a model for sinusoidal voltage disturbances composed of several harmonic components, which impact the state dynamics of each arm current.[4] These voltages represent the equivalent voltage drops at the CHB converter arms not considered in the standard converter model (3.6) due to modeling errors or caused by external disturbances. Then, a steady-state KF is designed to estimate these voltage drops and to predict the arm current values.

As a general case, a sinusoidal voltage harmonic component of constant amplitude and frequency can be expressed in the single-phase $\alpha\beta$-frame as

$$d_h^{\alpha}(t) = d\cos(h\omega t + \phi_h), \tag{3.20}$$

$$d_h^{\beta}(t) = d\sin(h\omega t + \phi_h), \tag{3.21}$$

where h denotes the harmonic order, ω is the fundamental frequency, and ϕ_h is its phase, indicating that different voltage harmonic components are not necessarily in phase. Moreover, differentiating the $\alpha\beta$ voltages in (3.20) and (3.21), the following dynamic equations that describe this voltage harmonic component can be found:

$$\dot{\boldsymbol{d}}_h^{\alpha\beta}(t) = \begin{bmatrix} 0 & -h\omega \\ h\omega & 0 \end{bmatrix} \boldsymbol{d}_h^{\alpha\beta}(t), \quad \boldsymbol{d}_h^{\alpha\beta}(t) = \begin{bmatrix} d_h^{\alpha}(t) \\ d_h^{\beta}(t) \end{bmatrix}. \tag{3.22}$$

In this way, (3.22) can be discretized using the ZOH method to obtain a dynamic model of voltage disturbance harmonic components that impact the current of the arm-χ, i.e.:

$$\boldsymbol{d}_{\chi h}^{\alpha\beta}(k+1) = \boldsymbol{\Gamma}_h \boldsymbol{d}_{\chi h}^{\alpha\beta}(k), \tag{3.23}$$

[4] Further details about the concept of estimating additive disturbances via an observer can be found in [117].

with

$$\boldsymbol{d}_{\chi h}^{\alpha\beta}(k) = \begin{bmatrix} d_{\chi h}^{\alpha}(k) \\ d_{\chi h}^{\beta}(k) \end{bmatrix}, \boldsymbol{\Gamma}_h = \begin{bmatrix} \cos(h\omega T_s) & -\sin(h\omega T_s) \\ \sin(h\omega T_s) & \cos(h\omega T_s) \end{bmatrix}. \tag{3.24}$$

As analyzed in the previous section, to fully eliminate the steady-state error in the arm currents, a voltage disturbance comprised of a first, third, and fifth harmonic component must be compensated at each arm. Consequently, the following augmented system state is defined:

$$\boldsymbol{x}_a(k) = \begin{bmatrix} \boldsymbol{x}^T(k) & (\boldsymbol{d}^{\alpha\beta}(k))^T \end{bmatrix}^T \in \mathbb{R}^{21\times 1}, \tag{3.25}$$

$$\boldsymbol{d}^{\alpha\beta}(k) = \begin{bmatrix} (\boldsymbol{d}_1^{\alpha\beta}(k))^T & (\boldsymbol{d}_3^{\alpha\beta}(k))^T & (\boldsymbol{d}_5^{\alpha\beta}(k))^T \end{bmatrix}^T, \tag{3.26}$$

where $\boldsymbol{d}_h^{\alpha\beta}(k)$= $\begin{bmatrix} (\boldsymbol{d}_{1h}^{\alpha\beta}(k))^T & (\boldsymbol{d}_{2h}^{\alpha\beta}(k))^T & (\boldsymbol{d}_{3h}^{\alpha\beta}(k))^T \end{bmatrix}^T \in \mathbb{R}^{6\times 1}$ is the vector containing the respective voltage disturbances of frequency $h\omega$ rad/s that affect each arm of the Δ-CHB converter. Moreover, considering (3.25), and the dynamic models (3.6) and (3.23), the proposed augmented state-space model that describes the converter and disturbances coupled dynamics can be expressed via:

$$\boldsymbol{x}_a(k+1) = \boldsymbol{\mathcal{A}}_a\boldsymbol{x}_a(k) + \boldsymbol{\mathcal{B}}_a\boldsymbol{u}(k) + \boldsymbol{p}(k), \tag{3.27}$$

$$\boldsymbol{y}(k) = \boldsymbol{x}(k) = \boldsymbol{\mathcal{C}}_a\boldsymbol{x}_a(k), \tag{3.28}$$

with

$$\boldsymbol{\mathcal{A}}_a = \begin{bmatrix} \boldsymbol{A} & \boldsymbol{D} \\ \boldsymbol{0}_{18\times 3} & \boldsymbol{\Gamma} \end{bmatrix}, \boldsymbol{\mathcal{B}}_a = \begin{bmatrix} \boldsymbol{B} \\ \boldsymbol{0}_{18\times 3} \end{bmatrix}, \boldsymbol{p}(k) = \begin{bmatrix} \boldsymbol{M}\boldsymbol{v}_g(k) \\ \boldsymbol{0}_{18\times 1} \end{bmatrix},$$

$$\boldsymbol{D} = \begin{bmatrix} \boldsymbol{D}_\alpha & \boldsymbol{D}_\alpha & \boldsymbol{D}_\alpha \end{bmatrix}, \boldsymbol{D}_\alpha = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}, \tag{3.29}$$

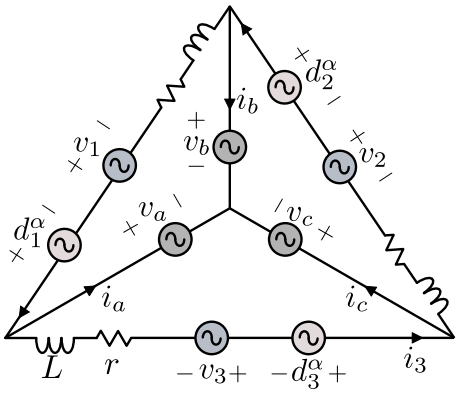


Figure 3.2: Equivalent continuous-time circuit diagram of the augmented state-space model for the CHB converter, where $d_\chi^\alpha = (d_{\chi 1}^\alpha + d_{\chi 3}^\alpha + d_{\chi 5}^\alpha)\frac{r\gamma}{L(\gamma-1)}$, $\gamma = e^{T_s r/L}$.

with $\boldsymbol{\Gamma} = \text{blkdiag}(\boldsymbol{\Gamma}_1, \boldsymbol{\Gamma}_1, \boldsymbol{\Gamma}_1, \boldsymbol{\Gamma}_3, \boldsymbol{\Gamma}_3, \boldsymbol{\Gamma}_3, \boldsymbol{\Gamma}_5, \boldsymbol{\Gamma}_5, \boldsymbol{\Gamma}_5)$, and $\boldsymbol{\mathcal{C}}_a = \begin{bmatrix} \boldsymbol{I}_3 & \boldsymbol{0}_{3\times 18} \end{bmatrix}$. Finally, Fig. 3.2 shows the equivalent circuit representation of the proposed augmented state-space model for the CHB converter topology with disturbances.

3.3.2 Proposed KF-based Compensation Strategy

The observability matrix of the proposed linear augmented state-space model (3.30) is full rank. Therefore, a state observer can be designed to estimate the arm voltage disturbances from the arm current measurements. Accordingly, the following state observer dynamic model is considered:

$$\begin{aligned} \hat{\boldsymbol{x}}_a(k+1) &= \boldsymbol{\mathcal{A}}_a \hat{\boldsymbol{x}}_a(k) + \boldsymbol{\mathcal{B}}_a \boldsymbol{u}(k) + \boldsymbol{p}(k) + \boldsymbol{K}_f(\boldsymbol{y}(k) - \hat{\boldsymbol{y}}(k)) \\ \hat{\boldsymbol{y}}(k) &= \boldsymbol{\mathcal{C}}_a \hat{\boldsymbol{x}}_a(k), \end{aligned} \tag{3.30}$$

where $\boldsymbol{K}_f$ is the observer gain matrix. This matrix must be designed to ensure that the closed-loop observer matrix $\boldsymbol{A}_{\text{obs}} = \boldsymbol{\mathcal{A}}_a - \boldsymbol{K}_f \boldsymbol{\mathcal{C}}_a$ is Schur stable, i.e., all its eigenvalues have a norm strictly less than one. Consequently, this work proposes the application of a steady-state Kalman Filter [113] to compute the observer gain matrix. In this way, $\boldsymbol{K}_f$ can be obtained offline by solving the following discrete-time algebraic Riccati equation:

$$\boldsymbol{K}_f = \boldsymbol{\mathcal{A}}_a \boldsymbol{P} \boldsymbol{\mathcal{C}}_a^T \left(\boldsymbol{\mathcal{C}}_a \boldsymbol{P} \boldsymbol{\mathcal{C}}_a^T + \boldsymbol{R} \right)^{-1}, \tag{3.31}$$

$$\boldsymbol{P} = \boldsymbol{\mathcal{A}}_a \boldsymbol{P} \boldsymbol{\mathcal{A}}_a^T - \boldsymbol{K}_f \boldsymbol{\mathcal{C}}_a \boldsymbol{P} \boldsymbol{\mathcal{A}}_a^T + \boldsymbol{Q}, \tag{3.32}$$

where $\boldsymbol{P} \in \mathbb{R}^{21\times21}$ is the steady-state estimate covariance matrix, and $\boldsymbol{Q} \in \mathbb{R}^{21\times21}$, $\boldsymbol{R} \in \mathbb{R}^{3\times3}$ are the process and sensor noise covariance matrices, respectively.

The process noise covariance matrix represents the uncertainty in the dynamic model (3.25), accounting for the modeling errors that cannot be represented by the proposed voltage harmonic disturbances. Conversely, the sensor noise covariance matrix represents the variability of the current sensor measurements. As the augmented system state is comprised of the arm currents and the sinusoidal voltage disturbances, and considering that the arm currents are the only measured outputs used for the state estimation, the covariance matrices of the proposed KF are defined as follows:

$$\boldsymbol{Q} = \begin{bmatrix} \boldsymbol{I}_3 & \boldsymbol{0}_{3\times18} \\ \boldsymbol{0}_{18\times3} & \lambda_q \boldsymbol{I}_{18} \end{bmatrix}, \quad \boldsymbol{R} = \lambda_r \boldsymbol{I}_3, \tag{3.33}$$

where λ_q and λ_r, are positive constants to model the relative uncertainty of the arm voltage disturbance estimates and the current sensors, respectively.

Firstly, in order to design the KF observer, the value of λ_r can be computed by recording a large number of measurements from the current sensors in the experimental setup for a constant input value and then computing the covariance of the data set. Subsequently, the value of λ_q can be adjusted to achieve the desired closed-loop performance of the state observer.

A small value for λ_q implies that the prediction model is remarkably accurate. As a result, the observer will tend to rely more on the model predictions rather than rapidly adjusting the state estimates of the voltage disturbances based on the arm currents prediction errors. On the contrary, larger values for λ_q imply that the dynamic model is quite uncertain, leading the observer to provide larger corrections to the state estimates based on the estimation errors. Nevertheless, larger values for λ_q can increase the amount of noise propagated from the sensors to the state estimation.

Finally, note that λ_r can also be modified to adjust the observer bandwidth or to avoid numerical rounding errors in the digital control platform when a value close to zero is obtained from the experimental setup measurements. However, it is essential to consider that increasing the value of λ_r makes the observer less aggressive by relying more on the dynamic model, whereas reducing its value diminishes the noise-filtering capabilities of the

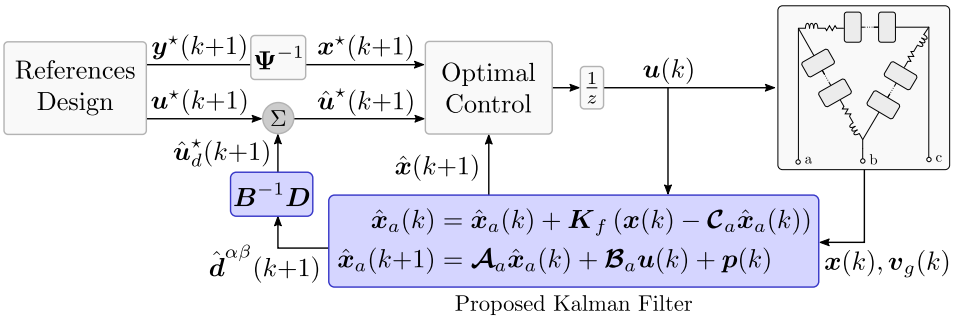


Figure 3.3: Block diagram of the proposed KF observer for steady-state error compensation.

KF observer.

The predicted voltage disturbance estimates can be extracted from the augmented system state and used to compute the required control input compensation that cancels their effect on the arm output voltages, as follows:

$$\hat{\boldsymbol{u}}_d^\star(k+1) = \boldsymbol{B}^{-1}\boldsymbol{D}\hat{\boldsymbol{d}}^{\alpha\beta}(k+1) \in \mathbb{R}^3. \tag{3.34}$$

Adding the control input compensation (3.34) to (3.12) leads to the compensated steady-state control input reference, which includes the aggregated modeling errors of the CHB converter. Accordingly, the control input that needs to be provided to the optimal control strategy is given by:

$$\hat{\boldsymbol{u}}^\star(k+1) = \boldsymbol{u}^\star(k+1) + \hat{\boldsymbol{u}}_d^\star(k+1). \tag{3.35}$$

Finally, a block diagram that depicts the implementation of the proposed KF strategy is shown in Fig. 3.3. Note that implementing the proposed KF not only involves using the enhanced steady-state control input reference (3.35), but also requires feeding the estimated predicted currents to the optimal control, as this state prediction considers the effect of the unmeasured disturbances[5].

[5]Note that in FCS-MPC schemes, the proposed model (3.30) must be used to obtain predictions to k+2 for the standard delay compensation technique.

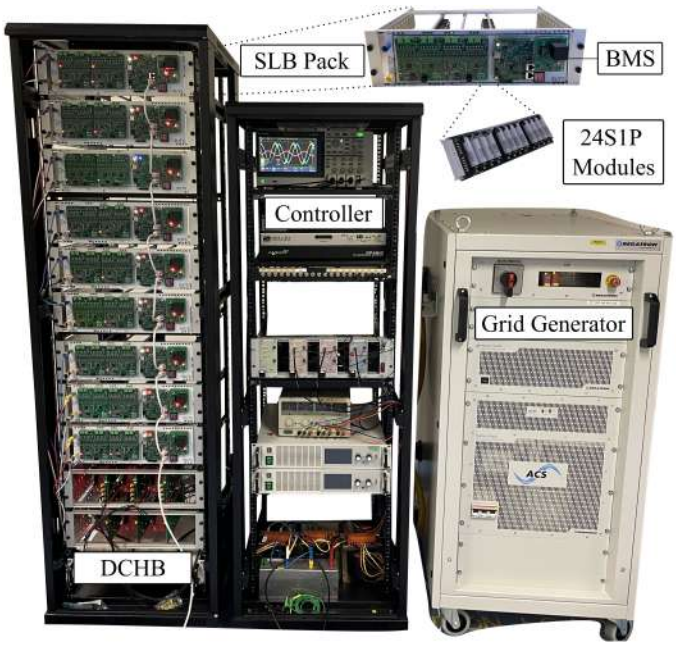


Figure 3.4: Three-phase CHB-BESS converter prototype.

Table 3.1: Main parameters for the experimental setup.

Description	Variable	Value
Number HB-SMs	n	9
CHB converter parameters	L, r, C	10 mH, 500 mΩ, 400 μF
Nominal battery voltage	V_{DC}	80.4 V
Grid voltage (LL-RMS)	V_g, f_0	122.47 V, 50 Hz
Nominal converter power	S_{nom}	1.5 kVA

3.4 Experimental Verification

3.4.1 Experimental Setup

Experimental results have been carried out to analyze the performance of the proposed KF harmonic compensator. The Δ-CHB converter shown in Fig. 3.4 has been used. This setup consists of a CHB-SL-BESS prototype in which the HB-SMs are directly connected to battery packs. These packs are assembled with 18650 Lithium-ion cells obtained from retired electric bike batteries using 24S2P and 24S3P cell configurations. The main parameters of the experimental setup and controller are summarized in Table 3.1

In addition, the experimental setup includes the grid-simulator REGATRON TC30.528.43-ACS, and an OPAL-RT OP4510 control platform, in which the optimal current control and the proposed KF strategy were implemented in the same CPU core.

3.4.2 Steady-State Performance Benchmarking

In order to evaluate the steady-state performance of the proposed KF harmonic compensator, experiments were carried out implementing the observer for three different optimal control schemes: 1) the FCS-MPC [105], 2) the PS-MPC [107], and 3) a standard linear quadratic regulator (LQR) [113]. Moreover, these controllers were also implemented with the PR-based compensation strategy proposed in [103] to compare its performance against the proposed KF harmonic compensator. Table 3.2 presents the main parameters for the optimal controllers and their corresponding KF.

Table 3.2: Optimal controllers and observers parameters. The lower sampling frequency for the LQR controller is given by the implementation of the sampling technique [72] with the proposed predictive OVA-PS-PWM.

Description	Variable	FCS-MPC	PS-MPC	LQR
PWM carrier frequency	f_c	–	2 kHz	2 kHz
Sampling frequency	f_s	10 kHz	12 kHz	4 kHz
Controller design	λ_u	10^{-6}	5	10^{-3}
Sensor noise covariance	λ_r	10^{4}	10^{-3}	10^{-3}
Process noise covariance	λ_q	10^{-1}	10^{-3}	10^{-3}

The converter parameters were modified to increase the modeling errors for the experiments described in this benchmark analysis. Values of $r = 1\,\Omega$ and $L = 5\,\text{mH}$ were given to the optimal current controllers and observer, introducing parameter errors of 100% and 50% for the arm resistance and inductance, respectively. In addition, the SM capacitor voltages were not measured for the FCS-MPC and LQR strategies; instead, each SM capacitor voltage was assumed to be equal to 80 V. This assumption was not possible for the PS-MPC, as this strategy requires the SM capacitor voltages for achieving the SM power imbalance needed for the SL-BESS application [89]. However, only the average SM capacitor voltage was passed to the PS-MPC strategy by applying a low-pass filter to the SM capacitor voltage measurements with a cutoff frequency equal to 1 Hz.

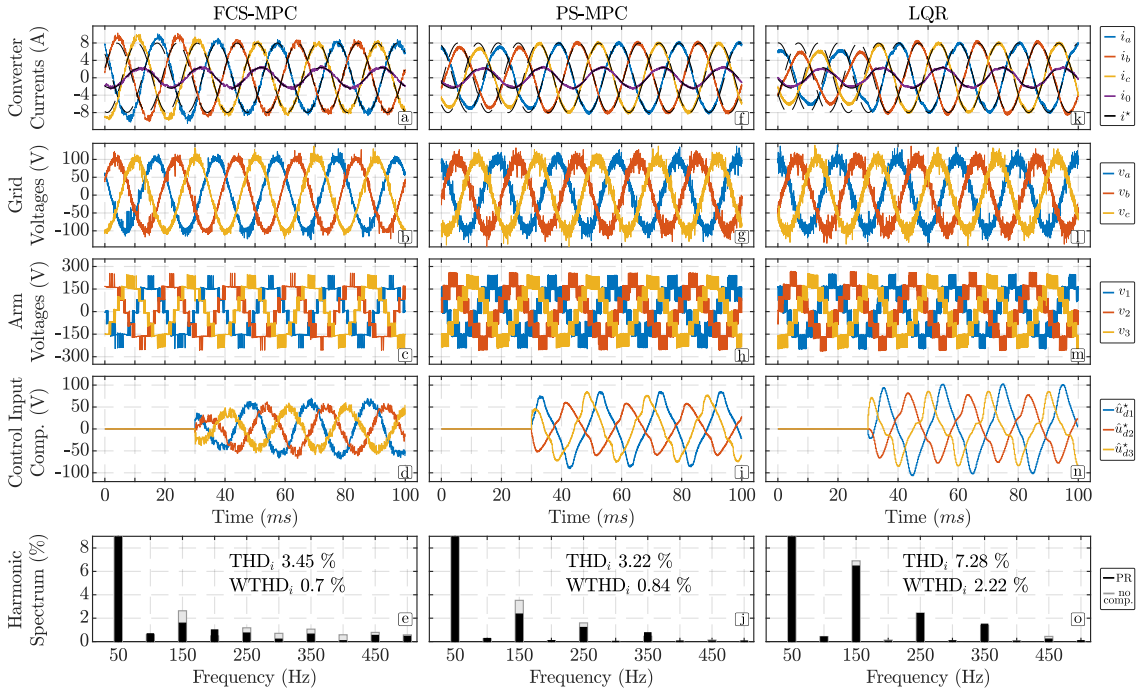


Figure 3.5: Experimental results with constant arm power references of P_1=P_3=500 W, P_2=200 W, Q=0 VAr, and the PR-based compensation strategy [103]. (a)-(e) shows the results for the FCS-MPC, (f)-(j) shows the results for the PS-MPC, and (k)-(o) shows the results for the LQR. The last row shows the harmonic spectrum of i_a with and without the compensation strategy.

The experimental results are displayed in Fig. 3.5 for the PR-based compensation and in Fig. 3.6 for the proposed KF strategy. The steady-state compensation techniques were enabled after the first 30 ms of each experimental test. Consequently, the first row of both figures, which show the converter currents tracking, clearly demonstrates that the standard optimal controllers, without a steady-state error compensation strategy, were unable to effectively track the current references due to disturbances caused by model parameter mismatches and SM capacitor voltage ripples. Further details of each experiment are provided in the following sections.

FCS-MPC

In this section, two different FCS-MPC strategies are compared. Firstly, the FCS-MPC scheme [103] was implemented. This FCS-MPC strategy utilizes an additional PR controller per arm to enhance the current prediction model and compensate for the steady-

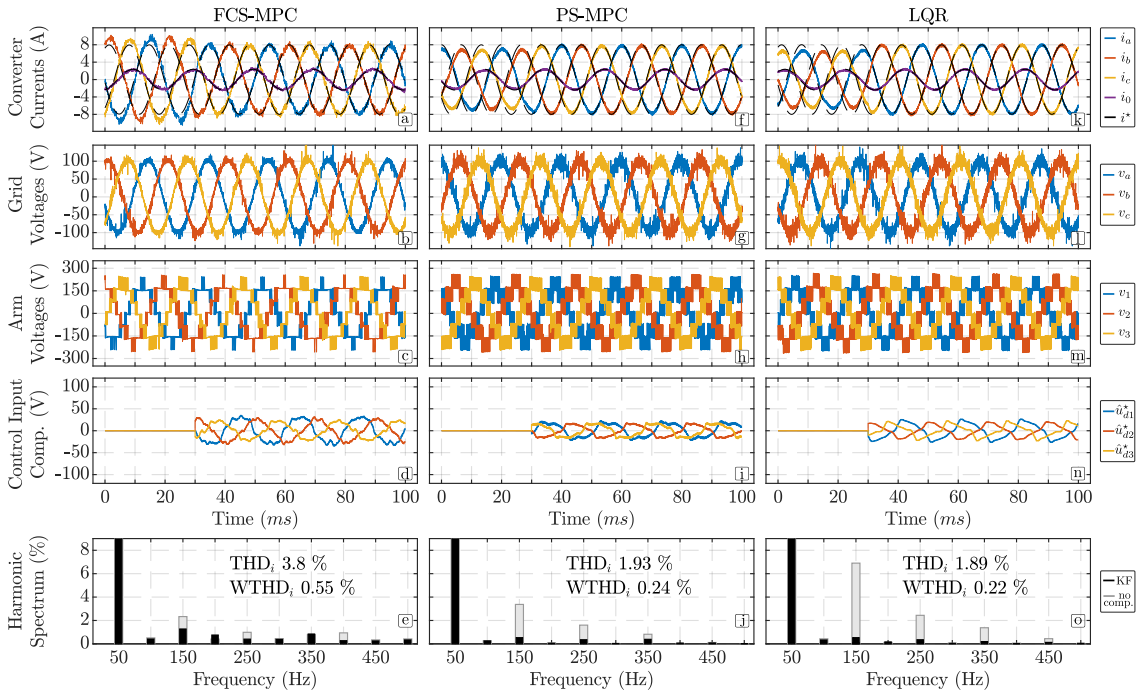


Figure 3.6: Experimental results with constant arm power references of P_1=P_3=500 W, P_2=200 W, Q=0 VAr, and the proposed KF harmonic compensator. (a)-(e) shows the results for the FCS-MPC, (f)-(j) shows the results for the PS-MPC, and (k)-(o) shows the results for the LQR. The last row shows the harmonic spectrum of i_a with and without the compensation strategy.

state errors. The experimental results for this control scheme are presented in Fig. 3.5(a)-(e). Secondly, the FCS-MPC [105] with the proposed KF harmonic compensator was tested, and the obtained experimental results for this strategy are presented in Fig. 3.6(a)-(e).

The CHB converter currents for each strategy are shown in Figs. 3.5(a) and 3.6(a), respectively. Both figures confirm that these steady-state error compensation techniques effectively mitigate the current tracking error at the fundamental frequency.

Furthermore, Figs. 3.5(e) and 3.6(e) depict the harmonic spectrums of i_a for their respective FCS-MPC strategies. These figures show that, before enabling the steady-state error compensation strategies, the FCS-MPC schemes presented the smallest third and fifth disturbance harmonic components for the converter output current, compared with the PS-MPC and the LQR. Accordingly, the FCS-MPC strategies were less sensitive to higher-frequency disturbances caused by the SM capacitor voltage ripples regarding the PS-MPC and the LQR.

The proposed KF harmonic compensator provided a better attenuation of the third and fifth voltage harmonic components, reducing the current WTHD from 0.7 % to 0.55 % compared to the PR-based strategy. However, the FCS-MPC strategy [103] demonstrated a slightly lower current THD, possibly due to its different cost function, which only penalizes current tracking errors, resulting in more aggressive current tracking than [105].

Based on these results, it is concluded that both PR- and KF-based compensation strategies offer similar steady-state performances for FCS-MPC schemes. In this sense, compensating voltage disturbances of higher-order harmonics may not be critical for steady-state error compensation in FCS-MPC strategies with a high sampling frequency, even if the SM capacitor voltages are assumed to be constant.

PS-MPC

The experimental results for this M^{2}PC technique are presented in Fig. 3.5(f)-(j) and Fig. 3.6(f)-(j) for the PR- and KF-based compensation strategies, respectively. Despite the high sampling frequency of 12 kHz applied in the PS-MPC, its steady-state performance was severely affected by considering the average SM capacitor voltages instead of the actual SM capacitor voltage measurements to calculate the optimal modulating signals. The current harmonic spectrums shown in Figs. 3.5(j) and 3.6(j) exhibit significant harmonic components at 150 Hz and 250 Hz, for the scenarios without compensation strategies. This disadvantage of the PS-MPC compared to the FCS-MPC is caused by the higher weighting factor λ_u, which is required to deal with the higher frequency measurement noise [89]. Therefore, errors in the calculation of $\boldsymbol{u}^{\star}(k{+}1)$ are more likely to deteriorate the steady-state current tracking performance under this control scheme.

The PR-based compensation strategy cannot properly mitigate the third and fifth harmonic voltage disturbances. Thus, these disturbances propagate into the arm currents as shown in Fig. 3.5(j). On the other hand, the proposed KF harmonic compensator allows the PS-MPC strategy to completely reject the fundamental and higher-order voltage disturbances. As a result, the proposed KF harmonic compensator outperforms the PR-based compensation strategy for this optimal control scheme, reducing the output current THD and WHTD in 1.29 % and 0.6 %, respectively [see Figs. 3.5(i) and 3.6(i)].

LQR

An LQR was implemented to obtain the CHB converter arm modulating voltages. These voltages were applied to the HB-SMs by implementing the proposed OVA-PS-PWM strategy introduced in the previous chapter, with the sampling technique [72]. The proposed modulation strategy allows the implementation of the current controller at a reduced sampling frequency of 4 kHz while maintaining the same PWM carrier frequency used in the PS-MPC strategy. Nevertheless, the slower sampling frequency and the assumption of the SM capacitor voltages being constant values impacted the steady-state performance of the LQR without compensation methods. Indeed, the LQR without steady-state error compensation strategy presented the poorest disturbance rejection for the third and fifth voltage harmonics compared to the previous optimal controllers, as shown in Figs. 3.5(o) and 3.6(o).

After enabling the steady-state compensation strategies, results similar to those of the PS-MPC were obtained. On the one hand, the LQR with the PR-based compensation strategy proposed in [103] could not compensate for higher-order harmonic disturbances propagated into the converter currents. On the other hand, the LQR with the proposed KF harmonic compensator drastically attenuated these voltage disturbances.

Table 3.3 summarizes the magnitude of the third and fifth harmonic components of i_a for each control strategy. These results demonstrate that the proposed KF harmonic compensator provided a superior disturbance rejection at these specific frequencies compared to both the absence of compensation and the PR-based scheme [103] for each optimal control scheme.

Additionally, Table 3.4 summarizes the steady-state performance of each optimal control strategy in terms of output current THD, the root mean square error (RMSE) for the arm current references tracking, and also details the computational burden observed on the control platform for each control scheme. This Table and Fig. 3.6(o) show that the smallest RMSE and output current THD among all the tested control strategies were obtained for the LQR with the proposed KF harmonic compensator and the OVA-PS-PWM stage. However, note from Table 3.3 that the magnitude of the third and fifth harmonic components was the same for the PS-MPC and LQR schemes when combined with the KF strategy.

In this way, the slightly superior performance of the LQR over the PS-MPC was given

Table 3.3: Third and fifth harmonic components of i_a for each control scheme and compensation technique.

Control	FCS-MPC			PS-MPC			LQR		
Compensation	-	PR	KF	-	PR	KF	-	PR	KF
150 Hz (%)	2.63	1.57	1.27	3.52	2.35	0.53	6.90	6.45	0.53
250 Hz (%)	1.18	0.73	0.41	1.60	1.21	0.35	2.44	2.40	0.35

Table 3.4: Comparison for the output currents THD, RMSE for the steady-state arm current references tracking, and computational burden. The CPU load is expressed in the percentage of the sampling period used by the control strategy.

Control System	THD_i	RMSE	CPU Load	Execution T.
FCS-MPC-PR	3.45%	0.234	51.43%	51.43 us
FCS-MPC-KF	3.8%	0.237	51.48%	51.48 us
PS-MPC-PR	3.22%	0.220	4.89%	4.4 us
PS-MPC-KF	1.93%	0.185	5.3%	4.42 us
LQR-OVA-PWM-PR	7.28%	0.269	3.14%	7.86 us
LQR-OVA-PWM-KF	1.89%	0.123	3.18%	7.95 us

by the modulation stage. The OVA-PS-PWM provides variable PWM carrier phase-shift angles, improving the THD of the output voltage by minimizing the harmonic components at twice the carrier frequency and its multiples. This modulation strategy outperforms the conventional PS-PWM when the HB-SMs present differences in their dc voltages or ac modulating signals as shown in the previous chapter, which was the case in the SL-BESS prototype used in this work.

Regarding the computational burden of each control scheme (see Table 3.4), it is essential to highlight that the difference in execution time between implementing the PR-based steady-state error compensation strategy [10], and the proposed KF harmonic compensator was negligible, being less than 1 us. This outcome is attributed to the reduced computational complexity of the proposed steady-state KF, in which the observer gain matrix is constant and computed offline. Furthermore, the dimension of the augmented model matrices (24) does not depend on the number of SMs, and these matrices are sparse. Thus, the implementation of the state prediction and correction can be optimized to reduce the number of floating-point operations.

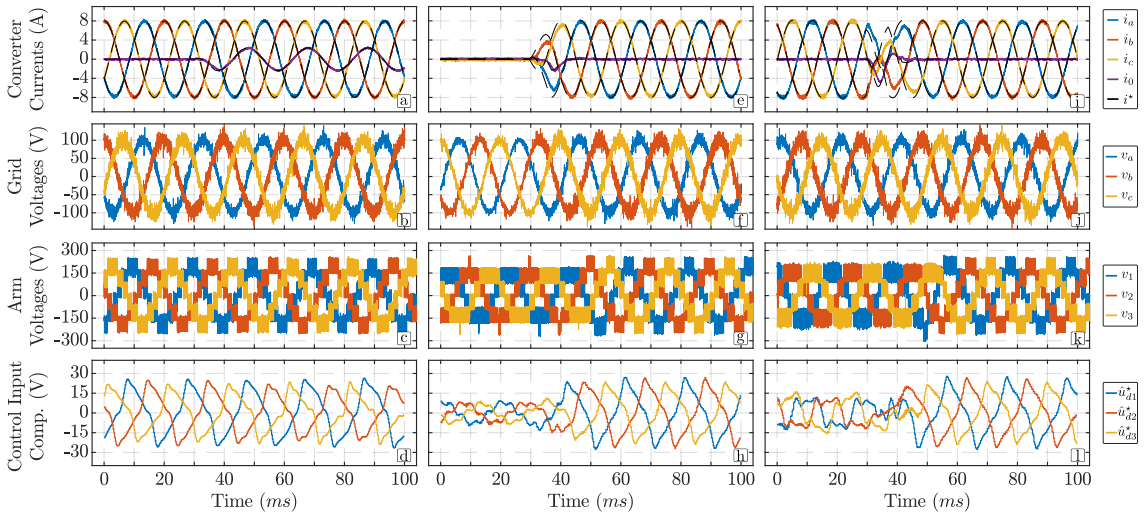


Figure 3.7: Experimental results for the proposed KF strategy under transients for an LQR. (a)-(d) shows a transient response for a circulating current step change, (e)-(h) shows an active power reference change of 1.2 kW, and (j)-(l) shows transient reversing the power flow from −1.2 kW to 1.2 kW.

It is concluded from the conducted experiments that the proposed KF harmonic compensator can eliminate the CHB converter steady-state current errors under severe parameter uncertainty and SM capacitor voltage measurement errors for direct and indirect MPC schemes. Moreover, the proposed KF harmonic compensator outperforms the existing PR-based solution in modulated optimal control techniques, as it enables a major disturbance rejection for the required higher-order voltage harmonic components.

3.4.3 Transient Performance

Three transient tests were carried out to assess the dynamic response of the proposed KF strategy. Due to its improved steady-state performance, the LQR current control strategy was implemented in this section. The SM capacitor voltages were assumed to be equal to the average battery voltage for these experiments. The first transient test is given by a circulating current transient to introduce an inter-arm power imbalance. The arm powers were modified from P_1=P_2=P_3=400 W, to P_1=500 W, P_2=200 W, and P_3=500 W; thus, maintaining a constant output power of 1.2 kW. The second experiment consisted of a ramp change in the three-phase active power reference from 0 kW to 1.2 kW, and the third test involved power flow inversion from −1.2 kW to 1.2 kW. The results for

each experiment are shown in each column of Fig. 4.8, in which each reference change was introduced at $t = 30\,\text{ms}$. The LQR current control combined with the proposed KF harmonic compensator demonstrated satisfactory dynamic performance in each test. From these experiments, it is demonstrated that the proposed KF strategy does not increase the overshoot of the current control, and it allows the controller to reach the current references without steady-state error or undesired harmonic distortion introduced by the SM capacitor voltage ripples.

3.5 Conclusions

In this chapter, a KF harmonic compensator to achieve an offset-free optimal control of CHB converters in SL-BESS applications has been proposed. The proposed KF strategy is based on an augmented linear state space model, which considers sinusoidal voltage disturbances of different harmonic components that affect the arm currents dynamics. These disturbances represent the equivalent voltage drops at the converter arms caused by modeling errors. Accordingly, the proposed KF observer estimates these voltage disturbances, allowing the calculation of a corrected steady-state control input reference and improving the arm current predictions.

Experimental results for a three-phase CHB-SL-BESS prototype have verified the effectiveness of the proposed KF harmonic compensator, tested with the FCS-MPC, PS-MPC, and LQR control strategies. These results show that the proposed KF strategy can completely eliminate the steady-state error introduced by significant model parameters and SM capacitor voltage measurement errors. Moreover, the proposed KF strategy demonstrated a satisfactory dynamic response without introducing overshoot at the output currents during transients.

In addition, for modulated optimal control strategies, the experimental results showed that the proposed KF harmonic compensator can outperform the steady-state compensation technique that combines an optimal control strategy with a PR controller. In particular, the best steady-state performance in terms of output current THD and WTHD was obtained by the LQR with the proposed KF and OVA-PS-PWM strategies. Moreover, this superior harmonic performance was obtained despite the assumption of constant SM capacitor voltages.

Therefore, the proposed KF strategy is a suitable solution for improving the steady-state performance of optimal controllers under model parameter uncertainty scenarios. This KF strategy can be easily added to existing optimal control schemes for CHB converters with and without a PWM stage. Additionally, by allowing the operation of the CHB-SL-BESS prototype without requiring SM capacitor voltage sensors for the FCS-MPC and LQR control strategies, the proposed harmonic compensator combined with these optimal control strategies can reduce the converter hardware complexity and measurement requirements for this particular application.

Chapter 4

Dual-Stage MPC for SoC Balancing in SL-BESS Based on Δ-CHB Converters

4.1 Introduction

After addressing the PS-PWM issues and the optimal current control steady-state error issues in the CHB converter, which can introduce low-frequency harmonic distortion components in the converter currents in practical CHB-SL-BESS applications, this chapter focuses on the main objective of the research project at hand. This objective aims to develop a novel MPC strategy that balances the SoC among SLBs in a Δ-CHB converter by regulating the inter-arm and -SM power imbalances while maintaining the BESS within its safe operation range.

As discussed in the first chapter, due to the wide range of capacity values that might exist among SLBs, the SoC balancing control problem is a critical task in CHB-SL-BESS. Indeed, without an adequate SoC balance control, the battery with the lowest capacity might reach its minimum SoC threshold considerably faster than the others, limiting the performance of the BESS [33]. Furthermore, achieving the SoC balance through a suitable unbalanced power distribution among the SMs while tracking the converter three-phase power references poses additional challenges in the control system [66].

To develop energy balancing control schemes for three-phase CHB-BESS, the inter-SM

and -arm power imbalance problems are often examined separately [32]. However, their energy-balancing control loops are not fully decoupled. Therefore, implementing independent controllers for the inter-SM and inter-arm SoC balance can result in overmodulation issues or violate the CHB-BESS power ratings [118].

Several works for single-phase CHB converters have been proposed to balance the inter-SM SoCs by adding a fundamental frequency ac component to each SM modulating signal, enforcing the uneven power distribution among SMs. In [65], [76], [77], PI regulators are used to compute the magnitude of these ac voltage components based on the errors between each battery SoC and the arm average SoC. Nevertheless, the controller gains selection becomes challenging for SLBs, due to the difference between battery capacities. Besides, large SoC balance errors in these methods can impact the CHB converter current control or result in high currents that can break the safe power limits of some BPs [70].

Sorting techniques [73], [79], [80] offer a different approach for balancing the inter-SM SoC. These methods select which SMs in the arm are inserted at each sampling instant, prioritizing the insertion of the SMs with the largest SoC imbalance while considering the arm current sign and its voltage reference. Although these methods provide a fast balancing speed, they cannot guarantee that the BPs are operated within their safe power limits [112].

Advanced inter-SM balance methods for CHB converters, such as the rule-based method (RBM) [70], and the MPC strategy [112] have been recently proposed to mitigate these issues. In these control strategies, the active power references for each SM are directly computed while considering the power limits of individual BPs. Nevertheless, these proposals require a separate sorting algorithm with a PS-PWM stage to track the SM power references. The MPC strategy [112] provides a faster SoC balance and reduced steady-state error caused by model parameter uncertainties compared with the RBM [70]. However, a standard MPC strategy provides an unconstrained solution similar to a dead-beat control (see, Ch. 3.2.4 in [119]). Thus, this approach becomes sensitive to small errors in the SoC estimation, which are a common issue in Lithium-ion BMS [120]. Additionally, a high carrier frequency for the PS-PWM stage is required in these approaches, as combining a sorting stage that aggressively modifies the modulating signals between sampling instants can deteriorate the harmonic performance of the conventional PS-PWM strategy, as analyzed in chapter 2.

For three-phase CHB converters, the inter-arm power imbalance capabilities of the Y-CHB and Δ-CHB converters have been analyzed in the field of solar photovoltaic power plants [32]. The Δ-CHB converter offers superior inter-arm power balancing capabilities without requiring significant voltage or current overrating. In addition, the circulating current injection in the Δ-CHB can allow the control system to balance the SoC among batteries without exchanging power with the electrical grid [66]. Therefore, this configuration becomes more attractive for CHB-SL-BESS. Remarkably, SoC balancing techniques for the Δ-CHB converter in BESS applications have not been examined with experimental results to this date, unlike previous works presented for the Y-CHB [33], [121], [122].

Motivated by the discussion above, this chapter proposes a dual-stage model predictive control (DS-MPC) strategy to balance the SoC among SLB packs directly connected to the SMs in a Δ-CHB-based SL-BESS. The proposed DS-MPC scheme is formulated by considering the arm currents and the SM modulating signals in the single-phase synchronous dq-frame. As a result, the impact of these control variables becomes explicit in the SoC state equations, describing the couplings between the inter-SM and inter-arm power imbalance problems. Moreover, the slow SoC dynamics, given by the large battery capacities, and the constant value of steady-state signals in the synchronous dq-frame allow the implementation of the proposed DS-MPC strategy at a slower sampling rate than the current controller without requiring fast communications.

The first stage of the proposed DS-MPC strategy uses the derived synchronous dq-frame model to compute an optimal circulating current reference for the Δ-CHB converter. Subsequently, in the following sampling instant, the second stage updates the proposed model with new measurements and computes optimal modulating signals for each SM. An equality constraint is imposed to preserve the resulting arm reference voltages obtained by the current controller. In this way, the optimal modulating signals do not distort the converter currents and are applied to a PS-PWM stage in a feed-forward fashion. Additional safety constraints are included in both optimization stages, resulting in a rapid SoC balance that avoids overmodulation and does not violate the maximum current limits of the SLB packs and the Δ-CHB converter arms.

In contrast with the inter-SM SoC balance MPC technique applied to a single-phase CHB converter [112], the proposed DS-MPC strategy tackles both inter-SM and inter-arm power imbalance problems for Δ-CHB converters by using a novel modeling frame and

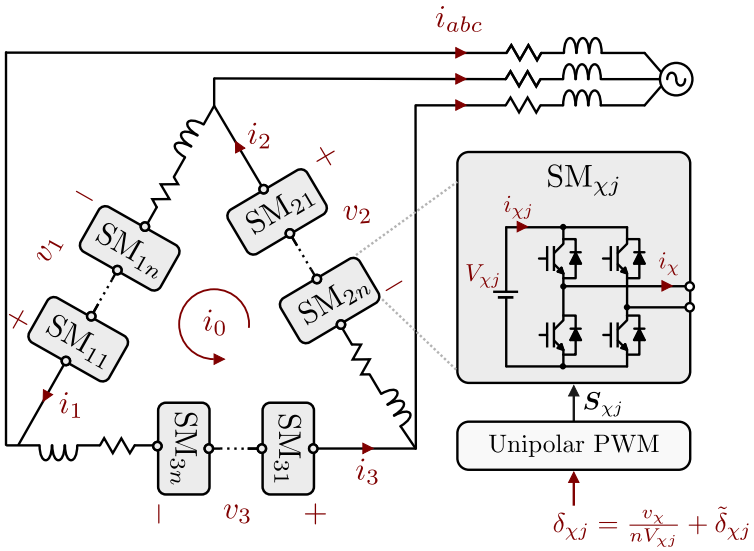


Figure 4.1: Current and voltage definitions for the three-phase Δ-CHB converter topology with n SMs per arm and batteries directly connected to each SM analyzed in this chapter.

introducing control input constraints that facilitate the sequential dual-stage implementation. Moreover, the proposed DS-MPC strategy includes an additional term in its cost functions to regulate the controller bandwidth and to enhance the controller disturbance rejection against SoC estimation errors.

In addition, the proposed DS-MPC modeling framework eliminates the need for an external sorting stage to control SM average powers. In fact, it can be directly implemented with the proposed OVA-PS-PWM and KF harmonic compensator strategies introduced in previous chapters. As a result, the combination of these control schemes achieves the optimal SoC balance control among SLBs, the offset-free control of the Δ-CHB converter currents, and it maintains a reduced output voltage harmonic distortion without increasing the PWM carrier frequency, even under highly unbalanced power distributions among SMs.

4.2 SoC Balancing in Δ-CHB Converters

In this chapter, the three-phase Δ-CHB converter topology discussed in chapter 3 is also considered. Figure 4.1 highlights the key signals of interest for this converter in the context of the proposed DS-MPC strategy. To analyze the inter-arm power flow capabilities of the converter, the arm currents $\boldsymbol{i}_{123} = [i_1 \;\; i_2 \;\; i_3]^T$, can be divided into two independent

components. The first component $\breve{\boldsymbol{\imath}}_{123} = [\breve{\imath}_1 \quad \breve{\imath}_2 \quad \breve{\imath}_3]^T$ is related with the grid currents, $\boldsymbol{i}_{abc} = [i_a \;\; i_b \;\; i_c]^T$. The second component is a circulating current, i_0, which flows through the arms without appearing in the output currents [32]. Accordingly, the Δ-CHB arm currents can be expressed via:

$$\boldsymbol{i}_{123}(t) = \breve{\boldsymbol{\imath}}_{123}(t) + \mathbf{1}_{3\times 1} i_0(t), \tag{4.1}$$

with

$$\breve{\boldsymbol{\imath}}_{123}(t) = \frac{1}{3}\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \boldsymbol{i}_{abc}(t). \tag{4.2}$$

4.2.1 Discrete-Time SoC Dynamic Model

The SoC of the j-th battery in the arm-χ, $\text{SoC}_{\chi j} \in \mathbb{Z} \triangleq [0,1]$ with $\chi \in \{1,2,3\} \triangleq \mathbb{X}$, and $j \in \{1,\ldots,n\} \triangleq \mathbb{J}$, represents the available battery capacity, regarding its maximum capacity $Q_{\chi j}$[1]. The discrete-time SoC dynamics for each battery pack can be described as [120]:

$$\text{SoC}_{\chi j}(k+1) = \text{SoC}_{\chi j}(k) - \frac{1}{Q_{\chi j}} \int_{kT_s}^{(k+1)T_s} i_{\chi j}(\tau) d\tau, \tag{4.3}$$

where $i_{\chi j}$ is the instantaneous battery current, and T_s is the controller sampling time. Considering the direct connection of each battery to an H-bridge SM, and taking advantage of the PS-PWM strategy, the instantaneous battery current can be represented in terms of the arm current and the SM modulating signal, $\delta_{\chi j} \in \mathbb{D} \triangleq [-1,1]$, as:

$$i_{\chi j}(t) = \delta_{\chi j}(t) i_{\chi}(t), \tag{4.4}$$

where $\delta_{\chi j}$ is the SM modulating signal.

Each battery current contains a dc-component, $\bar{\imath}_{\chi j}$, and an ac-component pulsating

[1]Note that ampere-seconds (As) are considered in the equations displayed in this chapter to represent battery capacity.

at twice the fundamental frequency, $\tilde{\imath}_{\chi j}$. Battery capacities usually exhibit a large value, e.g., dozens or hundreds of Ah. Therefore, the effect of $\tilde{\imath}_{\chi j}$ is negligible in the SoC state equation[2]. In this sense, only estimating $\bar{\imath}_{\chi j}$ becomes relevant in (4.3) for SoC control purposes. By neglecting $\tilde{\imath}_{\chi j}$ and assuming a constant dc component in the battery current within sampling instants, the SoC state equation can be expressed via:

$$\mathrm{SoC}_{\chi j}(k+1) = \mathrm{SoC}_{\chi j}(k) - \frac{T_s}{Q_{\chi,j}}\bar{\imath}_{\chi j}(k), \tag{4.5}$$

Furthermore, $\bar{\imath}_{\chi j}$ can be computed, similar to the active power calculation in single-phase power systems, by using the single-phase synchronous dq-frame components for the modulating signals and the arm current as follows:

$$\bar{\imath}_{\chi j}(t) = \frac{1}{2}\left(\boldsymbol{\delta}_{\chi j}^{dq}(t)\right)^T \boldsymbol{i}_{\chi}^{dq}(t), \tag{4.6}$$

with $\boldsymbol{\delta}_{\chi j}^{dq} = \left[\delta_{\chi j}^{d}\ \delta_{\chi j}^{q}\right]^T \in \mathbb{D}^2$, and $\boldsymbol{i}_{\chi}^{dq} = \left[i_{\chi}^{d}\ i_{\chi}^{q}\right]^T \in \mathbb{R}^2$ the SM modulating signal and arm current vectors in the single-phase dq-frame, respectively. Replacing (4.6) into (4.5), leads to:

$$\mathrm{SoC}_{\chi j}(k+1) = \mathrm{SoC}_{\chi j}(k) - \rho_{\chi j}\left(\boldsymbol{\delta}_{\chi j}^{dq}(k)\right)^T \boldsymbol{i}_{\chi}^{dq}(k), \tag{4.7}$$

with $\rho_{\chi j} = \frac{T_s}{2Q_{\chi j}}$. Moreover, this expression can be rewritten by considering the arm current decomposition (4.1) via:

$$\mathrm{SoC}_{\chi j}(k+1) = \mathrm{SoC}_{\chi j}(k) - \rho_{\chi j}\left(\boldsymbol{\delta}_{\chi j}^{dq}(k)\right)^T \left(\breve{\boldsymbol{\imath}}_{\chi}^{dq}(k) + \boldsymbol{i}_{0}^{dq}(k)\right). \tag{4.8}$$

From this expression, it is clear that changing the circulating current reference to modify the inter-arm power imbalance also impacts the inter-SM power imbalance by changing the average current that flows at each battery of the Δ-CHB-BESS. However, computing optimal modulating signals and a circulating current to balance the SoC using (4.8) is challenging. In fact, the product between the SM modulating signals and the circulating current, which are control variables, makes this expression a non-linear dynamic model. In this sense, the next section introduces the proposed DS-MPC strategy, which linearizes

[2]Besides, the current ripples in the battery ports of CHB converters generally have a negligible influence on battery aging [34].

(4.8) and obtains the optimal battery currents by solving two sequential optimization problems.

4.3 Proposed Dual-Stage MPC Strategy for SoC Balancing in Δ-CHB-BESS

This section introduces the proposed DS-MPC strategy for SoC balancing in Δ-CHB-BESS. A control diagram of this proposal is shown in Fig. 4.2, where the two required optimization stages are depicted. The inter-arm energy balance optimization stage computes the circulating current reference for the Δ-CHB converter, whereas the inter-SM energy optimization stage computes modulating signal values for each arm, which are added to the ones calculated by the current control loop in a feed-forward fashion.

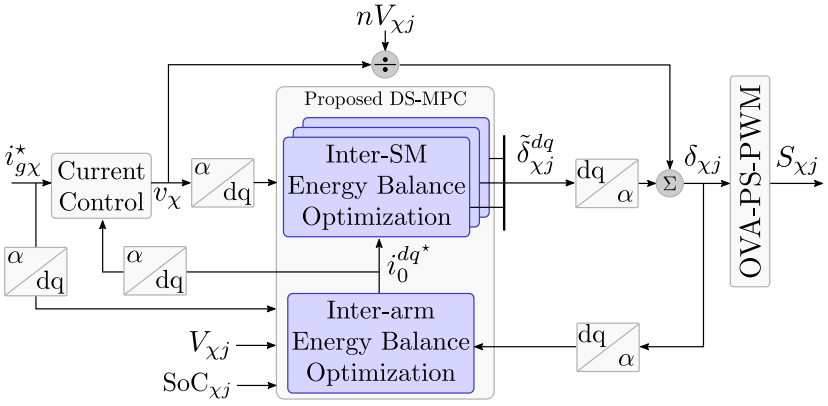


Figure 4.2: Proposed DS-MPC scheme for optimal SoC balancing in Δ-CHB-BESS.

The proposed DS-MPC strategy is designed to tackle each optimization stage in consecutive sampling instants rather than solving them simultaneously. Accordingly, each optimization stage measures the current steady-state operating point of the Δ-CHB-BESS and considers the solution from the preceding optimization to compute new optimal incremental changes to the battery currents without violating the safe range of operation.

It is important to remark that the SoC dynamics of each battery present a slow response compared with the converter current control. Indeed, several minutes can be required to compensate for SoC imbalances due to the large battery capacity values. In this sense, the execution rate for the proposed DS-MPC technique can be significantly slower than the current controller sampling time. Moreover, the proposed DS-MPC strategy takes

advantage of the constant dc nature of the steady-state converter measurements in the single-phase synchronous dq-frame, avoiding fast communication requirements with the current controller. As a result, the proposed DS-MPC strategy can be implemented in a dedicated core with a slow sampling frequency, e.g., 2 Hz, decoupling the computational requirements of this strategy from the converter current controller.

4.3.1 Proposed Inter-arm Energy Balance Optimization Stage

System State and Linearized Model

The following system state that includes the SoC of each battery in the Δ-CHB-BESS is considered for this optimization stage:

$$\mathbf{SoC}(k) = \begin{bmatrix} \mathbf{SoC}_1^T(k) & \mathbf{SoC}_2^T(k) & \mathbf{SoC}_3^T(k) \end{bmatrix}^T \in \mathbb{Z}^{3n}, \tag{4.9}$$

where $\mathbf{SoC}_\chi(k) = [\mathrm{SoC}_{\chi 1}(k) \ \cdots \ \mathrm{SoC}_{\chi n}(k)]^T \in \mathbb{Z}^n$ is the vector containing the SoC estimate of each battery pack in the arm-χ. Besides, the Δ-CHB circulating current in the single-phase rotating synchronous dq-frame, $\boldsymbol{i}_0^{dq}(k) \in \mathbb{R}^2$, is defined as the system control input for this stage.

Consequently, the following affine discrete-time model can be obtained from (4.8) by considering that the grid current references and modulating signals of each SM in the dq-frame remain constant within sampling instants:

$$\mathbf{SoC}(k+1) = \mathbf{SoC}(k) + \boldsymbol{B}_{i0}\left(\boldsymbol{\delta}^{dq}(k)\right)\boldsymbol{i}_0^{dq}(k) + \boldsymbol{\epsilon}_{i0}(k), \tag{4.10}$$

with

$$\begin{aligned}
\boldsymbol{B}_{i0}\left(\boldsymbol{\delta}^{dq}\right) &= \begin{bmatrix} \boldsymbol{B}_{i0}^T(\boldsymbol{\delta}_1^{dq}) & \boldsymbol{B}_{i0}^T(\boldsymbol{\delta}_2^{dq}) & \boldsymbol{B}_{i0}^T(\boldsymbol{\delta}_3^{dq}) \end{bmatrix}^T \in \mathbb{R}^{3n\times 2}, \\
\boldsymbol{B}_{i0}(\boldsymbol{\delta}_\chi^{dq}) &= -\begin{bmatrix} \rho_{\chi 1}\boldsymbol{\delta}_{\chi 1}^{dq} & \dots & \rho_{\chi n}\boldsymbol{\delta}_{\chi n}^{dq} \end{bmatrix}^T \in \mathbb{R}^{n\times 2}, \\
\boldsymbol{\epsilon}_{i0} &= \begin{bmatrix} \boldsymbol{B}_{i0}(\boldsymbol{\delta}_1^{dq}) & \mathbf{0}_{n\times 2} & \mathbf{0}_{n\times 2} \\ \mathbf{0}_{n\times 2} & \boldsymbol{B}_{i0}(\boldsymbol{\delta}_2^{dq}) & \mathbf{0}_{n\times 2} \\ \mathbf{0}_{n\times 2} & \mathbf{0}_{n\times 2} & \boldsymbol{B}_{i0}(\boldsymbol{\delta}_3^{dq}) \end{bmatrix} \begin{bmatrix} \breve{\boldsymbol{i}}_1^{dq} \\ \breve{\boldsymbol{i}}_2^{dq} \\ \breve{\boldsymbol{i}}_3^{dq} \end{bmatrix} \in \mathbb{R}^{3n}.
\end{aligned} \tag{4.11}$$

Cost Function and Constraints

The control objective of the inter-arm energy optimization stage in this work is to balance the average SoC of each arm, using the effect of the circulating current at each battery current. Besides, maximum battery charging/discharging currents and arm current constraints are needed to operate the Δ-CHB-BESS safely.

To balance the average SoC at each arm using the Δ-CHB circulating current, the following quadratic cost function is introduced:

$$J^{i0}(k) = \left\| \overline{\mathbf{SoC}}(k+1) - \overline{\mathbf{SoC}}^{\star}(k+1) \right\|_2^2 + \lambda_u^{i0} \left\| \boldsymbol{i}_0^{dq}(k) - \boldsymbol{i}_{0,ss}^{\star}(k) \right\|_2^2 \tag{4.12}$$

$$\overline{\mathbf{SoC}}(k) = \boldsymbol{C}\mathbf{SoC}(k), \quad \boldsymbol{C} = \frac{1}{n} \begin{bmatrix} \mathbf{1}_{1\times n} & \mathbf{0}_{1\times n} & \mathbf{0}_{1\times n} \\ \mathbf{0}_{1\times n} & \mathbf{1}_{1\times n} & \mathbf{0}_{1\times n} \\ \mathbf{0}_{1\times n} & \mathbf{0}_{1\times n} & \mathbf{1}_{1\times n} \end{bmatrix}, \tag{4.13}$$

where $\overline{\mathbf{SoC}}(k) = \begin{bmatrix} \overline{\mathrm{SoC}}_1(k) & \overline{\mathrm{SoC}}_2(k) & \overline{\mathrm{SoC}}_3(k) \end{bmatrix}^T \in \mathbb{Z}^3$, is the vector containing the average SoC of each arm. The first term in $J^{i0}(k)$ penalizes the tracking error of each arm average SoC with the arm SoC reference. Conversely, the second term penalizes the control effort. Therefore, the weighing factor selection of λ_u^{i0} allows the designer to regulate the controller bandwidth, similarly to the predictive control strategy [115]. As follows, the optimal circulating current reference can be obtained by solving the following constrained optimization problem:

$$\boldsymbol{i}_0^{dq,\mathrm{opt}}(k) = \arg \left\{ \min_{\boldsymbol{i}_0^{dq}(k) \in \mathbb{R}^2} J^{i0}(k) \right\} \tag{4.14}$$

subject to:

$$\mathbf{SoC}(k+1) = \mathbf{SoC}(k) + \boldsymbol{B}_{i0}\left(\boldsymbol{\delta}^{dq}(k)\right) \boldsymbol{i}_0^{dq}(k) + \boldsymbol{\epsilon}_{i0}(k) \tag{4.15a}$$

$$i_{\chi j}^{\min} \leq \frac{1}{2}\left(\boldsymbol{\delta}_{\chi j}^{dq}(k)\right)^T \left(\breve{\boldsymbol{\imath}}_{\chi}^{dq}(k) + \boldsymbol{i}_0^{dq}(k)\right) \leq i_{\chi j}^{\max} \tag{4.15b}$$

$$\boldsymbol{\Psi}_{dq}^{\alpha}\left[\breve{\boldsymbol{\imath}}_{\chi}^{dq}(k) + \boldsymbol{i}_0^{dq}(k)\right] \leq \mathbf{1}_{20\times 1} i_{\mathrm{arm}}^{\max} \tag{4.15c}$$

$$\boldsymbol{i}_0^{dq}(k-1) - \mathbf{1}_{2\times 1}\Delta u_{i0}^{\max} \leq \boldsymbol{i}_0^{dq}(k) \leq \boldsymbol{i}_0^{dq}(k-1) + \mathbf{1}_{2\times 1}\Delta u_{i0}^{\max} \tag{4.15d}$$

for all $\chi \in \mathbb{X}$, and $j \in \mathbb{J}$. In this optimization problem, (4.15a)-(4.15c) encompasses the physical power converter constraints and the safety current limits for the Δ-CHB-BESS. In particular, (4.15b) limits each battery current within its safe operating ratings, whereas (4.15c) limits the peak current value of each arm current to $i_{\text{arm}}^{\max}$, given the H-bridge SMs power rating. The matrix $\boldsymbol{\Psi}_{dq}^{\alpha}$ transforms a vector from the synchronous dq-frame into a vector containing sampled values of the equivalent steady-state single-phase signal for a complete fundamental period, i.e.:

$$\boldsymbol{\Psi}_{dq}^{\alpha} = \begin{bmatrix} \sin(\omega_0 0 T_{\text{step}}) & \cos(\omega_0 0 T_{\text{step}}) \\ \vdots & \vdots \\ \sin(\omega_0 19 T_{\text{step}}) & \cos(\omega_0 19 T_{\text{step}}) \end{bmatrix} \in \mathbb{R}^{20\times 2}, \tag{4.16}$$

with $T_{\text{step}} = 0.001\,\text{s}$, and $\omega_0 = 2\pi 50\,\text{rad/s}$ considered in this work.

The last constraint (4.15d) limits the rate of change for the optimal circulating current reference between consecutive inter-arm optimizations, i.e., the dq-components of the circulating current reference cannot be modified by a value larger than $\pm\Delta u_{i0}^{\max}$. In this way, when the proposed DS-MPC SoC balancing strategy is enabled, this constraint prevents the battery currents and/or arm current constraints from becoming active after the first execution of the inter-arm energy balance optimization. Therefore, the inter-SM SoC optimization stage can update the battery currents in the following sampling instant before any Δ-CHB-BESS safety constraint becomes active, allowing the individual battery currents to be adjusted to minimize both the inter-arm and inter-SM SoC imbalance.

Finally, by replacing (4.15a) into $J^{i0}(k)$ and omitting all the terms that do not depend on $\boldsymbol{i}_0^{dq}(k)$, the cost function can be rewritten in the standard quadratic programming (QP) form:

$$J^{i0}(k) = \frac{1}{2}\left(\boldsymbol{i}_0^{dq}(k)\right)^T \boldsymbol{W}_{i0}(k)\boldsymbol{i}_0^{dq}(k) + \boldsymbol{F}_{i0}^T(k)\boldsymbol{i}_0^{dq}(k), \tag{4.17}$$

where,

$$\begin{aligned}
\boldsymbol{W}_{i0}(k) &= \boldsymbol{B}_{i0}^{T}\left(\boldsymbol{\delta}^{dq}(k)\right)\boldsymbol{C}^{T}\boldsymbol{C}\boldsymbol{B}_{i0}\left(\boldsymbol{\delta}^{dq}(k)\right) + \lambda_{u}^{io}\boldsymbol{I}_{2\times 2},\\
\boldsymbol{F}_{i0}(k) &= \boldsymbol{B}_{i0}^{T}\left(\boldsymbol{\delta}^{dq}(k)\right)\boldsymbol{C}^{T}\boldsymbol{C}\boldsymbol{\gamma}_{i0}(k) - \lambda_{u}^{io}\boldsymbol{i}_{0,ss}^{\star}(k),\\
\boldsymbol{\gamma}_{i0}(k) &= \mathbf{SoC}(k) - \mathbf{SoC}^{\star}(k+1) + \boldsymbol{\epsilon}_{i0}(k).
\end{aligned} \tag{4.18}$$

Consequently, this standard form can be used to solve this optimization problem with any standard QP solver [123].

Average Arm SoC Reference Design

By neglecting the battery and SM losses in (4.5), the $\mathrm{SoC}_{\chi j}$ can be expressed in terms of their SM average active power, as follows:

$$\mathrm{SoC}_{\chi j}(k+1) = \mathrm{SoC}_{\chi j}(k) - T_s\frac{P_{\chi j}(k)}{\alpha_{\chi j}(k)}, \tag{4.19}$$

with $\alpha_{\chi j}(k) = Q_{\chi j}V_{\chi j}(k)$, $P_{\chi j}(k) = V_{\chi j}(k)\bar{\imath}_{\chi j}(k)$, and $V_{\chi j}$ the battery voltage. Multiplying both sides of (4.19) by $\alpha_{\chi j}(k)$, and adding the resulting equations for each battery in the Δ-CHB-BESS leads to:

$$\sum_{\chi=1}^{3}\sum_{j=1}^{n}\alpha_{\chi j}(k)\mathrm{SoC}_{\chi j}(k+1) = \sum_{\chi=1}^{3}\sum_{j=1}^{n}\alpha_{\chi j}(k)\mathrm{SoC}_{\chi j}(k) - T_s\sum_{\chi=1}^{3}\sum_{j=1}^{n}P_{\chi j}(k), \tag{4.20}$$

where $\sum_{\chi=1}^{3}\sum_{j=1}^{n}P_{\chi j}(k)$, can be considered as the three-phase active power reference for the Δ-CHB-BESS, $P^{\star}(k)$, by neglecting the power losses. Moreover, assuming that the SoC balance is achieved for every SLB in the next sampling instant, i.e., $\mathrm{SoC}_{\chi j}(k+1) = \mathrm{SoC}^{\star}(k+1)\,\forall\,\chi\in\mathbb{X}$, $j\in\mathbb{J}$, and replacing this assumption into (4.20) yields to:

$$\mathrm{SoC}^{\star}(k+1) = \frac{\sum_{\chi=1}^{3}\sum_{j=1}^{n}\alpha_{\chi j}(k)\mathrm{SoC}_{\chi j}(k)}{\alpha_{\mathrm{BESS}}(k)} - \frac{T_s P^{\star}(k)}{\alpha_{\mathrm{BESS}}(k)} \tag{4.21}$$

with $\alpha_{\mathrm{BESS}}(k) = \sum_{\chi=1}^{3}\sum_{j=1}^{n}\alpha_{\chi j}(k)$. Finally, this SoC reference can be used to define $\overline{\mathbf{SoC}}^{\star}(k+1) = \mathbf{1}_{3\times 1}\mathrm{SoC}^{\star}(k+1)$ in the cost function (4.12).

Steady-State Circulating Current Reference Design

In a Δ-CHB-BESS with a balanced SoC among SLBs, each arm must operate at a power reference proportional to the ratio between the arm energy capacity and the BESS total energy capacity [33]. Accordingly, the following steady-state arm power reference is assumed in this work:

$$P_{\chi}^{\star}(k) = P^{\star}(k)\frac{\sum_{j=1}^{n}\alpha_{\chi j}(k)}{\alpha_{\text{BESS}}(k)}. \tag{4.22}$$

Moreover, taking advantage of the single-phase synchronous dq-frame, the active power of each arm can be computed as:

$$2P_{\chi}(k) = v_{\chi}^{d}(k)i_{\chi}^{d}(k) + v_{\chi}^{q}(k)i_{\chi}^{q}(k). \tag{4.23}$$

Considering the arm current decomposition (4.1), this expression can be expanded into

$$\begin{aligned} 2P_{\chi}(k) = {} & v_{\chi}^{d}(k)\breve{i}_{\chi}^{d}(k) + v_{\chi}^{q}(k)\breve{i}_{\chi}^{q}(k) \\ & + v_{\chi}^{d}(k)i_{0}^{d}(k) + v_{\chi}^{q}(k)i_{0}^{q}(k), \end{aligned} \tag{4.24}$$

with v_{χ}^{d}, and v_{χ}^{q} the dq-frame components of the arm modulating voltage reference, v_{χ}, obtained by the current controller, respectively.

Replacing $P_{\chi}^{\star}(k)$ for arm-1 and -2 into (4.24), and omitting the sampling time notation, k, in the time-variant variables for the sake of brevity, the following relationship is obtained:

$$\begin{bmatrix} 2P_1^{\star} \\ 2P_2^{\star} \end{bmatrix} = \begin{bmatrix} v_1^d & v_1^q \\ v_2^d & v_2^q \end{bmatrix} \boldsymbol{i}_0^{dq} + \frac{2}{3}\begin{bmatrix} P^{\star} \\ P^{\star} \end{bmatrix}. \tag{4.25}$$

Therefore, solving this equation system for $\boldsymbol{i}_0^{dq}$ leads to the following steady-state reference for the circulating current:

$$\boldsymbol{i}_{0,ss}^{\star}(k) = \frac{2}{\alpha_v(k)}\begin{bmatrix} v_2^q & -v_1^q \\ -v_2^d & v_1^d \end{bmatrix}\begin{bmatrix} P_1^{\star} - P^{\star}/3 \\ P_2^{\star} - P^{\star}/3 \end{bmatrix}, \tag{4.26}$$

where $\alpha_v(k) = v_1^d(k)v_2^q(k) - v_1^q(k)v_2^d(k)$. Note that by design, the SoC reference (4.21) is

achieved only when the circulating current also reaches its steady-state reference.

4.3.2 Proposed Inter-SM Energy Balance Optimization Stage

Linearized Model

The previously introduced inter-arm optimization problem considers that the modulating signals are constant within sampling instants to compute the optimal circulating current. On the contrary, the inter-SM optimization stage assumes that the arm currents remain constant and equal to their dq-frame current references. Accordingly, the inter-SM balancing stage linearizes (4.3) for each arm as follows:

$$\mathbf{SoC}_j(k+1) = \mathbf{SoC}_j(k) + \boldsymbol{B}_\delta\left(\boldsymbol{i}_\chi^{dq}(k)\right)\widetilde{\boldsymbol{\delta}}_\chi^{dq}(k) + \boldsymbol{\epsilon}_{\chi\delta}(k), \tag{4.27}$$

with

$$\widetilde{\boldsymbol{\delta}}_\chi^{dq} = \left[(\widetilde{\boldsymbol{\delta}}_{\chi 1}^{dq})^T \ \dots \ (\widetilde{\boldsymbol{\delta}}_{\chi n}^{dq})^T\right]^T \in \mathbb{D}^{2n}, \tag{4.28}$$

$$\boldsymbol{B}_\delta\left(\boldsymbol{i}_\chi^{dq}\right) = -\begin{bmatrix} \rho_{\chi 1}(\boldsymbol{i}_\chi^{dq})^T & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \ddots & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \rho_{\chi n}(\boldsymbol{i}_\chi^{dq})^T \end{bmatrix} \in \mathbb{R}^{n\times 2n}, \tag{4.29}$$

$$\boldsymbol{\epsilon}_{\delta,\chi} = \boldsymbol{B}_\delta\left(\boldsymbol{i}_\chi^{dq}\right)\begin{bmatrix} \dfrac{\left(\boldsymbol{v}_\chi^{dq}\right)^T}{nV_{\chi 1}} & \cdots & \dfrac{\left(\boldsymbol{v}_\chi^{dq}\right)^T}{nV_{\chi n}} \end{bmatrix}^T \in \mathbb{R}^n. \tag{4.30}$$

Note that in $\boldsymbol{\epsilon}_{\chi\delta}$ not only considers the arm current dq-components as known values, but also the modulating voltage reference given by the current control loop, $\boldsymbol{v}_\chi^{dq}$, which is equally distributed among SMs. As a result, the control input $\tilde{\boldsymbol{\delta}}_\chi^{dq}$ works as a feed-forward component that modifies the ac modulating signal of each SM to achieve optimal battery currents, as shown in Fig. 4.2.

Cost Function and Constraints

The linearized model (4.27) shows that the SoC state equations are independent. However, the optimal modulating signals obtained by the inter-SM optimization stage must

not distort the arm voltage references computed by the current controller. Therefore, constraints for each of the SM modulating signals that belong to the same arm must be imposed. As a consequence, the inter-SM SoC balancing problem can be tackled by solving three independent constrained optimization problems defined for each CHB arm. The following cost function is introduced to define these inter-SM optimizations:

$$J_{\chi}^{\delta}(k) = \left\|\mathbf{SoC}_{\chi}(k+1) - \mathbf{SoC}_{\chi}^{\star}(k+1)\right\|_2^2 + \lambda_u^{\delta}\left\|\widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k) - \widetilde{\boldsymbol{\delta}}_{\chi}^{\star}(k)\right\|_2^2 \tag{4.31}$$

with $\mathbf{SoC}_{\chi}^{\star}(k+1) = \mathrm{SoC}_{\chi}^{\star}(k+1)\mathbf{1}_{n\times 1} \in \mathbb{Z}^n$ the respective SoC reference vector for each arm.

Similarly to the inter-arm optimization stage, the weighing factor λ_u^{δ} is used to regulate the SoC balancing speed and the control effort. As follows, the constrained inter-SM optimization problem that obtains optimal modulating signals for the SMs of each arm is given by:

$$\widetilde{\boldsymbol{\delta}}_{\chi}^{dq,\mathrm{opt}}(k) = \arg\left\{\min_{\widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k)\in\mathbb{D}^{2n}} J_{\chi}^{\delta}(k)\right\} \tag{4.32}$$

subject to:

$$\mathbf{SoC}_j(k+1) = \mathbf{SoC}_j(k) + \boldsymbol{B}_{\delta}\left(\boldsymbol{i}_{\chi}^{dq}(k)\right)\boldsymbol{u}_{\delta\chi}^{dq}(k) + \boldsymbol{\epsilon}_{\delta\chi}(k) \tag{4.33a}$$

$$\sum_{j=1}^{n} V_{\chi j}(k)\widetilde{\boldsymbol{\delta}}_{\chi j}^{dq}(k) = \mathbf{0}_{2\times 1} \tag{4.33b}$$

$$\boldsymbol{\Psi}_{dq}^{\alpha}\left(\frac{\boldsymbol{v}_{\chi}^{dq}(k)}{nV_{\chi j}(k)} + \widetilde{\boldsymbol{\delta}}_{\chi j}^{dq}(k)\right) \leq \mathbf{1}_{20\times 1} m_a^{\max} \tag{4.33c}$$

$$i_{\chi j}^{\min} \leq \frac{1}{2}\left(\boldsymbol{i}_{\chi}^{dq}(k)\right)^T\left(\frac{\boldsymbol{v}_{\chi}^{dq}(k)}{nV_{\chi j}(k)} + \widetilde{\boldsymbol{\delta}}_{\chi j}^{dq}(k)\right) \leq i_{\chi j}^{\max} \tag{4.33d}$$

$$\widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k-1) - \mathbf{1}_{2\times 1}\Delta\delta^{\max} \leq \widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k) \leq \widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k-1) + \mathbf{1}_{2\times 1}\Delta\delta^{\max} \tag{4.33e}$$

for all $j \in \mathbb{J}$. In this problem, the equality constraint (4.33b) forces the resulting voltage given by the optimal modulating signals of the arm-χ to be equal to zero. As a result, this constraint avoids distorting the arm voltage references calculated by the current controller. Additionally, the inequality constraints (4.33c) and (4.33d) avoid the SM overmodulation and enforce the safe operation of the SLBs, limiting the maximum SM modulating index

and the battery maximum charging/discharging current, respectively. Finally, (4.33e) restricts the rate of change of the optimal control input, similar to (4.15d) for the inter-arm optimization problem. Thus, updates of the modulating signals at each execution of the inter-SM optimization cannot be greater than $\pm\Delta\delta^{\max}$. Accordingly, this constraint prevents the maximum battery current constraints from becoming active in one execution step, allowing the inter-arm optimization to adjust the battery currents in the next sampling instant.

Inter-SM SoC Reference Design

The required SoC reference can be obtained independently for each arm by assuming that all their corresponding battery SoCs become balanced in the following sampling instant, i.e., $\mathrm{SoC}_{\chi j}(k+1) = \mathrm{SoC}^{\star}_{\chi}(k+1)\,\forall\, j \in \mathbb{J}$. Following the same steps as section 4.3.1, it follows that[3]:

$$\mathrm{SoC}^{\star}(k+1) = \frac{\sum_{j=1}^{n} \alpha_{\chi j}(k)\mathrm{SoC}_{\chi j}(k)}{\alpha_{\mathrm{arm}}(k)} - \frac{T_s P^{\star}_{\chi}}{\alpha_{\mathrm{arm}}(k)}, \tag{4.34}$$

where $\alpha_{\mathrm{arm}}(k) = \sum_{j=1}^{n} Q_{\chi j} V_{\chi j}(k)$.

Steady-State SM Modulating Signals Reference Design

Following the same assumption as in the steady-state circulating current reference design, each SM needs to operate at a power reference proportional to its respective battery capacity once the SoCs are balanced. In this sense, the following steady-state SM active power reference can be considered:

$$P^{\star}_{\chi j}(k) = P^{\star}_{\chi}(k)\frac{\alpha_{\chi j}(k)}{\alpha_{\mathrm{arm}}(k)}. \tag{4.35}$$

Accordingly, battery current references are obtained as:

$$\vec{\imath}^{\star}_{\chi j}(k) = \frac{P^{\star}_{\chi j}(k)}{V_{\chi j}(k)}. \tag{4.36}$$

The following system of equations can be introduced analogously to the active and

[3]For a detailed derivation refer to [112].

reactive power calculation of single-phase power systems:

$$\begin{bmatrix} i_{\chi j}^{d,\star}(k) \\ i_{\chi j}^{q,\star}(k) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \delta_{\chi j}^{d}(k) i_{\chi}^{d}(k) + \delta_{\chi j}^{q}(k) i_{\chi}^{q}(k) \\ \delta_{\chi j}^{q}(k) i_{\chi}^{d}(k) - \delta_{\chi j}^{d}(k) i_{\chi}^{q}(k) \end{bmatrix}. \tag{4.37}$$

Ideally, the current component related to the single-phase reactive power of each battery should be zero in steady-state, in order to minimize the battery low-frequency ac current ripple. Thus, $i_{\chi j}^{q,\star}(k) = 0$, whereas $i_{\chi j}^{d,\star}(k) = \overline{\imath}_{\chi j}^{\star}(k)$. Replacing these current references and rearranging terms in (4.37), it follows that:

$$\begin{bmatrix} \overline{\imath}_{\chi j}^{\star}(k) \\ 0 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} i_{\chi}^{d}(k) & i_{\chi}^{q}(k) \\ -i_{\chi}^{q}(k) & i_{\chi}^{d}(k) \end{bmatrix} \boldsymbol{\delta}_{\chi j}^{dq}(k). \tag{4.38}$$

Moreover, considering the proposed feed-forward implementation for the inter-SM optimization shown in Fig. 4.2,

$$\boldsymbol{\delta}_{\chi j}^{dq}(k) = \left[\frac{\left(\boldsymbol{v}_{\chi}^{dq}(k)\right)^{T}}{n V_{\chi j}(k)} + \left(\tilde{\boldsymbol{\delta}}_{\chi 1}^{dq}(k)\right)^{T} \right]^{T}. \tag{4.39}$$

In this way, the modulating signal references that maintain the SoC balanced for each SM can be obtained by solving (4.38) for $\tilde{\boldsymbol{\delta}}_{\chi j}^{dq}(k)\ \forall\ j \in \mathbb{J}$. Therefore,

$$\tilde{\boldsymbol{\delta}}_{\chi}^{\star}(k) = \left[(\tilde{\boldsymbol{\delta}}_{\chi 1}^{dq,\star}(k))^{T}\ \ldots\ (\tilde{\boldsymbol{\delta}}_{\chi n}^{dq,\star}(k))^{T} \right]^{T}, \tag{4.40}$$

with

$$\tilde{\boldsymbol{\delta}}_{\chi j}^{dq,\star}(k) = \frac{2\overline{\imath}_{\chi j}^{\star}(k)}{I_{\chi}^{2}(k)} \boldsymbol{i}_{\chi}^{dq}(k) - \frac{\boldsymbol{v}_{\chi}^{dq}(k)}{n V_{\chi j}}, \tag{4.41}$$

$$I_{\chi}^{2}(k) = \left(i_{\chi}^{d}(k)\right)^{2} + \left(i_{\chi}^{q}(k)\right)^{2}. \tag{4.42}$$

Then, the cost function $J_{\chi}^{\delta}(k)$ can be written in the standard QP form by replacing (4.27) and ignoring the terms that do not depend on the control input:

$$J_{\chi}^{\delta}(k) = \frac{1}{2} \left(\widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k)\right)^{T} \boldsymbol{W}_{\chi\delta}(k) \widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k) + \boldsymbol{F}_{\chi\delta}^{T}(k) \widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k), \tag{4.43}$$

where

$$\begin{aligned}
\boldsymbol{W}_{\chi\delta}(k) &= \boldsymbol{B}_{\chi\delta}^{T}\left(\boldsymbol{i}_{\chi}^{dq}(k)\right)\boldsymbol{B}_{\chi\delta}\left(\boldsymbol{i}_{\chi}^{dq}(k)\right) + \lambda_{u}^{\delta}\boldsymbol{I}_{2\times 2},\\
\boldsymbol{F}_{\chi\delta}(k) &= \boldsymbol{B}_{\chi\delta}^{T}\left(\boldsymbol{i}_{\chi}^{dq}(k)\right)\boldsymbol{\gamma}_{\chi\delta}(k) - \lambda_{u}^{\delta}\widetilde{\boldsymbol{\delta}}_{\chi}^{\star}(k),\\
\boldsymbol{\gamma}_{\chi\delta}(k) &= \mathbf{SoC}(k) - \mathbf{SoC}^{\star}(k+1) + \boldsymbol{\epsilon}_{\chi\delta}(k).
\end{aligned} \tag{4.44}$$

Finally, Table 4.1 presents a summary of the state variables and constraints dimensions for each stage of the proposed DS-MPC strategy.

Table 4.1: Summary of the main parameters and constraints of the proposed DS-MPC. Note than an inter-SM optimization is required for each converter arm.

Description	Symbol/Definition	Dimension
Inter-arm Optimization		
State vector	$[\mathbf{SoC}_1^T \quad \mathbf{SoC}_2^T \quad \mathbf{SoC}_3^T]^T$	$\mathbb{Z}^{3n}$
Control input	$\boldsymbol{i}_0^{dq}$	$\mathbb{R}^2$
Dynamic SoC Model	$\mathbf{SoC}(k+1) = \mathbf{SoC}(k) + \boldsymbol{B}_{i0}\left(\boldsymbol{\delta}^{dq}(k)\right)\boldsymbol{i}_0^{dq}(k) + \boldsymbol{\epsilon}_{i0}(k)$	$\mathbb{Z}^{3n}$
Cost function $J^{i0}(k)$	$\left\|\overline{\mathbf{SoC}}(k+1) - \overline{\mathbf{SoC}}^{\star}(k+1)\right\|_2^2 + \lambda_u^{i0}\left\|\boldsymbol{i}_0^{dq}(k) - \boldsymbol{i}_{0,ss}^{\star}(k)\right\|_2^2$	$\mathbb{R}_{\geq 0}$
Inequality Constraints		
Max. dc battery current	$\frac{1}{2}\left(\boldsymbol{\delta}_{\chi j}^{dq}(k)\right)^T\left(\breve{\boldsymbol{i}}_{\chi}^{dq}(k) + \boldsymbol{i}_0^{dq}(k)\right) \leq i_{\chi j}^{\max}$	$\mathbb{R}^{3n}$
Min. dc battery current	$-\frac{1}{2}\left(\boldsymbol{\delta}_{\chi j}^{dq}(k)\right)^T\left(\breve{\boldsymbol{i}}_{\chi}^{dq}(k) + \boldsymbol{i}_0^{dq}(k)\right) \leq -i_{\chi j}^{\min}$	$\mathbb{R}^{3n}$
Arm current amplitude	$\boldsymbol{\Psi}_{dq}^{\alpha}\left[\breve{\boldsymbol{i}}_{\chi}^{dq}(k) + \boldsymbol{i}_0^{dq}(k)\right] \leq \mathbf{1}_{20\times 1} i_{\text{arm}}^{\max}$	$\mathbb{R}^{60}$
i_0 update upper bound	$\boldsymbol{i}_0^{dq}(k) \leq \boldsymbol{i}_0^{dq}(k-1) + \mathbf{1}_{2\times 1}\Delta u_{i0}^{\max}$	$\mathbb{R}^2$
i_0 update lower bound	$-\boldsymbol{i}_0^{dq}(k) \leq -\boldsymbol{i}_0^{dq}(k-1) + \mathbf{1}_{2\times 1}\Delta u_{i0}^{\max}$	$\mathbb{R}^2$
Inter-SM Optimization		
State vector	$\mathbf{SoC}_j$	$\mathbb{Z}^n$
Control input	$\tilde{\boldsymbol{\delta}}_{\chi}^{dq}$	$\mathbb{D}^{2n}$
Dynamic SoC Model	$\mathbf{SoC}_j(k+1) = \mathbf{SoC}_j(k) + \boldsymbol{B}_{\delta}\left(\boldsymbol{i}_{\chi}^{dq}(k)\right)\tilde{\boldsymbol{\delta}}_{\chi}^{dq}(k) + \boldsymbol{\epsilon}_{\chi\delta}(k)$	$\mathbb{Z}^n$
Cost function	$\left\|\mathbf{SoC}_{\chi}(k+1) - \mathbf{SoC}_{\chi}^{\star}(k+1)\right\|_2^2 + \lambda_u^{\delta}\left\|\widetilde{\boldsymbol{\delta}}_{\chi}^{dq}(k) - \widetilde{\boldsymbol{\delta}}_{\chi}^{\star}(k)\right\|_2^2$	$\mathbb{R}_{\geq 0}$
Equality Constraints		
Arm modulating voltage	$\sum_{j=1}^{n} V_{\chi j}(k)\tilde{\boldsymbol{\delta}}_{\chi j}^{dq}(k) = \mathbf{0}_{2\times 1}$	$\mathbb{R}^2$
Inequality Constraints		
Max. dc battery current	$\frac{1}{2}\left(\boldsymbol{i}_{\chi}^{dq}(k)\right)^T\left(\boldsymbol{\delta}_{\chi j}^{dq}(k) + \tilde{\boldsymbol{\delta}}_{\chi j}^{dq}(k)\right) \leq i_{\chi j}^{\max}$	$\mathbb{R}^n$
Min. dc battery current	$-\frac{1}{2}\left(\boldsymbol{i}_{\chi}^{dq}(k)\right)^T\left(\boldsymbol{\delta}_{\chi j}^{dq}(k) + \tilde{\boldsymbol{\delta}}_{\chi j}^{dq}(k)\right) \leq -i_{\chi j}^{\min}$	$\mathbb{R}^n$
Max. modulating index	$\boldsymbol{\Psi}_{dq}^{\alpha}\left(\boldsymbol{\delta}_{\chi j}^{dq}(k) + \tilde{\boldsymbol{\delta}}_{\chi j}^{dq}(k)\right) \leq \mathbf{1}_{20\times 1} m_a^{\max}$	$\mathbb{R}^{20n}$
$\tilde{\boldsymbol{\delta}}_{\chi j}^{dq}$ update upper bound	$\tilde{\boldsymbol{\delta}}_{\chi}^{dq}(k) \leq \tilde{\boldsymbol{\delta}}_{\chi}^{dq}(k-1) + \mathbf{1}_{2\times 1}\Delta\delta^{\max}$	$\mathbb{R}^{2n}$
$\tilde{\boldsymbol{\delta}}_{\chi j}^{dq}$ update lower bound	$-\tilde{\boldsymbol{\delta}}_{\chi}^{dq}(k) \leq -\tilde{\boldsymbol{\delta}}_{\chi}^{dq}(k-1) + \mathbf{1}_{2\times 1}\Delta\delta^{\max}$	$\mathbb{R}^{2n}$

4.4 Control Effort Analysis and Simulation Results

This section analyses the unconstrained solution of the inter-SM optimization stage to provide further insight into the proposed DS-MPC strategy. Moreover, simulations are carried out to highlight the importance of the steady-state reference design in achieving a major disturbance rejection against errors in the SoC estimates.

4.4.1 Unconstrained Solution for the Battery Currents

The unconstrained solution of a standard QP problem can be obtained directly by performing the partial derivative $\frac{\partial J(k)}{\partial \boldsymbol{u}(k)} = 0$, leading to:

$$\boldsymbol{u}^{\text{unc}}(k) = -(\boldsymbol{W}(k))^{-1}\boldsymbol{F}(k). \tag{4.45}$$

Therefore, the cost functions (4.17) and (4.43), can be evaluated to obtain the inter-arm and inter-SM optimization problem unconstrained solutions, respectively.

Obtaining a reduced analytical expression for the optimal circulating current by replacing (4.18) into (4.45) is challenging, since this current impacts the SoC of each battery in the Δ-CHB-BESS. On the contrary, the unconstrained solution of the inter-SM optimization problem leads to a simpler expression, as the optimal modulating signal of each SM controls its battery current without directly considering the remaining SoC values. Assuming that there is no arm voltage reference given by the current control loop, i.e., $\boldsymbol{v}_x^{dq} = 0$, the following analytical expression is obtained by replacing (4.44) into (4.45):

$$\widetilde{\boldsymbol{\delta}}_{\chi j}^{dq,\text{unc}}(k) = \beta(k)\boldsymbol{i}_{\chi}^{dq}(k), \tag{4.46}$$

with

$$\beta(k) = \frac{2\overline{i}_{\chi j}^{\star}(k)}{I_{\chi}^{2}(k)} - \frac{\rho_{\chi j}(\text{SoC}^{\star}(k+1) - \text{SoC}_{\chi j}(k) + 2\overline{i}_{\chi j}^{\star}(k)\rho_{\chi j})}{\rho_{\chi j}^{2} I_{\chi}^{2}(k) + \lambda_{u}^{\delta}}. \tag{4.47}$$

In addition, replacing (4.46) into (4.6) to obtain the unconstrained battery current

solution yields to:

$$\bar{\imath}_{\chi j}^{\text{unc}}(k) = \frac{\Delta\text{SoC}_{\chi j}(k+1)}{2\rho_{\chi j}} + \frac{\lambda_u^{\delta}\left(2\rho_{\chi j}\bar{\imath}_{\chi j}^{\star}(k) - \Delta\text{SoC}_{\chi j}(k+1)\right)}{2\rho_{\chi j}\left(\rho_{\chi j}^2 I_{\chi}^2(k) + \lambda_u^{\delta}\right)}, \tag{4.48}$$

with $\Delta\text{SoC}_{\chi j}(k+1) = \text{SoC}_{\chi j}(k) - \text{SoC}^{\star}(k+1)$. Note that if $\lambda_u^{\delta} = 0$, the second term of this unconstrained solution for each battery current becomes zero. Conversely, the first term does not depend on any weighing factor, and is equivalent to the corresponding current reference given by the dead-beat solution proposed in [112] for the optimal active power distribution among SMs in single-phase CHB converters. This previous work proved that the dead-beat strategy is robust against significant parametric uncertainties related to the battery voltage measurement, the battery capacity, and the power conversion efficiency. Nevertheless, the dead-beat solution makes the optimal battery current solution sensitive to small errors in the SoC estimates, usually present even in advanced SoC estimation techniques [120]. As a result, selecting $\lambda_u^{\delta} = \lambda_u^{i0} = 0$, in the proposed DS-MPC strategy, can deteriorate the performance of the Δ-CHB-BESS as shown in the analysis presented in the following section.

4.4.2 Control Effort Analysis for the Unconstrained Battery Current Solution

This section analyzes the impact of SoC estimation errors in the analytical expression of the unconstrained battery current solution that balances the SoC at each SM. Firstly, assuming that $\lambda_u^{\delta} = 0$, and replacing (4.34) into (4.48), the unconstrained dead-beat battery current solution can be written as:

$$\bar{\imath}_{\chi j}^{\text{unc}}(k) = \frac{Q_{\chi j}}{T_s}\left(\text{SoC}_{\chi,j}(k) - \frac{\sum_{j=1}^{n}\alpha_{\chi j}(k)\text{SoC}_{\chi j}(k)}{\alpha_{\text{arm}}(k)}\right) + \frac{Q_{\chi j}P_{\chi}^{\star}(k)}{\alpha_{\text{arm}}(k)}. \tag{4.49}$$

The following expression is introduced to account for the SoC estimate uncertainty:

$$\widehat{\text{SoC}}_{\chi j}(k) = \text{SoC}_{\chi j}(k) + \widetilde{\text{SoC}}_{\chi j}(k), \tag{4.50}$$

where $\widehat{\text{SoC}}_{\chi j}(k)$ represents the SoC estimate, $\text{SoC}_{\chi j}(k)$ is the true SoC value, which in practice cannot be measured, and $\widetilde{\text{SoC}}_{\chi j}(k)$ accounts for the estimation error. In this

way, the estimated unconstrained battery current solution, $\widehat{\bar{\imath}}^{\text{unc}}_{\chi j}(k)$ can be obtained by replacing (4.50) into (4.49). Moreover, the current error between the ideal current reference, which only considers the true SoC value, and the estimated battery current solution, i.e, $\Delta\bar{\imath}^{\text{unc}}_{\chi j}(k) = \bar{\imath}^{\text{unc}}_{\chi j}(k) - \widehat{\bar{\imath}}^{\text{unc}}_{\chi j}(k)$, is given by:

$$\Delta\bar{\imath}^{\text{unc}}_{\chi j}(k)=\frac{Q_{\chi j}}{T_s}\left(\frac{\sum_{j=1}^{n}\alpha_{\chi j}(k)\widetilde{\text{SoC}}_{\chi j}(k)}{\alpha_{\text{arm}}(k)} - \widetilde{\text{SoC}}_{\chi j}(k)\right). \tag{4.51}$$

Considering that the SoC estimation error can be maintained below 2% [120], and that $Q_{\chi j} >> 3600\,\text{As}$, the following approximation can be made:

$$\frac{\sum_{j=1}^{n}\alpha_{\chi j}(k)\widetilde{\text{SoC}}_{\chi j}(k)}{\alpha_{\text{arm}}(k)} \approx 0. \tag{4.52}$$

Therefore,

$$\Delta\bar{\imath}^{\text{unc}}_{\chi j}(k) \approx -\frac{Q_{\chi j}}{T_s}\widetilde{\text{SoC}}_{\chi j}(k). \tag{4.53}$$

Given the large battery capacity values and the fact that the sampling period is usually set to fractions of a second, it becomes evident from (4.53) that minor inaccuracies in the SoC estimation can induce significant errors in the unconstrained current reference if the dead-beat solution is considered. However, this issue can be avoided by increasing the value of the weighing factor λ_u^{δ}.

A numerical example is carried out to show the impact of λ_u^{δ} at the unconstrained battery current solution. This analysis is obtained by evaluating (4.45) and obtaining the corresponding unconstrained battery current for one SM, while introducing disturbances at the battery capacity value and SoC estimate. In this analysis, a Δ-CHB-BESS with nine cells of similar characteristics of the experimental setup (see Table 4.2 and 4.3) was assumed to be operating in steady-state with a power reference of 1.2 kW. Besides, the true SoC of each battery was balanced and equal to 0.5.

The unconstrained current solution is assessed for the SM_{11} across a spectrum of perturbed values for the battery capacity and SoC estimate. The parameter Q_{11} is modified from its true value within the range of $\pm 50\%$ of its nominal capacity. In contrast, slight variations within $\pm 0.1\%$ were considered in the SoC estimation error, as small disturbances

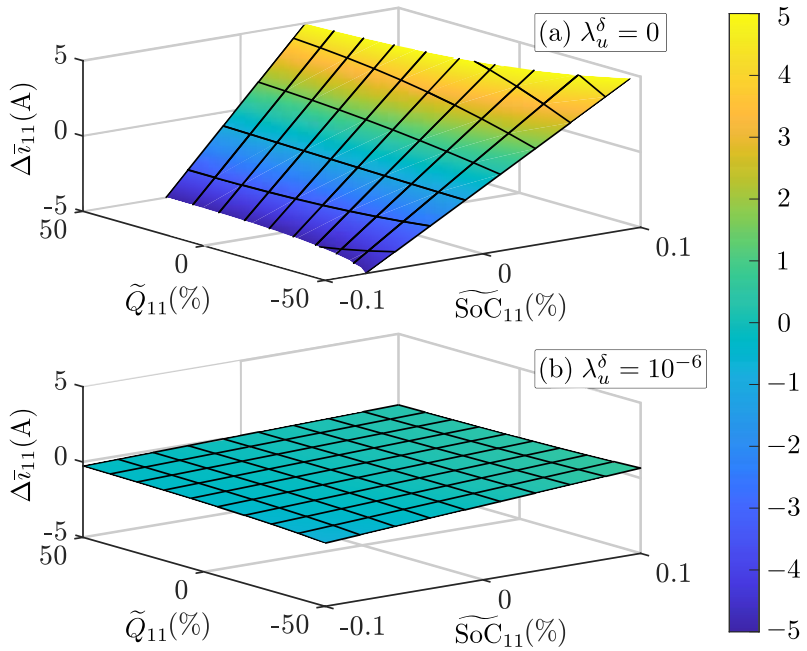


Figure 4.3: Numerical example of the current error at the unconstrained battery current solution due to disturbances in the capacity values and SoC estimates. (a) dead-beat solution, (b) proposed DS-MPC strategy inter-SM solution.

in this value lead to large current errors.

Figure 4.3(a) shows the impact of the capacity and SoC disturbances at the battery current error for the unconstrained dead-beat solution. The unconstrained battery current solution is remarkably more sensitive to SoC errors than large battery capacity errors. Indeed, an SoC estimation error of 0.08% leads to an error of $-5\,\text{A}$, which surpasses the maximum recommended charging current by the cell manufacturer of the Lithium-ion cells used in the experimental setup.

On the other hand, Fig. 4.3(b) shows the impact of the same variations in capacity and SoC estimation error for the unconstrained current solution with the weighing factor set at $\lambda_u^\delta = 10^{-6}$. In this case, the largest current error reaches only $-0.8\,\text{A}$, when the capacity estimate equals the 50% of the true capacity and the SoC estimation error is -0.1%. Therefore, this reduced impact in the estimated battery current solution due to the steady-state control input reference tracking improves the disturbance rejection of the proposed DS-MPC strategy under SoC estimation errors given at the battery pack BMS.

4.5 Simulation Results and Benchmarking

4.5.1 Impact of Weighting Factors and Steady-state Performance

A simulation of the proposed DS-MPC strategy was conducted to verify the impact of the cost function weighting factors on the optimal current solutions. Likewise the previous section, most of the converter and controller parameters for the simulation were equivalent to the ones of the experimental setup, shown in Table 4.2, except for f_{MPC}=20 Hz, $\Delta u_{i0}^{\max}$=2.5, $\Delta\delta^{\max}$=0.3, and the battery capacities, which were scaled down as shown in Table 4.4. These differences between the simulation study and the experimental verification were introduced to achieve the SoC balance in a few simulated seconds instead of requiring several minutes. Moreover, white noise was added to each true SoC value, forcing random SoC estimation errors within a range of ±0.1% for each battery. Finally, significant errors in the capacity estimates, with deviations reaching up to 20% of the true capacity values, were also considered to test the steady-state performance of the proposed DS-MPC strategy. Table 4.4 shows the estimated capacities with added error.

The simulation results are shown in Fig. 4.4. The true battery capacity values were given to the proposed DS-MPC scheme during the first 15 s. As a result, the proposed DS-MPC strategy exhibited a rapid SoC balance for each battery in the Δ-CHB converter without steady-state error. Between 15 s and 30 s, the inaccurate capacity estimates $\hat{Q}_{\chi j}$ were given to the proposed DS-MPC strategy, introducing significant disturbances in the capacity values. These errors were propagated in the calculation of the steady-state circulating current and modulating signal references. Thus, the steady-state current references for each battery were affected, as shown in Fig. 4.4(c), 4.4(f), and 4.4(i). Despite the significant parametric disturbances, only a small steady-state error appears at each SoC, as shown in Fig. 4.4(b), 4.4(e), and 4.4(h).

After 30 s, the weighing factors $\lambda_u^{i0}, \lambda_u^{\delta}$ were set equal to zero. Thus, both MPC stages of the proposed DS-MPC strategy became constrained dead-beat controllers. In this sense, the battery current solutions obtained by the inter-SM optimization stage were similar to the MPC strategy [112]. As depicted in Fig. 4.4(c), 4.4(f), and 4.4(i), the DS-MPC optimal solutions became too aggressive after changing the weighing factors, as the small SoC estimation errors introduced by the white noise, led to large oscillations in the battery currents. Besides, note that the battery current steady-state references also oscillated after

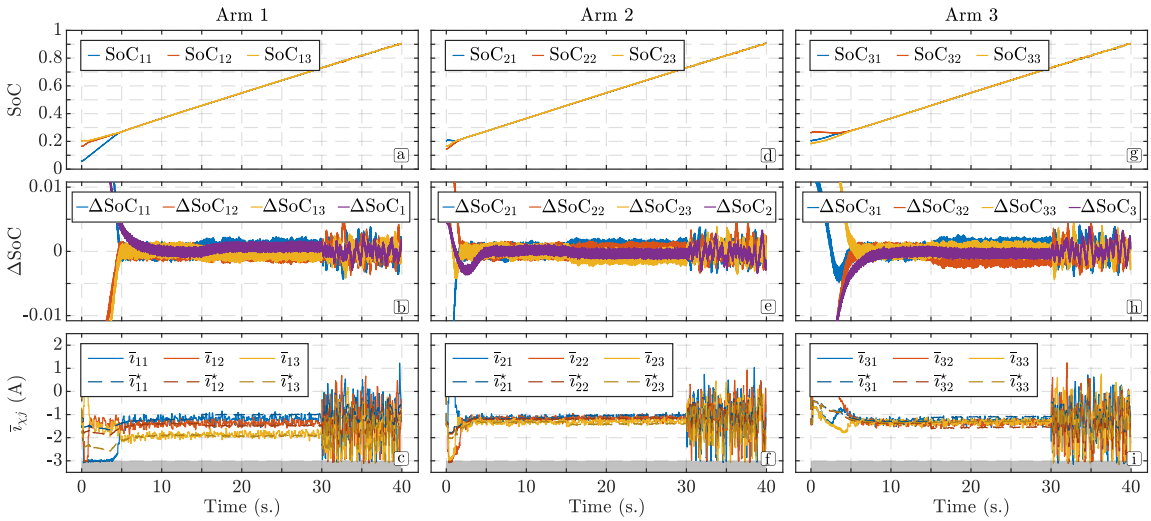


Figure 4.4: Simulation results for the proposed DS-MPC strategy. Each column shows the signals related to a different Δ-CHB converter arm. The first row shows the battery SoCs. The second row shows the SoC error for each SM, $\Delta\text{SoC}_{\chi j}$, and the arm SoC error, ΔSoC_{χ}. The third row shows the battery currents and their steady-state references for a minimum allowed current of -3 A. Disturbances in the capacity values are introduced after 15 s, and $\lambda_u^{\delta}, \lambda_u^{i0}$ are set to zero after 30 s.

30 s. These reiterative changes at the steady-state battery current references were given due to large changes in the Δ-CHB circulating current, caused by SoC estimation noise propagated through the inter-arm optimization.

Although the simulation showed that the constrained dead-beat controllers reached zero mean steady-state error over time, the resultant battery current oscillations are undesirable for the Δ-CHB-BESS. In fact, these current oscillations increase the Δ-CHB converter and battery losses, and the significant changes in modulating signals required to modify the battery currents can deteriorate the harmonic performance of PS-PWM strategies [124].

Consequently, the simulation results verify the aforementioned analytical and numeric analysis, confirming that the additional cost function term and control input references design of the proposed DS-MPC technique benefit the control strategy by increasing its disturbance rejection against SoC estimation errors and improving its steady-state performance.

Table 4.2: Δ-CHB converter and controller main parameters for the experimental verification.

Description	Variable	Value
Number of H-Bridge cells	n	9
Arm inductance	L	10 mH
Nominal battery pack voltage	V_{DC}	80.4 V
Average battery pack capacity	Q_{avg}	3.98 Ah
Safe battery current rating	$\left[i_{\chi j}^{\min}, i_{\chi j}^{\max}\right]$	[-3, 3] A
Safe arm current rating	$\left[i_{\chi}^{\min}, i_{\chi}^{\max}\right]$	[-8, 8] A
Grid voltage (LL-RMS)	V_g	122.47 V
Fundamental frequency	f_0	50 Hz
Nominal converter power	S_{nom}	1.2 kVA
PS-PWM carrier frequency	f_c	2 KHz
Current controller sampling frequency	f_s	4 kHz
DS-MPC sampling frequency	f_{MPC}	2 Hz
Weighing factors inter-arm stage	λ_u^{i0}	10^{-7}
Weighing factors inter-SM stage	λ_u^{δ}	10^{-6}
Rate of change constraints	$\Delta u_{i0}^{\max}$, $\Delta\delta^{\max}$	0.1, 0.05
Maximum allowed modulation index	$m_a^{\max}$	0.9

Table 4.3: Experimental setup SLB pack capacities in Ah.

χj	11	12	13	21	22	23	31	32	33
$Q_{\chi j}$	3.56	4.1	5.53	3.37	3.5	3.84	3.86	4.1	4.0

Table 4.4: Simulated battery capacities in mAh. $Q_{\chi j}$ refers to the true simulated capacities, and $\hat{Q}_{\chi j}$ refers to the estimated capacities with added disturbance used by the DS-MPC.

χj	11	12	13	21	22	23	31	32	33
$Q_{\chi j}$	17.8	20	27.6	16.8	17.3	19	19.3	20.5	20
$\hat{Q}_{\chi j}$	15.1	22	29	16	18.2	22	17.3	24.6	21

4.5.2 Comparison With Different SoC Balancing Methods

In this subsection, simulations are carried out to compare the performance of the proposed DS-MPC strategy against the PI-based method [76], the sorting-based method [125],

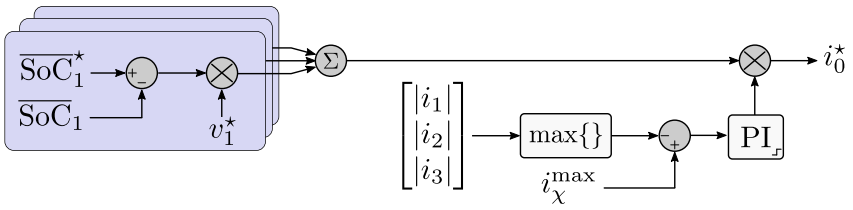


Figure 4.5: Circulating current reference generation scheme applied to the benchmark inter-SM methods analyzed in the simulation results.

and the MPC strategy [112]. The latter two approaches only address the inter-SM SoC balancing problem, whereas the inter-arm SoC balance strategy in [76] does not consider the maximum current rating of the arm. Therefore, the circulating current reference generation stage, depicted in Fig. 4.5, was considered for these methods in this analysis.

Figure 4.6(a) and 4.6(b) show the performance of the PI- and sorting-based methods, respectively. These methods are unable to limit the maximum battery current, resulting in overcurrents when large SoC errors are presented. Additionally, note from Fig. 4.6(a) that the PI-based method showed the largest steady-state error despite the initial high SLB currents. This result highlights the trade-off between overcurrents and steady-state error for the PI-based method, which poses a challenge in the controller gain selection for SL-BESS applications.

The performance of the MPC strategy [3] is shown in Fig. 4.6(c). Although this method considers the battery power limits in its formulation, it also fails to constrain the maximum SLB currents. This issue arises since this MPC strategy does not address the inter-arm energy balancing problem. Consequently, the circulating current injection provided by the external inter-arm SoC balance control (see Fig. 4.5), makes the inter-SM optimization problem unfeasible for arm-1 during the initial seconds. Moreover, note that this problem occurs despite the arm currents not exceeding their maximum allowed threshold of 10 A.

Finally, Fig. 4.6(d) shows the performance of the proposed DS-MPC strategy. The proposed SoC balancing scheme ensures that the SL-BESS operates within its safe range. This result is achieved by the proposed DS-MPC by considering the SLB current constraints in both inter-SM and inter-arm optimization stages. As a result, a lower circulating current reference is given to the current controller to avoid battery overcurrents.

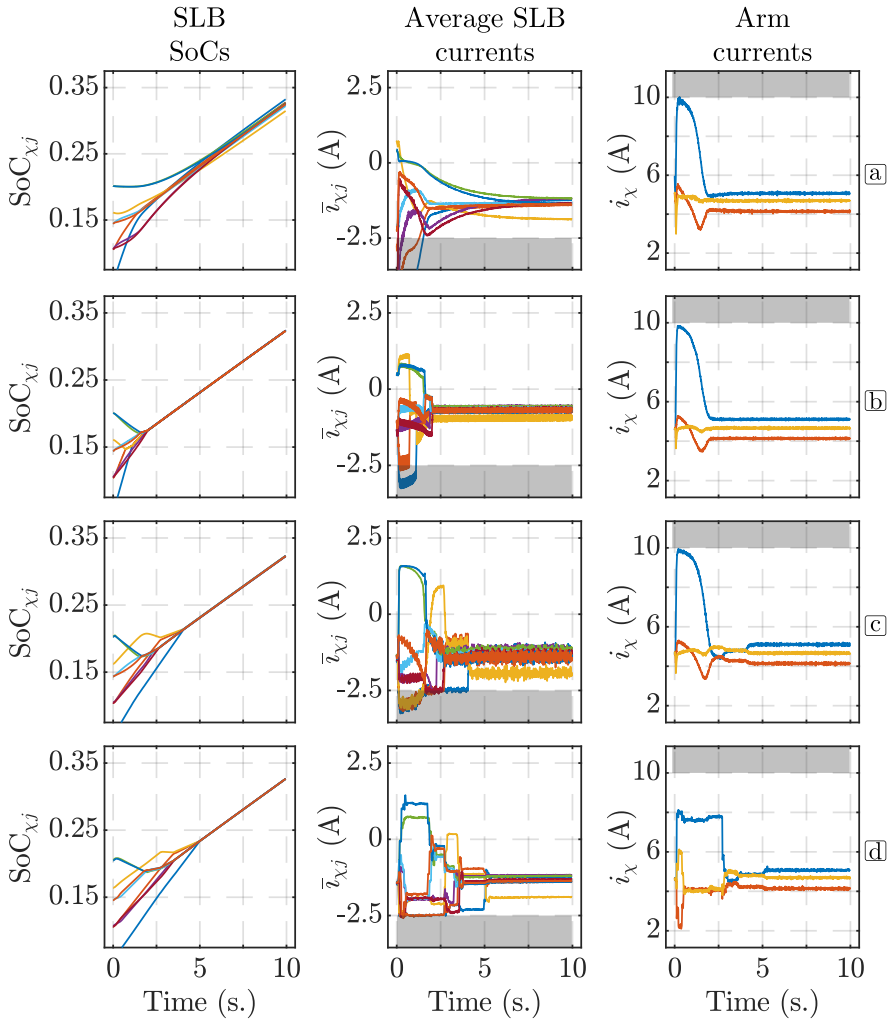


Figure 4.6: Simulation results for different SoC balancing methods. (a) PI-based method [76], (b) sorting-based method [125], (c) MPC strategy [112], and (d) proposed DS-MPC strategy. The shadowed areas represent the imposed safety constraint thresholds.

4.6 Experimental Verification

4.6.1 Experimental Setup

Discarded electric bike (e-bike) batteries were collected and dismantled to retrieve their 18650 Lithium-ion cells for their second-life application. The cells of each e-bike battery that exhibited a voltage within the recommended operation range between [2.75, 4.2] V were tested and sorted to assemble new SLB packs of 24S2P and 24S3P cell configurations. The capacity of each battery pack was then tested by doing a complete charge and discharge

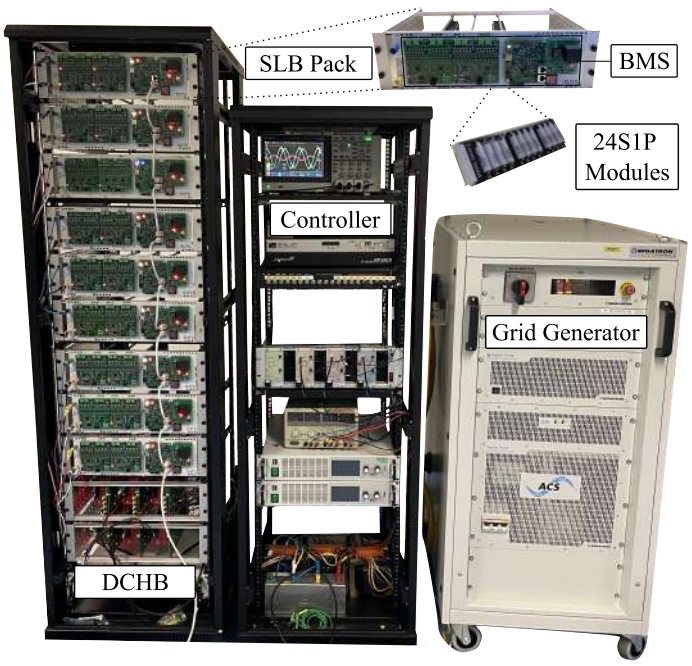


Figure 4.7: Δ-CHB-BESS experimental prototype with 9 SMs and SLBs.

cycle. A cut-off voltage threshold of 2.75 V for the weakest cell at each pack was set as the terminating condition for the SLB pack capacity tests. The obtained capacities of each pack are shown in Table 4.3, and the experimental setup is shown in Fig. 4.7.

The converter current control and the proposed DS-MPC strategy were implemented on an OPAL-RT OP4510 control platform based on an Intel Xeon E3 v5 CPU and two Kintex-7 field programmable gate arrays (FPGAs). Moreover, a multi-core configuration was employed to separate the execution rate and the computational burden of the Δ-CHB converter current control, and the proposed DS-MPC strategy. Accordingly, the current controller and the required single-phase synchronous *dq*-frame transformations were implemented with a sampling frequency of 4 kHz, whereas the proposed DS-MPC sampling frequency was set at 2 Hz, taking advantage of the slow battery SoC dynamics. The main parameters of the experimental setup and controller are shown in Table 4.2.

In addition, the proposed OVA-PS-PWM and KF harmonic compensator strategies, and the modulation sampling technique [72], were implemented to obtain the switching signals of each SM using the same core of the current controller.

Given the reduced sampling rate of the proposed DS-MPC strategy, the QP solver had plenty of time to find the optimal solutions, facilitating its implementation. Indeed, the

execution time of the interior point solver [123] implemented in the experimental setup to find the optimal solution of the proposed DS-MPC strategy only used 0.1% of the available time between samples. Therefore, only a reduced fraction of the second core computational capacity was used.

4.6.2 Weighting Factor Selection

When the SoCs become close to their reference for the inter-arm and the inter-SM optimizations, the first term in the cost functions (4.12) and (4.31) is almost zero. As a consequence, the second term, related to the control input steady-state reference tracking, becomes predominant, which means that the circulating current and SM modulating signals become close to $\boldsymbol{i}^{\star}_{0,ss}(k)$, and $\widetilde{\boldsymbol{\delta}}^{\star}_{\chi}(k)$, respectively.

In this sense, the cost function weighing factors λ_u^{i0} and λ_u^{δ} allows to adjust the closed-loop performance of the proposed SoC balancing strategy by determining the relative importance of the control input tracking errors against the state tracking errors. As the proposed optimization constraints ensure the Δ-CHB-BESS operates within its safe range, small weighing factor values are recommended to provide a fast SoC balance. However, as proved in Section 4.5.1, setting these weighing factors equal to zero makes the proposed DS-MPC sensitive to minor errors in the SoC estimation.

Accordingly, the selection of λ_u^{i0} and λ_u^{δ} can be carried out by a heuristic process, starting from small values, e.g., $\lambda_u^{i0} = \lambda_u^{\delta} = 10^{-8}$, and increasing these values depending on the amount of noise that propagates to the steady-state battery current references from the BMS SoC estimates, when each SoC is close to its reference value. The weighing factor values used in the experimental setup are shown in Table 4.2.

4.6.3 Control Input Rate of Change Constraints Design

The parameters $\Delta u_{i0}^{\max}$ and $\Delta \delta^{\max}$ define the maximum rate of change for the circulating current reference and the SM modulating signals in the optimization constraints. Thus, these parameters determine how fast the Δ-CHB converter can change its operating point to balance the SLB SoCs. In this way, assuming that the Δ-CHB converter is operating at its nominal power with no active constraints, the time periods required by the inter-arm and inter-SM optimization stages to modify the Δ-CHB converter operating point until

reaching the arm current and modulation index thresholds are given by:

$$T_{i0}^{\max} = 2T_s \frac{i_{\text{arm}}^{\max} - i_{\text{arm}}^{\text{nom}}}{\Delta u_{i0}^{\max}},$$
$$T_{\delta}^{\max} = 2T_s \frac{m_a^{\max} - m_a^{\text{nom}}}{\Delta \delta^{\max}}, \tag{4.54}$$

with $i_{\text{arm}}^{\text{nom}}$ and m_a^{nom}, the nominal arm current amplitude and modulation index for the Δ-CHB converter, respectively. Consequently, (4.54) can be used to compute $\Delta u_{i0}^{\max}$ and $\Delta \delta^{\max}$ after defining the desired response times $T_{i0}^{\max}$ and $T_{\delta}^{\max}$ for each optimization stage. The values for $\Delta u_{i0}^{\max}$ and $\Delta \delta^{\max}$ used in this work are shown in Table 4.2. A faster response for the inter-SM optimization stage was established by setting $T_{\delta}^{\max} \approx 5\,\text{s}$, and $T_{i0}^{\max} \approx 35\,\text{s}$. As a result, the DS-MPC strategy provides smooth circulating current reference changes and more aggressive changes in the SM modulating signals regarding their feasible range of values.

4.6.4 Experimental Results

An experimental test of one hour long was carried out to verify the effectiveness of the proposed DS-MPC SoC balancing strategy for Δ-CHB-BESS. Before this experiment, the SLBs were discharged at different rates, forcing large SoC imbalances for the inter-SM and inter-arm optimizations as the initial conditions of the experimental test.

During the experiment, an initial constant power reference of $-1.2\,\text{kW}$ was set for the Δ-CHB converter in order to charge the SLBs. After the average SoC among the SMs reached 0.7, the three-phase power flow was reversed until the first hour of operation was finished. The results for the complete experimental test are shown in Fig. 4.8.

The interaction between the proposed inter-SM and the inter-arm optimization stages can be observed when large SoC errors are present during the first minutes of the experiment. For instance, let us focus on arm-1. Figure 4.8(e), shows a fast initial change in the modulation indexes, $|\delta_{\chi j}|$. In fact, $|\delta_{11}|$ and $|\delta_{12}|$ reach their maximum allowed value in only a few seconds. This change in modulating signals led the battery currents $\bar{\imath}_{11}$ and $\bar{\imath}_{12}$ to also quickly reach their minimum current threshold at $-3\,\text{A}$, as depicted in Fig. 4.8(c). Conversely, Fig. 4.8(d) shows that the arm current presented a more gradual increase than the modulation indexes, as expected due to the selected values for $\Delta u_{i0}^{\max}$ and $\Delta \delta^{\max}$. Moreover, note that while the arm current was slowly increased, the modulating signals

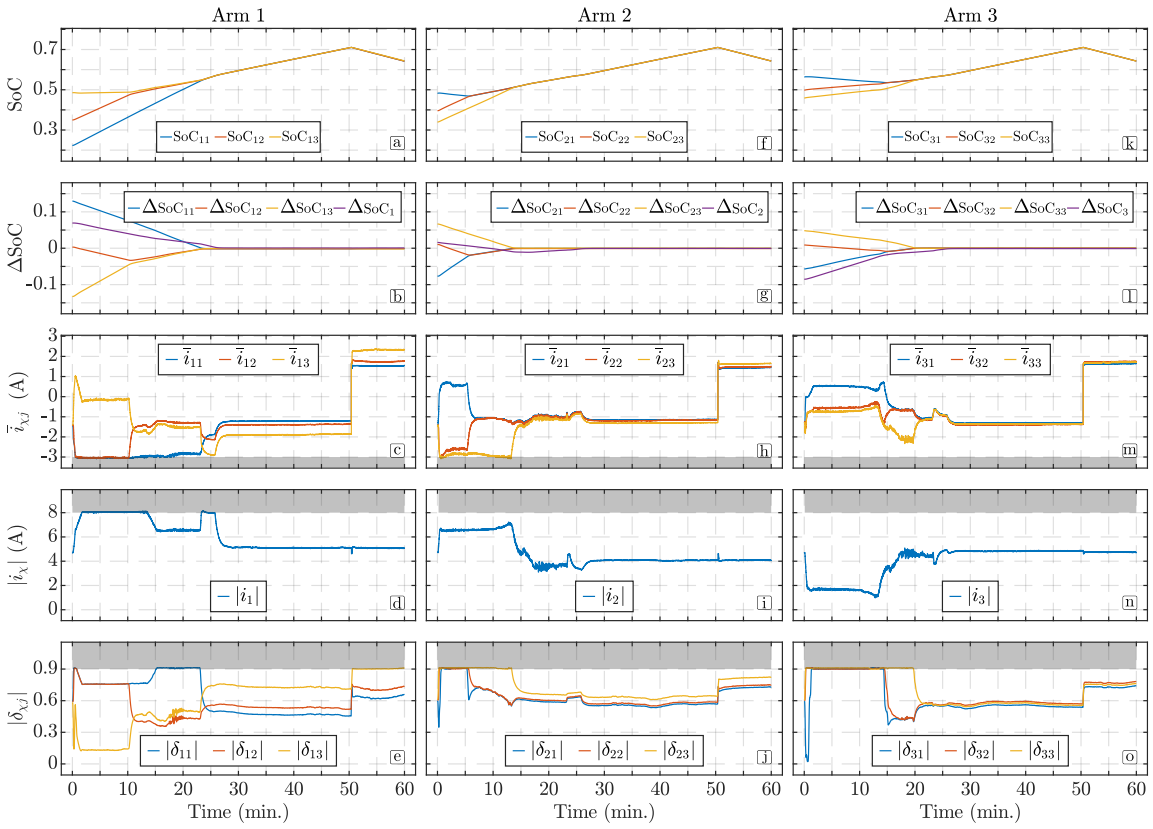


Figure 4.8: Experimental results for the proposed DS-MPC strategy. Each column shows the signals related to a different Δ-CHB converter arm. The first row shows the SLB estimated SoCs, the second row shows the SoC errors for each SLB, and the average SoC error of the arm, the third row shows the SLB currents, the fourth row shows the amplitude of each arm current, and the fifth row shows the amplitude of each modulating signal. The shadowed areas represent the DS-MPC constraint thresholds.

were incrementally adjusted, avoiding battery overcurrents. Around $t = 2\,\mathrm{min.}$, the proposed DS-MPC strategy started providing constant SM modulating signals and circulating current reference solutions for this arm until approximately $t = 10\,\mathrm{min}$.

It is important to highlight that during this period, in which the optimal solutions remained constant, the proposed DS-MPC strategy prioritized the rapid SoC balance over the steady-state reference tracking. This behavior was caused by the large SoC tracking errors, which were predominant in the optimization cost functions. As a result, active constraints were obtained for the maximum current amplitude at arm-1 and for the maximum charging currents for SM_{11} and SM_{12}. Therefore, when the proposed DS-MPC strategy is operating with significant SoC errors, the optimal solutions of each optimization stage

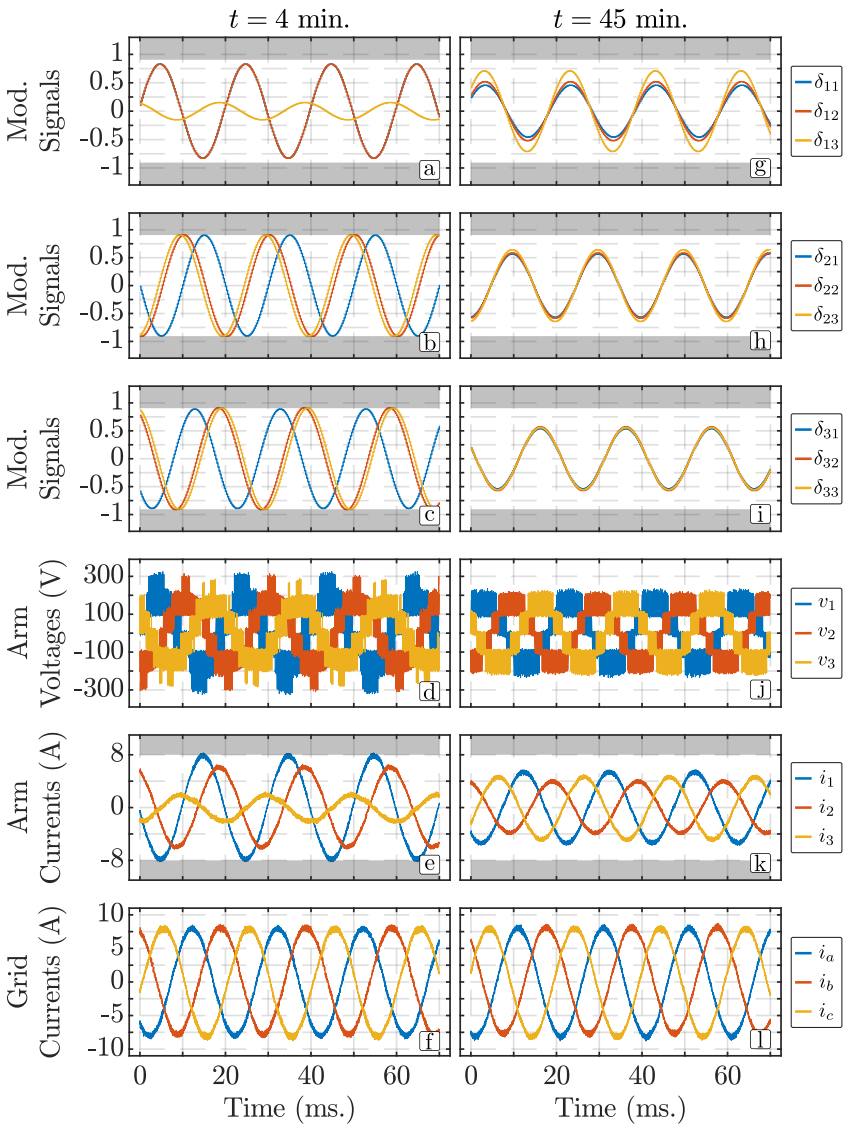


Figure 4.9: Experimental results for the Δ-CHB waveforms at the beginning and end of the experimental test. The left column shows the converter signals at the beginning of the balancing test. The right column shows the signals close to the end of the test after the SoC balance was achieved.

modify the Δ-CHB converter operating point until reaching the optimal battery currents that reduce the SoC error at the fastest feasible rate, given the Δ-CHB-BESS safe operation constraints.

Figure 4.9(a)-(f) shows the instantaneous modulating signals sent to the OVA-PS-PWM stage, and oscilloscope measurements for the Δ-CHB arm voltages and currents, recorded

at $t = 4\,\text{min}$. From Fig. 4.9(a)-(f), it can be confirmed that the SM modulating signals and arm currents do not surpass their maximum allowed limits and that the active constraints do not distort the grid currents. Furthermore, note that the modulating signals of the SMs of the same arm exhibit different phase lags regarding their respective arm current. In this sense, the proposed inter-SM optimization not only inherently assigns the active power distribution among SMs, but also assigns their reactive powers by controlling the modulating signals in the synchronous dq-frame.

After 25 minutes, the SoC balance was achieved for each SLB. At this time of the test, the steady-state current of arm-1 also exhibited the highest amplitude, as shown in Figs. 4.8(d), 4.8(j), and 4.8(n). This higher arm current was caused by the fact that arm-1 had the SLBs with the largest capacities. Accordingly, the Δ-CHB circulating current reference given by the inter-arm optimization stage achieved the required inter-arm power imbalance to maintain the average arm SoC balanced within the Δ-CHB-BESS arms. Besides, arm-1 was comprised of SLBs with substantial capacity disparities, compared with the other arms (see Table 4.3). Consequently, even after the SoC balance was reached, the battery currents at this arm and its SM modulating indexes presented significant differences as depicted in Fig. 4.8(c), and Fig. 4.8(e), respectively.

The Δ-CHB converter instantaneous operation was also captured at $t = 45\,\text{min}$. These results are shown in Fig. 4.9(g)-(l). Here, it can be seen that all the inequality constraints related to the Δ-CHB-BESS safe operation were no longer active. Furthermore, Fig. 4.9(g)-(i) shows that all the modulating signals belonging to the same arm became aligned as a result of the proposed steady-state reference design, which enforced $i_{\chi j}^{q,\star} = 0$ at its derivation. Therefore, once the SoC tracking errors are reduced, the steady-state control input reference tracking becomes predominant at the optimization cost functions, leading the DS-MPC strategy optimal solutions to converge to the corresponding steady-state SLB current references, avoiding undesired current oscillations.

4.7 Conclusions

In this chapter, a DS-MPC strategy to balance the SoC of SLBs in a Δ-CHB-BESS has been proposed. To describe the SoC dynamics of the SLBs accounting for the inter-arm and inter-SM power couplings, a novel discrete-time model based on the single-phase

synchronous dq-frame representation of the Δ-CHB converter currents and SM modulating signals is derived. This model is used to formulate two constrained optimal control problems, whose solutions led to optimal battery currents that balance the SoC among the SLB packs.

Simulation tests were carried out to assess the relevance of the steady-state control input reference design proposed for each optimization stage. The results showed that using a dead-beat solution similar to [112] can lead to battery current oscillations if reduced errors are introduced in the SoC estimates. However, this issue can be mitigated by increasing the weighing factors λ_u^{δ}, and λ_u^{i0} at each cost function of the DS-MPC scheme.

Experimental results verified the effectiveness of the proposed DS-MPC strategy in a Δ-CHB-BESS prototype composed of second-life e-bike Lithium-ion cells. The proposed DS-MPC strategy gradually changes the operating point of the Δ-CHB converter, reaching optimal battery currents at each SM that favor the rapid SoC balance among the SLBs. Moreover, the proposed DS-MPC technique achieves the SoC balance without violating the SLB maximum current ratings or the operational constraints of the Δ-CHB converter at any time.

Consequently, the proposed DS-MPC strategy is a promising control alternative to govern Δ-CHB-BESS with SLBs, offering fast SoC balancing and flexibility to impose the required current constraints at each battery SM, ensuring the safe operation of the overall SL-BESS. Moreover, the proposed DS-MPC strategy can be directly integrated with the OVA-PS-PWM technique and the KF harmonic compensator introduced in previous chapters, achieving a reduced voltage harmonic distortion and mitigating the Δ-CHB currents steady-state errors despite the unbalanced power distribution among SMs.

Chapter 5

Conclusions

5.1 Conclusions

The Δ-CHB converter is considered a promising technology for next-generation BESS inverters, offering its well-known advantages, such as modularity, excellent harmonic performance, and the ability to provide unbalanced power distributions among its SMs. These advantages can be exploited to regulate the output power of the converter while maintaining the SoC balanced among SLB packs connected to the converter SMs. However, achieving an effective SoC balance that maintains the CHB-SL-BESS operation within its safe operation range poses several challenges to the converter control system. Consequently, some of these control challenges regarding the integration of SLBs to the CHB converter have been addressed in this thesis.

In chapter 2, a predictive OVA-PS-PWM strategy suited for CHB-SL-BESS has been proposed. A novel discrete-time dynamic model was derived to obtain CHB output voltage harmonic distortion predictions. This model was used to formulate an optimal control problem, which can be solved analytically. As a result, an optimal PS-angle update rule that minimizes the output voltage WTHD was derived.

Simulation results assessed the performance of the proposed OVA-PS-PWM against the VA-PS-PWM [83]. The results showed that the proposed optimal modulation scheme outperforms the VA-PS-PWM by minimizing the CHB converter output voltage WTHD at every sampling instant for the complete operational range of the converter; thus, including the operating conditions in which prior VA-PS-PWM strategies provide undetermined

PS-angle solutions. Moreover, experimental results also confirmed the effectiveness of the proposed OVA-PS-PWM under unbalanced operation conditions, including different SM dc-voltages and uneven power references for each SM for a nine-cell single-phase CHB converter. The proposed OVA-PS-PWM strategy significantly reduces the undesired switching harmonic components compared with the conventional PS-PWM. Therefore, the proposed optimal modulation strategy can extend the excellent harmonic performance of PS-PWM for unbalanced operation conditions, which makes it a promising modulation alternative for CHB-SL-BESS.

In chapter 3, a KF-based strategy for steady-state error compensation in optimal control strategies for Δ-CHB converters has been proposed. The proposed KF strategy is based on an augmented affine state space model, which includes voltage disturbances that impact the arm currents dynamics. These disturbance states represent the equivalent voltage drops at the converter arms caused by modeling errors or by not measuring the SM capacitor voltages and assuming a constant dc voltage at each SM. Accordingly, the proposed KF observer estimates these voltage disturbances, allowing the calculation of a corrected steady-state control input reference and improving the arm current predictions.

Experimental results for a CHB-SL-BESS prototype composed of second-life e-bike Lithium-ion cells have verified that the proposed KF strategy eliminates the converter's current steady-state errors while showing a satisfactory transient response without introducing current overshoots. Furthermore, the proposed KF observer can be easily added to existing optimal current control schemes for the CHB converter, improving the closed-loop disturbance rejection and the steady-state performance under parameter uncertainty scenarios. Furthermore, the proposed KF strategy can reduce the converter hardware complexity and measurement requirements for CHB-SL-BESS, by not requiring SM capacitor voltage measurements or fast communications with the BMS when implemented with an LQR or FCS-MPC strategy.

Finally, in chapter 4, a constrained DS-MPC strategy to balance the SoC of SLBs in a Δ-CHB-BESS while meeting safety constraints has been proposed. A novel SoC discrete-time dynamic model is derived to account for the inter-arm and inter-SM power couplings in the Δ-CHB converter. This model is used to formulate two constrained optimal control problems, whose solutions led to optimal battery currents that balance the SoC among the SLB packs.

Experimental results verified the efficacy of the proposed DS-MPC strategy in a CHB-SL-BESS prototype. Moreover, these experiments validated the integration of the OVA-PS-PWM, the KF strategy, and the DS-MPC in the CHB-SL-BESS prototype. The results showed that the proposed DS-MPC strategy incrementally modifies the operating point of the Δ-CHB converter, reaching optimal battery currents at each SM that favor the rapid SoC balance among the SLBs. In this way, the proposed DS-MPC technique achieves the SoC balance without violating the SLB maximum current ratings or the operational constraints of the Δ-CHB converter at any time.

In conclusion, the hypothesis under question for this research project was proven true by implementing the proposed control system in the SL-BESS prototype. Experimental verification demonstrated that the combination of the proposed MPC strategies can achieve optimal SoC balancing in a CHB-SL-BESS, without deteriorating the output power quality of the converter and maintaining the BESS in its safe range of operation at all times. In this way, the control strategies proposed in this thesis offer a suitable control solution to govern CHB-BESS with SLBs, providing fast SoC balancing and flexibility to impose the required current constraints at each battery SM, ensuring the safe operation of the SL-BESS.

5.2 Recommendations for Further Research

Providing SL-BESS control system solutions is a complex task. Therefore, there are still several challenges and opportunities related to this research topic, which go beyond the scope of this work. Accordingly, the following interesting topics are proposed to further advance the field of CHB-SL-BESS based on the results obtained in this research project and the experience gained working with SLBs:

- **Temperature control of SLBs:** battery packs assembled with second-life cells usually exhibit differences in internal resistance. As a consequence, batteries with larger resistance tend to operate at higher temperatures if no independent cooling system is implemented for each BP. Although the proposed DS-MPC strategy includes current constraints to prevent the batteries from reaching unsafe operating conditions, charging and discharging the batteries at their maximum allowed rate to balance the SoC might not be optimal to promote the longevity of the SL-BESS.

In this way, new optimization cost functions can be formulated, or electro-thermal battery models can be considered to develop MPC strategies that not only achieve the SoC balance but also allow the designer to make trade-offs between increasing the SoC balancing speed and maintaining the temperature of each BP within limits that promote the extension of the SL-BESS operational lifespan.

- **SoH control of SLBs:** similar to the previous research topic, focusing only on balancing the SoC to exploit the total available energy in the SL-BESS may cause an accelerated end of life of some batteries. For instance, in a SL-BESS that combines BPs of different manufacturers or BPs from different EV models, the BP with the largest capacity could be the one with the lowest remaining useful life. Consequently, the DS-MPC strategy will charge and discharge this pack at the highest current rate, leading to the potential accelerated degradation of this BP. In this way, including the SoH balancing as a primary control target could be preferred over maximizing the available energy utilization if the operational costs of replacing the SLBs at the end of their life surpass the economic benefits of fully exploiting the available energy of each BP within the SL-BESS.

- **Extended horizon MPC schemes with forecasted data:** depending on the application, a day ahead pre-dispatch for the SL-BESS can be available. This additional information for the SL-BESS grid power references can be exploited to further optimize the operation of the SL-BESS, achieving secondary control objectives like the ones mentioned above. Accordingly, extended horizon MPC schemes can be investigated under these operating scenarios as a future research topic.

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