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Review

Traditional and Hybrid Topologies for Single-/Three-Phase Transformerless Multilevel Inverters

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Abstract: With increasing interest in integrating solar power into the utility grid, multilevel inverters are gaining much more attention for medium- and high-power applications due to their high-quality waveform, low voltage stress across active components, and low total harmonic distortion in output voltage. However, to achieve these benefits, a large number of active and passive components are required. A transformer is also required to provide galvanic isolation, which increases its size and weight and reduces its power density and efficiency. In order to overcome the disadvantages posed by transformer-based inverters, research is being conducted on the transformerless topology of multilevel inverters. The first aim of this review article is to summarize traditional transformerless multilevel inverters (TMLIs) considering both single- and three-phase topologies. Secondly, the main aim of this article is to provide a detailed overview of the hybrid topologies of TMLIs that employ fewer components for photovoltaic applications. In addition, this study compares traditional and hybrid single-/three-phase topologies in terms of component count and performance factors, which will be useful to researchers.

Keywords: transformerless; multilevel inverter; single and three phase inverters; reduced component count; photovoltaic (PV) systems

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1. Introduction

Photovoltaic (PV) energy is one of the most reliable, clean, environmentally friendly, and widely available renewable energy sources [1–3]. The focus on PV systems has greatly increased over the years owing to growing concerns regarding climate change and reducing fossil fuel emissions. Moreover, the conversion efficiency of solar panels has also been improved due to technological advancements in PV modules, leading to the generation of more electricity [4–6].

PV systems make use of solar cells for the conversion of solar energy into electrical energy to be employed in residential as well as commercial applications. A considerable reduction in cost of PV systems has been observed due to various factors including cheap raw materials, improvement in manufacturing techniques, better policies and government incentives like tax credits as well as continuous research and innovations in the areas of PV energy storage and integration with the energy grid. While commercial PV system applications have undergone numerous advancements over the years, their efficiency poses a major challenge affecting overall performance. This is due to technological limits regarding conventional silicon solar cells and system-level losses, which include wiring, shading

and temperature effects, as well as the efficiency of inverters. The overall performance of commercial PV systems can be enhanced through the optimization of inverter design and their integration [7,8]. Several types of inverters have been introduced to improve the performance of PV systems [9–12]. While the conventional two-level inverter topology is both simple as well as cost-effective, it has low efficiency, produces high distortion in harmonics, high leakage current, requires a high switching frequency and cannot be employed for high-power applications [13–15].

The advancement of multilevel inverters (MLIs) has helped overcome power quality issues by improving the output waveform with less THD and operating with both fundamental and high-switching-frequency pulse-width modulation (PWM) techniques. The voltage stress across the switches is significantly reduced in these MLIs [16]. For transformerless operation, MLIs are the best choice because they can dramatically reduce cost, weight, and size by avoiding the use of a bulky and heavy transformer. Placing low-frequency transformers after MLIs is a viable technique to ensure isolation in high-power applications and effectively handle the leakage current issue [17,18]. However, transformerless MLIs (TMLIs) are the most suitable choice in terms of efficiency [19]. Thus, academics and scientists are emphasizing more detailed investigations into TMLIs [20].

Figure 1 shows a simplified classification of inverter topologies for PV applications. The major classifications are traditional and hybrid topologies based on their structure and number of phases. Traditional topologies such as cascaded multilevel inverters [21–24], neutral-point-clamped inverters (NPCs) [25,26] and flying capacitor inverters (FCs) [27] have been developed and considered as the foundation of many multilevel converters. The topology of the cascaded multilevel inverter incorporates a modular structure, leading to a stepped AC waveform generation. A more sinusoidal AC waveform is generated, with the increase in output steps thereby reducing the THD. The modular structure also increases the reliability of the inverter under faulty conditions [28]. Single-phase cascaded inverters are suitable for low- and medium-power applications. Three-phase cascaded multilevel inverters have been introduced in the past for high-power applications [29,30].

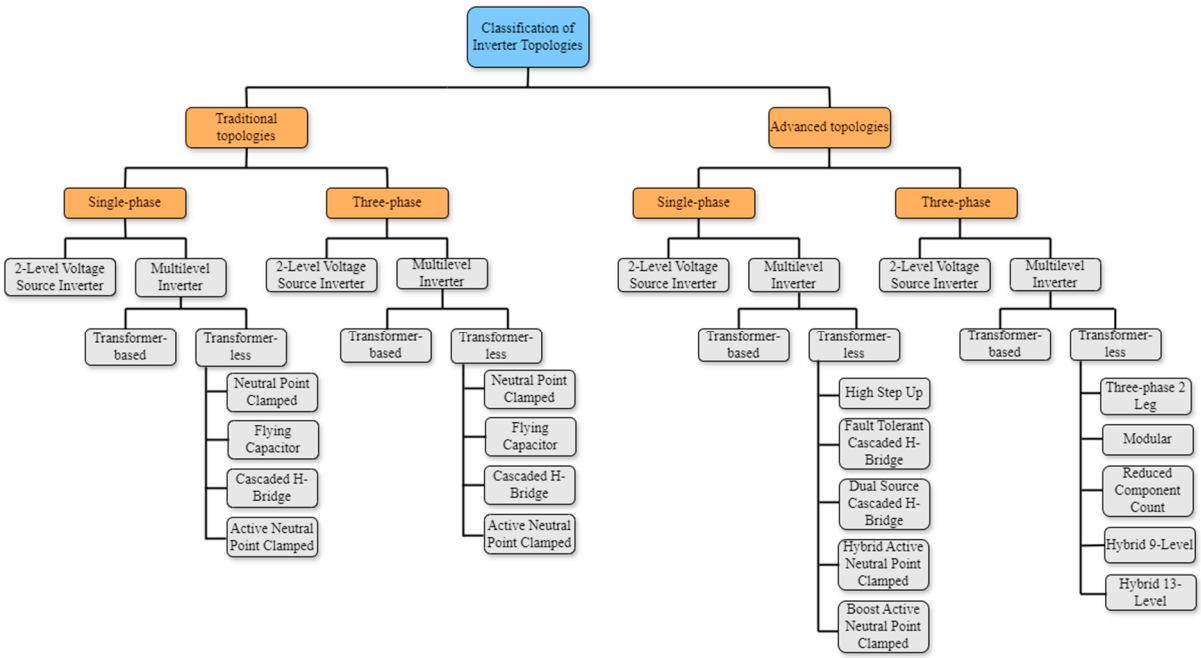

Figure 1. Classification of inverter topologies both for single- and three-phase inverter systems.

In TMLIs, the absence of galvanic isolation can cause severe damage to the system owing to the flow of leakage current between the PV and ground [31,32]. To avoid this problem, NPC topologies based on single and three phases have been introduced and are widely used for renewable energy applications [33,34]. However, to achieve higher

voltage levels using NPC topology, a large number of clamping diodes are required, which creates voltage-unbalancing issues in the capacitor and unequal distribution of losses in the active components [35]. These drawbacks can be overcome by using an active-NPC topology [36–40]. A uniform distribution of the voltage stress on the active components can also be achieved using the FC topology [41,42]. The main limitations of using the FC topology are the capacitor voltage imbalance issue and the usage of large capacitors [43,44].

The cascaded multilevel inverter is the most attractive among NPC, ANPC and FC due to its modular architecture and requirement of the fewest components; however, it has the drawback of using separate DC sources for each cell, which increases its cost but, on the other hand, also provides independent control and high reliability [45]. The replacement of DC sources with capacitors has been suggested in previous studies [46]. The main drawbacks of these TMLIs [16–40] are the use of a large number of active and passive components to increase voltage levels and efficiency. An additional active component requires the gate driver's circuits, heat sinks, and circuits for isolation, and makes the controller complex, which increases its cost, size, and complexity [47–49]. Therefore, a prevalent research topic in different sectors and academic institutions is the development of hybrid topologies with fewer components, to address cost, size, and complexity challenges [50]. Hybrid topologies include TMLIs with a smaller number of active and passive components, which increases the reliability of the inverter by decreasing the total cost. This reduction in cost is due to the incorporation of fewer components in the multilevel topologies. A smaller number of components provides a reduction in material costs as well as complexity of the assembly, in turn providing simpler control strategies and easy implementation. The smaller number of components leads to fewer potential failure points, thus leading to improved reliability in the overall system. Several hybrid TMLIs have been proposed in the last few years. Different parameters have been considered to evaluate and improve the performance of inverters, which include reducing DC sources, employing a smaller number of switches with novel structures, incorporating asymmetric and symmetric configurations with a smaller number of components, as well as employing transformerless inverter topology. Research and development have paved the way for new as well as efficient inverter topologies, each having the potential to become the preferred choice for various industrial applications.

This paper gives a detailed overview of traditional and hybrid inverter topologies for PV applications, considering single-phase and three-phase topologies. First, the traditional topologies of TMLIs are presented, which are considered the foundation of multilevel inverters. Improvements in the performance of basic inverters are also well described by changing the structure and arrangement of switches. Next, hybrid topologies using a smaller number of active and passive components for each topology are discussed in detail. This is followed by the comparison of the traditional and hybrid topologies in terms of component count, which will be helpful in many industrial applications.

The remainder of this paper is organized as follows. Section 2 presents the classification of the conventional and hybrid topologies of single-/three-phase TMLIs along with a detailed discussion on the architecture and the employed experimental process of each. Section 3 presents an extensive comparative analysis of the single-/three-phase TMLIs based on their physical as well as performance parameters. Conclusions are presented in Section 4.

2. Classification of Conventional and Hybrid TMLI Topologies

This section presents the classification of traditional and hybrid topologies of TMLIs for PV applications. Figure 1 shows the overall classification of these topologies, in which both traditional and hybrid topologies are classified into single-phase and three-phase inverters. The effective utilization of single-phase inverters in a variety of residential, commercial, and industrial applications has significantly contributed to the development and use of three-phase inverters, extending their wide range for high-power applications across multiple industries [51,52].

Single and three-phase inverters are subdivided into two-level voltage source inverters (VSI) and MLIs. For various applications, MLIs are the best choice because they can overcome power quality issues and improve the THD in the output waveform while providing high efficiency and reliability [53–55]. The voltage stress across the switches is significantly reduced in these MLIs [56]. MLIs are further divided into transformer-based and transformerless inverters. Implementing transformerless operation can considerably reduce both the cost and size of the inverter while also removing copper and core losses, thereby increasing the overall efficiency [57–59]. Figure 2 shows the configuration of single- and three-phase grid-connected PV systems. Solar PV panels in a PV system produce DC, which is highly reliant on climate and PV terminal voltage. Solar energy is converted into electrical energy using PV cells, which are then transferred to the grid using a PV inverter and other additional components [60,61]. The entire system can be either transformer-based or transformerless. The transformer helps to step up the voltage level and provides galvanic isolation between the PV modules and the grid, preventing current flow leakage [62]. However, a bulky transformer increases the size and weight while decreasing the system efficiency, owing to copper and core losses.

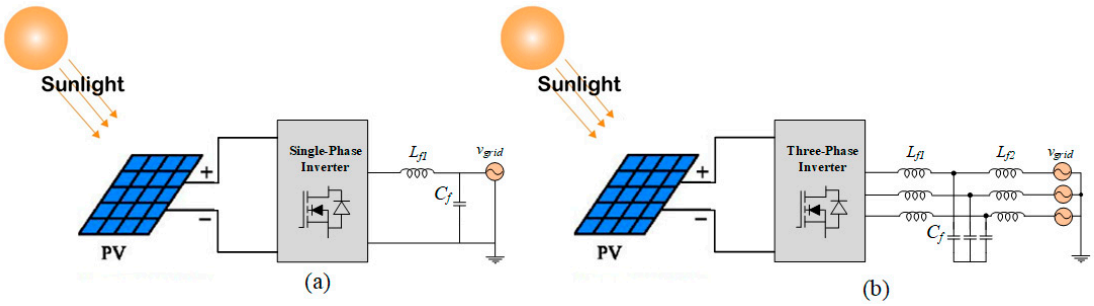

Figure 2. Grid-connected PV system. (**a**) Single-phase system; (**b**) three-phase system.

2.1. Conventional Topologies of TMLIs

Cascaded H-bridge, NPC, ANPC, and FC inverters are some of the most commonly used and considered foundations of multilevel inverters. The use of these inverters has increased due to their multilevel capability and transformerless operation. Each type of MLI has its benefits and drawbacks, and the choice of inverter depends on the specific application requirements. In this section, these four conventional topologies of TMLIs for single- and three-phase applications are discussed.

2.1.1. NPC TMLIs

The most common topologies of MLIs applied to PV systems are neutral-point-clamped (NPC) inverters [63]. They are commonly used in single-phase and three-phase applications, as shown in Figure 3 [64,65]. The single-phase consists of one leg, and the three-phase consists of three legs, each of which is composed of four switches and two voltage clamping diodes, as shown in Figure 3. These diodes are used to regulate the voltage on the DC bus and achieve the desired output voltage level in MLIs. They also help to maintain the balance of voltages in the inverter by allowing current to flow to/from the neutral point when needed [63]. The diodes of the NPC inverter are selected to have the same rated voltage. This implies that they can block voltage levels that are not intended for inverter operation [64]. The concept behind this is to divide the DC input voltage into different levels using clamping diodes and capacitors. The number of levels is determined by the number of capacitors used [65]. In theory, any number of voltage levels can be achieved by using this topology. Reduced voltage stress on switches, lower harmonics, and improved output waveform quality are among the benefits of NPC inverters [66]. Owing to their numerous advantages and important characteristics, NPC inverters have attracted significant interest in PV applications. The connection of the DC-link midpoint to the grid neutral is a key benefit of this topology for transformerless applications. As a result,

the leakage current, which is a significant challenge in transformerless inverters, can be significantly reduced using redundant switching states [67,68]. However, there are two major drawbacks to this topology: the increased number of active components and the requirement for voltage-balancing of the DC-link capacitors. Furthermore, power device losses may not be evenly distributed [69].

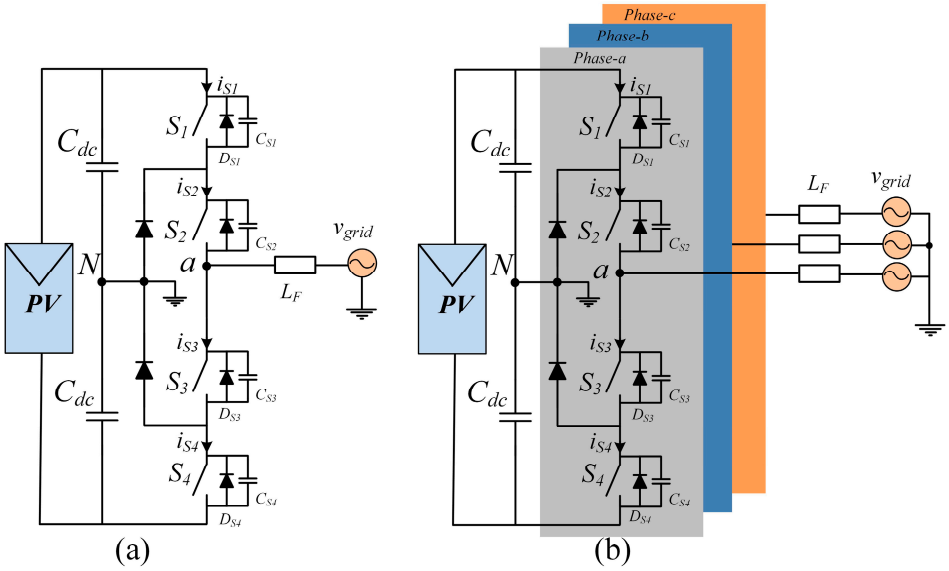

Figure 3. NPC TMLI. (**a**) Single-phase; (**b**) three-phase.

2.1.2. Cascaded TMLIs

A cascaded multilevel inverter (CMLI) was introduced as a power electronic topology in the late 1990s [70]. The cascaded H-bridge (CHB) multilevel inverter is an advanced topology that has emerged as a modification of the traditional two-level inverters. In both single-phase and three-phase configurations (see Figure 4), multiple H-bridge cells are connected in series [28–30]. Each H-bridge cell consists of four power switches and a PV/DC source. The desired output voltage level can be achieved by controlling the switching states of the power switches in each H-bridge cell. The number of H-bridge cells corresponds to the number of the desired voltage levels [71]. In three-phase CHB TMLIs, multiple H-bridge cells are connected in series in each phase leg. CHB MLI topology represents a significant advancement over the traditional two-level inverter, providing greater flexibility in generating multiple voltage levels, reducing harmonics, and achieving high-quality output waveforms [72,73]. However, it has some limitations that need to be considered carefully when designing the cascaded multilevel inverters. One significant limitation is the increased complexity and cost compared with traditional two-level inverters. CHB topology requires a larger number of power switches, capacitors, and control circuits, resulting in higher system complexity and cost [74]. Additionally, an increased number of components may lead to increased power loss and an overall low efficiency. Moreover, the control strategy for CHB MLI is more complex and requires advanced modulation techniques and sophisticated control algorithms [75]. This complexity may pose challenges in terms of system design, implementation, and maintenance.

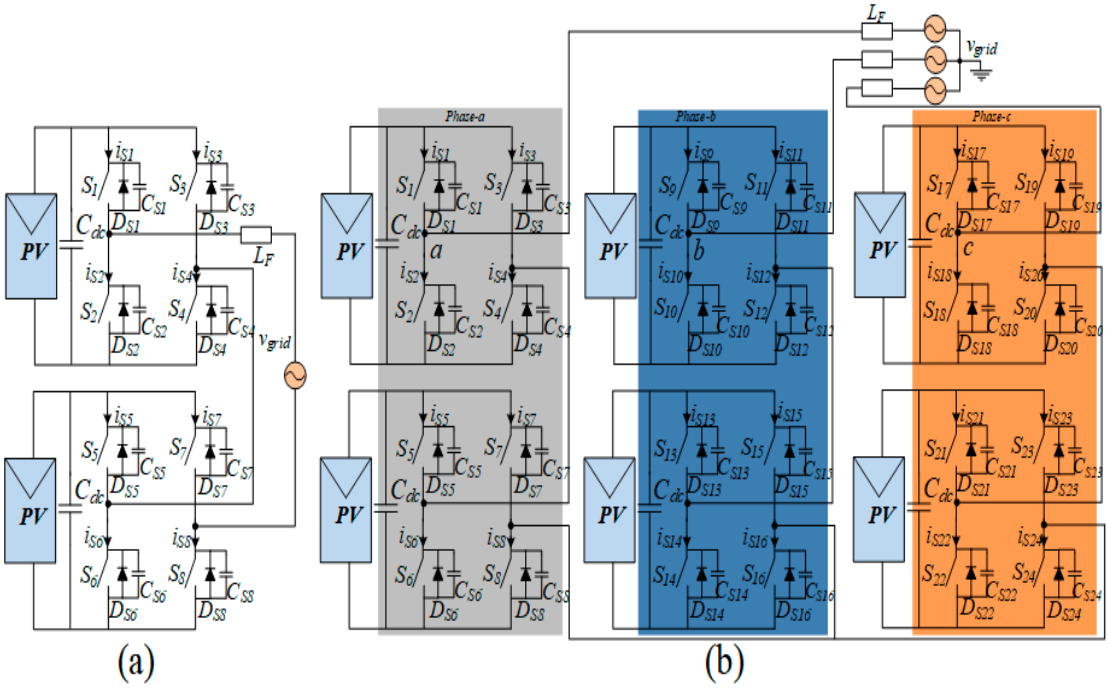

Figure 4. CHB TMLI. (**a**) Single-phase; (**b**) three-phase.

2.1.3. FC TMLIs

The flying capacitor (FC) multilevel inverter is another advanced power electronic topology that offers several advantages, such as improved waveform quality and reduced harmonic distortion. It features a unique topology that uses a series of flying capacitors to achieve multiple voltage levels [41,42]. In the FC multilevel inverter, each phase leg consists of multiple capacitors, typically three or more, connected in a ladder-like configuration between the PV/DC source and power switches, as shown in Figure 5. These FCs dynamically distribute the voltage among themselves to generate the desired output voltage waveform [76,77].

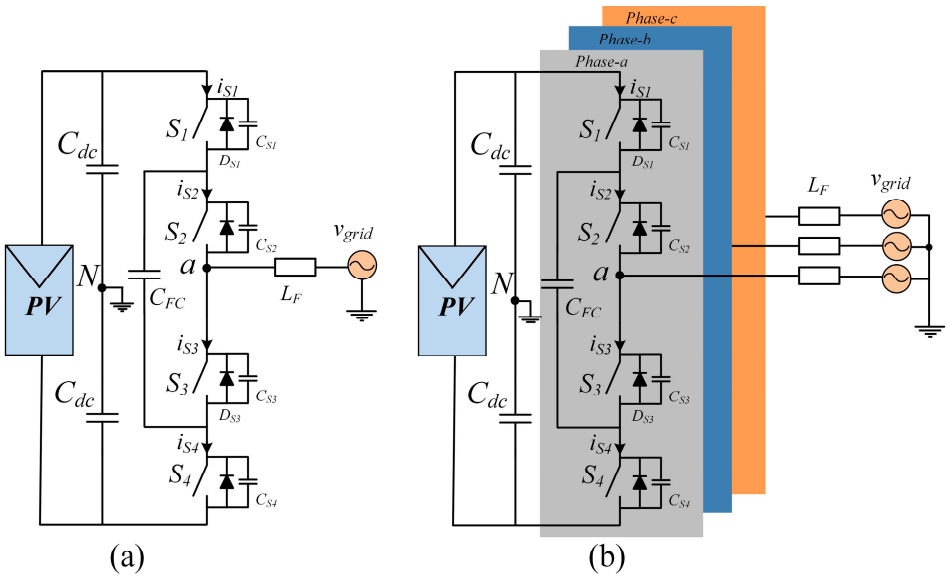

Figure 5. FC TMLI. (**a**) Single-phase; (**b**) three-phase.

By controlling the voltage-sharing among the capacitors, the FC multilevel inverter achieves an increased voltage resolution and improved waveform quality. This topol-

ogy is applicable to both single-phase and three-phase systems, enabling efficient power conversion in various applications such as renewable energy systems, motor drives, and grid-connected devices [78–82]. However, it is important to consider the limitations of FC MLI, including the increased complexity and cost associated with a larger number of capacitors and control circuits. Additionally, voltage imbalances among flying capacitors and higher voltage stresses on the capacitors can affect system performance and efficiency [83–85]. Therefore, proper design considerations and control strategies are crucial for the effective implementation of the FC TMLI topology.

2.1.4. ANPC TMLIs

The active neutral-point-clamped (ANPC) inverter shown in Figure 6 offers significant advantages over the traditional NPC for both single-phase and three-phase inverters [86–90]. The ANPC inverter operates by utilizing a combination of power semiconductor devices, typically insulated gate bipolar transistors (IGBTs) or MOSFETS, and diodes, similar to the NPC inverter.

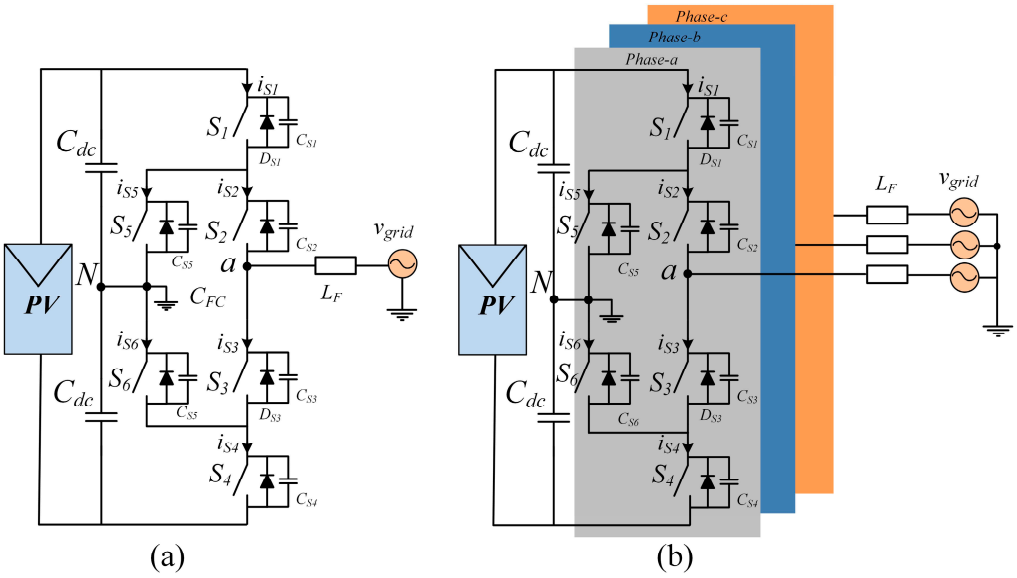

Figure 6. ANPC TMLI. (**a**) Single-phase; (**b**) three-phase.

However, unlike the NPC inverter, the ANPC inverter incorporates active clamping techniques to regulate the neutral-point voltage [91]. By actively controlling the voltage across the neutral point, the ANPC inverter can achieve improved power balancing and mitigate the voltage imbalance commonly associated with the NPC inverter [92,93]. This feature allows for better utilization of the DC-link voltage, reduced power loss, and improved efficiency. Moreover, the ANPC inverter offers flexibility in choosing voltage levels, allowing for a higher output voltage quality [94]. There are also some drawbacks associated with ANPC inverters. More complex control strategies are required to ensure proper clamping and balanced operation, which can increase the complexity of the control algorithms [95]. Additionally, the ANPC inverter may have a higher component count than the NPC inverter, leading to increased cost and complexity in the hardware design. Despite these drawbacks, the benefits of improved power balancing, increased efficiency, and improved voltage quality make the ANPC inverter an attractive option for applications that require precise control, high efficiency, and reduced power loss [96].

2.2. Hybrid Topologies of RC-TMLIs

Hybrid inverter topologies are made by combining different inverter topologies, such as FC, NPC, ANPC, and cascaded H-bridge inverters, etc. For an effective multilevel operation, these hybrid inverters have better performance characteristics and require

fewer components. The following section provides a detailed explanation of the reduced-component TMLIs (RC-TMLIs).

2.2.1. Single-Phase RC-TMLIs

High Step-Up Five-Level RC-TMLI

Figure 7 shows a single-phase reduced-component transformerless multilevel inverter (RC-TMLI) [97] providing the feature of boosting the output voltage. This TMLI is composed of three major components: a traditional boost converter (TBC), a switch-diode-capacitor cell (SDCC), and a full H-bridge inverter (FHB). Each of these three components serves a distinct purpose, acting as a voltage step-up stage, level generation stage, and inversion stage. Interestingly, using only a single DC power source, three power diodes, two capacitors, six switches, and an input inductor, this setup can generate five different voltage levels. The modulation methodology incorporated for this proposed topology is the level shift multicarrier-based pulse-width modulation (PWM) technique. Furthermore, it operates at high frequencies with only four switches, resulting in low overall switching loss. Compared to other traditional five-level inverters described in [32,67,79], this topology stands out because of its boosting capability, use of a single DC power source, and lower switch count. However, with six switching states in each half cycle and a total of 12 modes, the proposed topology does present a complexity in modulation. The total harmonic distortion (THD), defined as a percentage index quantifying the unwanted harmonics present in a waveform, presented for the output voltage is 40.48% [97].

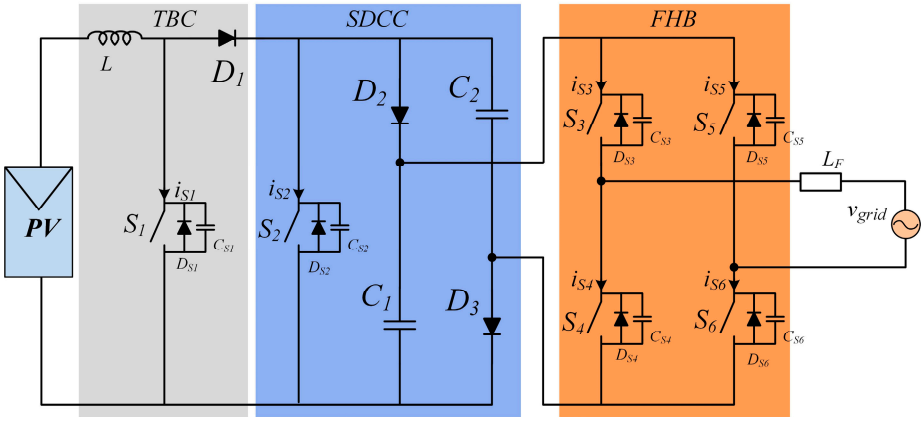

Figure 7. High step-up 5 level RC-TMLI.

With previously proposed topologies and realizing a voltage step-down inversion as well as modifying the transformerless topology to achieve a step-up voltage inversion but having to incorporate two DC sources, an important point worth considering for this topology is the realization of step-up voltage at the output through a single DC source.

Table 1 provides a summary of comparisons between popular five-level inverter designs and the hybrid inverter concept. In contrast to the traditional five-level configurations [27,32,54], the proposed inverter reduces the number of power switches and diodes, resulting in a less costly and more compact system. This topology has received much attention owing to its simple structure, user-friendly control, and ability to achieve a high step-up voltage ratio. Moreover, the proposed topology is also efficient in terms of voltage stress as it incorporates comparatively few diodes as compared to other five-level inverters.

FCHB-Type RC-TMLI

The power circuit configuration of a nine-level inverter [98] is shown in Figure 8, which includes 3 capacitors, 10 switches, and a single PV/DC source.

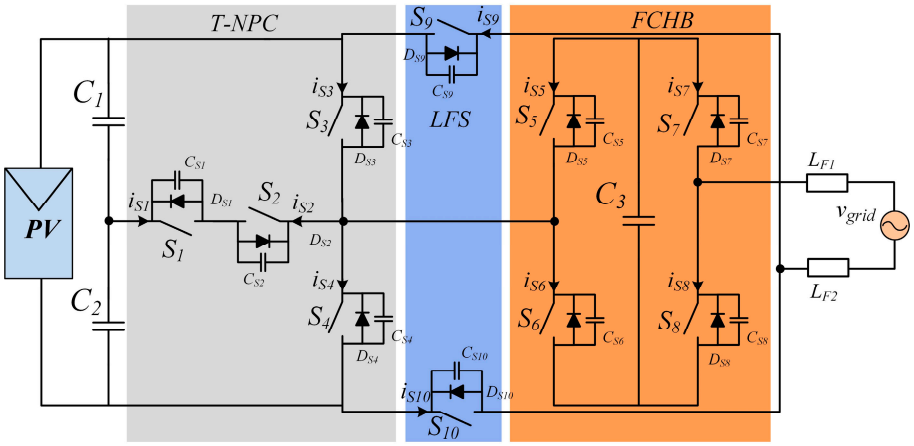

Figure 8. FCHB-type RC-TMLI.

This inverter is built by combining a T-type NPC inverter with an FC H-bridge (FCHB) in a cascade configuration. In addition, two low-frequency switches (LFS) are used to bridge the DC link, allowing the inverter to generate a nine-level waveform. Along with the implementation of a sensorless PWM technique for voltage regulation, the combination of T-NPC and FC offers several advantages, including a reduced number of power components such as switches, diodes, and capacitors. With a reduced number of diodes, the voltage stress is comparatively less, thus improving efficiency. Furthermore, it has a modularity that distinguishes it from other inverters [99,100] that produce an equivalent number of voltage levels. This resulting configuration is readily extendable to support a greater number of voltage levels by simply adding an additional FCHB, as needed, to achieve the desired level count, thus making the proposed topology comparatively simpler in terms of modulation. The topology also presents a comparatively better efficiency as the total number of conducting power switches is less (ranging from four to five for each mode) and with one switch always operating at a low frequency. The proposed configuration thus provides a better efficiency as the number of active switches is less as compared to other topologies.

In an ideal scenario, the inverter would be able to generate nine output voltage levels. Without an LFS unit, the combined T-NPC and FC cascade could generate only five voltage levels. However, by connecting two LFS units across the DC-link, it is possible to access the full magnitude of the DC-link voltage during both the positive and negative half cycles of the output voltage. Consequently, additional output voltage levels can be generated.

Compared with traditional inverter designs [99–101], the remarkable contribution of this inverter is its ability to produce a nine-level waveform while using fewer components. Another important feature worth considering is from an economic aspect. The proposed configuration employing only one FC bridge brings about an overall reduction in cost. An important characteristic of this inverter is its resilience; if the FC H-bridge fails, it can be bypassed. This allows the inverter to continue operating as a five-level inverter at its rated power capacity, even though the power quality is compromised.

DSCC-HBC RC-TMLI

Figure 9 depicts the presented nine-level inverter [102], which is divided into two stages. The first stage employs a developed switched-capacitor circuit (DSCC), which differs from conventional SC cells described in [103,104] by its ability to generate a greater number of voltage levels with fewer components. In the next phase, an H-bridge circuit (HBC) is used to reverse the polarity of the front-end output. The suggested inverter can produce nine distinct output voltage levels under ideal conditions. To achieve this, a single PV/DC voltage source, two capacitors, two diodes, and nine power switches are required.

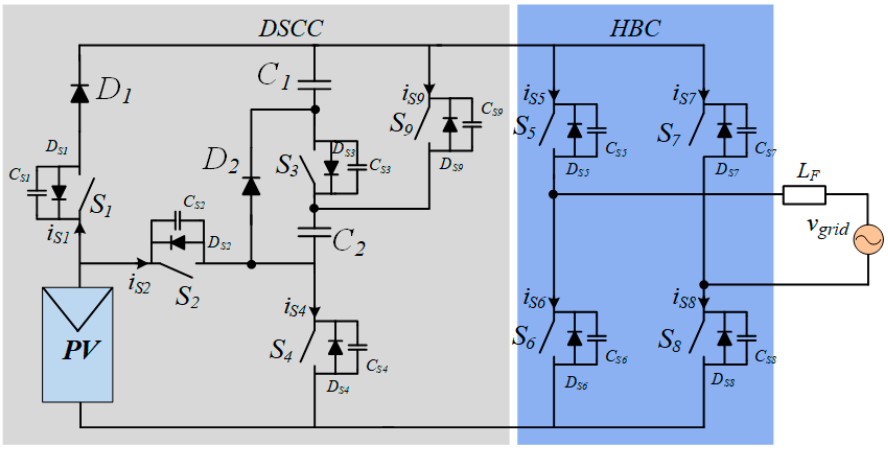

Figure 9. DSCC-HBC RC-TMLI.

The voltage stress on the power devices is reduced, which expands their potential applications. The nine-level inverter also has built-in self-voltage balancing, which simplifies the modulation algorithm. Compared with traditional nine-level inverter topologies [99–101], this topology can achieve a same-level staircase output with a single voltage source, fewer power devices, and lower voltage stress.

Hybrid ANPC-LVS RC-TMLI

The ANPC inverter [87–92] is a hybrid TMLI, which is derived from NPC and FC converters [64,67,76,78–81], that combines the resilience of NPC with the adaptability of FC. This combination incorporates the advantages of both the NPC and FC in the ANPC converter, making it suitable for a wide range of industrial applications. ANPC is typically expanded to achieve higher levels by adding more FC units [105,106]. These components are critical in terms of the cost, dimensions, power density, and complexity of FC-based converters. Furthermore, the dimensions and cost of capacitors are influenced by their voltage ratings, with higher voltage-rating capacitors being significantly more expensive and larger in size. Consequently, considering cost and power density evaluations, the voltage ratings and variety of FCs play a crucial and influential role in FC-based converters, as indicated in [48].

The conventional 11-level ANPC converter is composed of an NPC and four 2-level FC cells. However, the 11-level TMLI (Figure 10) described in [107] comprises of a 5-level ANPC and a low-voltage submodule (LVS). It uses a single FC and a smaller number of high-frequency switches. As a result, the voltage variation, voltage ratings, stored energy, and the number of expensive and bulky FCs are significantly reduced.

The experimental process involves the implementation of a combination of both level-shifted as well as phase-shifted PWM in order to generate the reference signals for the submodule and the 5L-ANPC. Furthermore, when the enhanced submodule operates at low voltage and power levels, the output voltage levels double. As a result, by doubling the number of output voltage levels, this augmentation significantly improves the output voltage quality of the 11-level ANPC converters while incurring minimal additional cost and size for the 5-level ANPC converter. These improvements result in a significant reduction in the size of the large and costly output LC filter and an improvement in both the dynamic and steady-state performance [107].

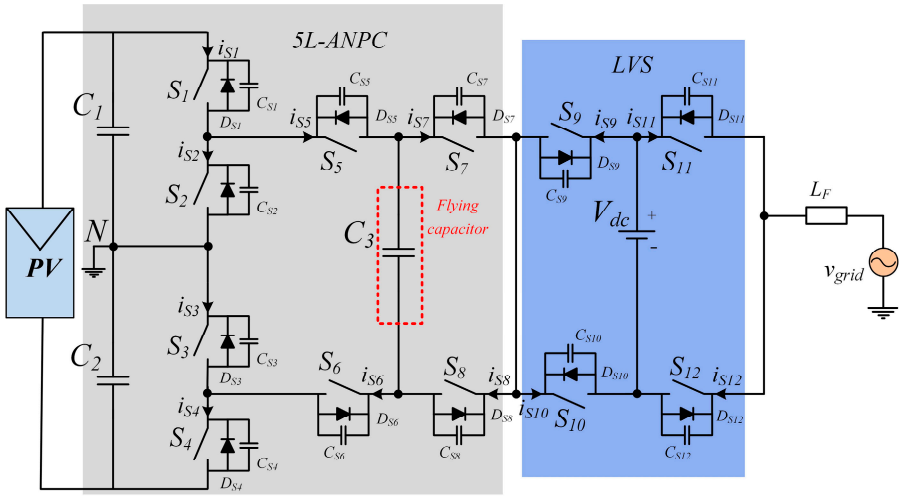

Figure 10. Hybrid ANPC-LVS.

Boost ANPC RC-TMLI

The seven-level ANPC inverter [108] is created by adding four extra switches to the five-level ANPC inverter [109], as shown in Figure 11. It comprises nine switches, one floating capacitor (C1), and two DC-link capacitors (C1 and C2). Compared to the inverter described in [109], it improves both the voltage gain and the number of output levels. More specifically, it allows for an increase in voltage gain from 1 to 1.5, or 2.5, as well as an increase in the number of output levels to 7, 9, and 11.

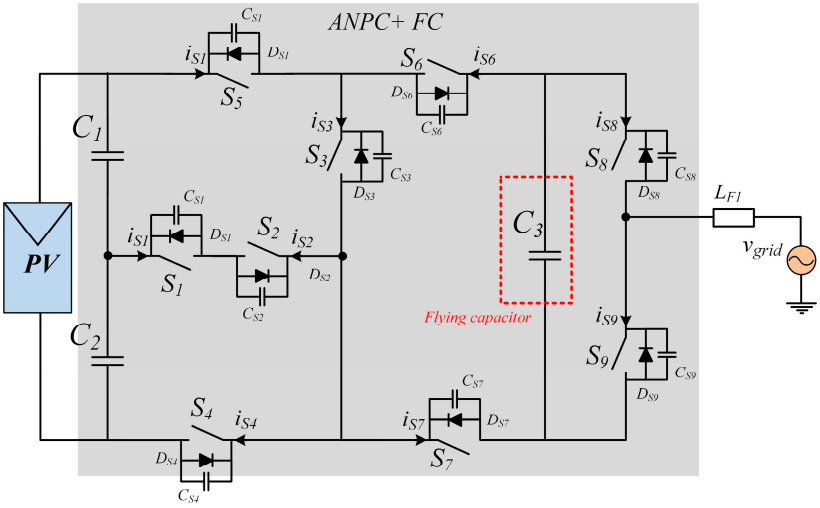

Figure 11. Seven-level ANPC RC-TMLI.

By connecting C3 in series with DC link capacitors (C1 and C2), the additional four switches enable the generation of two more levels. Switch integration is possible because C3 is not directly connected to the DC link. This inverter is known as a seven-level ANPC boost inverter because it can generate two additional voltage levels while increasing the voltage gain from 1 to 1.5.

By incorporating an additional FC and three power switches, the seven-level ANPC inverter can easily be upgraded to achieve higher voltage levels as shown in Figure 12. Two FCs are used to achieve a greater number of voltage levels. During operation, either the upper or lower DC-link capacitor charges these two FCs in series, with each reaching a charge of $0.25V_C$, where $Vc = Vc_1 + Vc_2$.

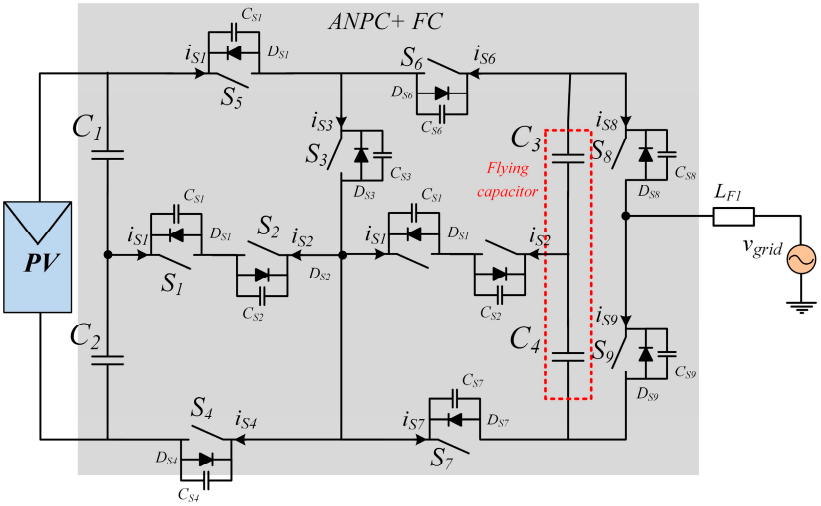

Figure 12. Nine/eleven-level ANPC RC-TMLI.

This configuration helps to generate nine voltage levels. To increase the number of voltage levels without changing the structure of the nine-level ANPC inverter, each FC was charged to Vc, resulting in a maximum achievable voltage of $2.5V_C$. The number of voltage levels also increased to 11 because each level now has a magnitude of $0.5V_C$. An important feature of this topology is the fact that a boost in voltage is achieved without the requirement of boost converter or any voltage-balancing process. Moreover, another significant improvement is in terms of voltage stress, where standard unipolar switches are employed that provide the necessary bidirectional blocking without having to use any antiparallel diodes. An increase in total switch count, however, is observed for this topology as compared to topologies mentioned in [110] and [109], adding to the overall cost, but also providing generation of high voltage as well as boost in voltage.

2.2.2. Control Approaches of Hybrid Single-Phase RC-TMLI Topologies

This section provides a detailed overview of the control strategies employed for each of the single-phase, hybrid topologies for the RC-TMLI mentioned in the previous section.

High Step-Up Five-Level RC-TMLI

This reduced component topology [97] provides a boost in the output voltage and employs the pulse-width modulation method based on the level-shift multicarrier. Two stages are carried out for both the positive as well as negative output voltages, respectively.

1. *Positive Output Voltage:*

During this period, the switches S_4 and S_5 are kept OFF. In the first stage in this period, the switching action is carried out by switch S_3, owing to the common intersection of both the lower carrier waveform and the sinusoidal reference signal. Switch S_6 is kept ON, whereas while switch S_2 is maintained in the OFF state. The output voltage of the inverter in this case comes out to be either 0 or U_c.

The second stage consists of the intersection of the upper carrier waveform and reference sinusoidal signal, during which the switching action is performed by switch S_2. The switch S_3 is kept ON. The output of this stage is an alternate of the first stage, and the inverter output is either u_c or $2U_C$.

2. *Negative Output Voltage:*

In order to obtain a negative inverter output, switches S_3 and S_6 are kept in the OFF state.

The two stages for the negative output voltage period are opposite to that of the positive output period.

The polarity of inverter output voltage is determined by the working of switches S_3–S_6, whereas the amplitude of the output voltage is determined by the switching action of switch S_2.

FCHB-Type RC-TMLI

This cascade topology [98] combining T-type NPC inverter with an FC H-bridge (FCHB) makes use of the multilevel pulse-width-modulation technique integrating a voltage-balancing control as shown in Figure 13. This control operates by comparing the carrier signal with four reference signals. These four reference signals are similar in terms of frequency, amplitude and phase. The only difference among the four is the offset added to each. Each offset added is equivalent to the maximum amplitude value of the carrier signal. The modulation index incorporates the four reference signals and is given by:

$$m_a = \frac{V_m}{4 \times V_c}$$

where V_m represents the peak value of the reference signal, and V_c represents the peak value of the carrier signal.

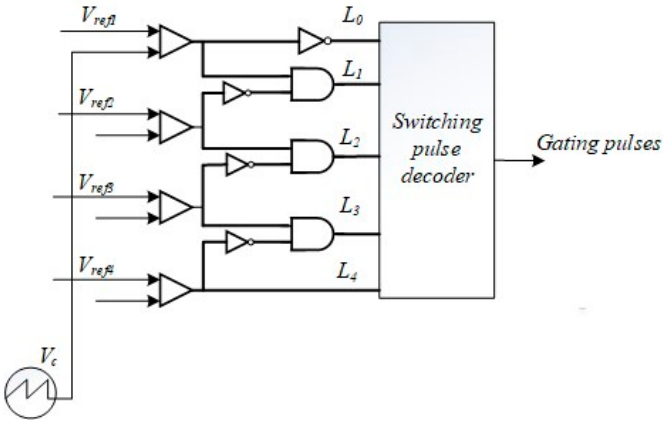

Figure 13. PWM modulator for FCHB type RC-TMLI.

The PWM signals are thus generated by the comparison of the carrier and reference signals. This is followed by implementation of specific logic operations in comparators in order to acquire the output voltage that is required. The binary interpretations obtained are then stored in the switching pulse decoder in order to select a specific switching state and generate the requisite gating pulses. The switching losses are also considered in the operation of the control due to transitions for the minimization of which the redundant switching states are included in order to generate a zero-voltage output. Through the deployment of this technique, an inverter output voltage consisting of nine levels is obtained, which does not make use of any voltage sensors. This in turn leads to a considerable reduction in the complex control calculations. Along with being simple in implementation, the mentioned PWM strategy is economical as well as it only makes use of a carrier signal, sinusoidal reference signals that are level-shifted and logic gates.

DSCC-HBC RC-TMLI

The operational working of the topology in [102] is based on the high-frequency AC distribution system. This includes the transformation of DC voltage by the inverter into a high-frequency staircase output by incorporating fewer components and an increase in the voltage levels. Four quasi-square waves are employed with amplitudes $\pm V_{dc}/2$ in order to obtain a staircase voltage output containing nine levels. With the output frequency of the high frequency inverter being very high and considering the high switching frequency and switching losses associated with modulation methods related to high frequency, the

fundamental frequency modulation strategy is employed. The working of the proposed topology is in two stages. The first stage is the frontend stage consisting of a switched capacitor circuit using fewer components and providing a large number of voltage levels in the output. The backend stage makes use of a H-bridge circuit that changes the polarity of the output acquired from the frontend. The modulation strategy for the proposed nine-level inverter also includes the implementation of the selected harmonic elimination strategy through which the 5th, 7th and 11th harmonics are selected to be removed. The modulation index and conduction angle of the four square waves are determined from below mentioned formula. The obtained conduction angles are associated with the driving signals for the switches S_1–S_9.

Hybrid ANPC-LVS RC-TMLI

The switching strategy proposed and implemented for this 11-level topology [107] conducts the regulation of the output voltage of the flying capacitor to the voltage level that is desired without using any closed-loop control. This brings about a considerable reduction in control complexity.

The proposed switching method consists of a combination of a level-shifted as well as phase-shifted PWM in order to generate the low-voltage reference signals. The even levels in the output are generated by the five-level ANPC module, whereas the odd levels are acquired from the low-voltage submodule. The switching strategy consists of the comparison of a sinusoidal reference waveform with ten level-shifted and phase-shifted carrier signals. The output signals from the comparators are then added to develop an 11-level staircase modified reference signal. This is followed by the generation of a low-frequency five-level staircase signal from the five-level ANPC submodule, which is applied to switches S_3–S_6. A high frequency three-level reference is generated from the low-voltage control, which is then applied to switches S_1 and S_2. In this way, through the combination of phase-shifted and level-shifted pulse-width modulation techniques, some switches are operated at the fundamental frequency, whereas some are operated at the carrier frequency, generating an 11-level high-frequency output voltage. The proposed switching methodology combines a low-frequency and high-voltage submodule with a low-voltage, high-frequency submodule in order to generate a multilevel output that has optimized efficiency and a reduced number of harmonics.

Boost ANPC RC-TMLI

The output voltage of the proposed ANPC topology [109] is controlled through the implementation of a level-shifted pulse-width modulation strategy. This modulation scheme comprises of three parts and is shown in Figure 14. The sinusoidal reference waveform is compared with five level-shifted carrier signals in order to develop the necessary switching states. These switching states are combined using a digital circuit in order to generate the requisite switching signal for each switch.

Table 1 provides a summary of the different control approaches used for hybrid single-phase RC-TMLI topologies.

Table 1. Control approaches of hybrid single-phase RC-TMLI topologies.

Control Approaches				
High Step-Up RC-TMLI	**FCHB-Type RC-TMLI**	**DSCC HBC RC-TMLI**	**Hybrid ANPC**	**Boost ANPC**
[97] Level-shift PWM	[98] Multilevel PWM with voltage control	[102] Quasi wave PWM	[107] Level-shift phase-shift PWM	[109] Level-shift PWM

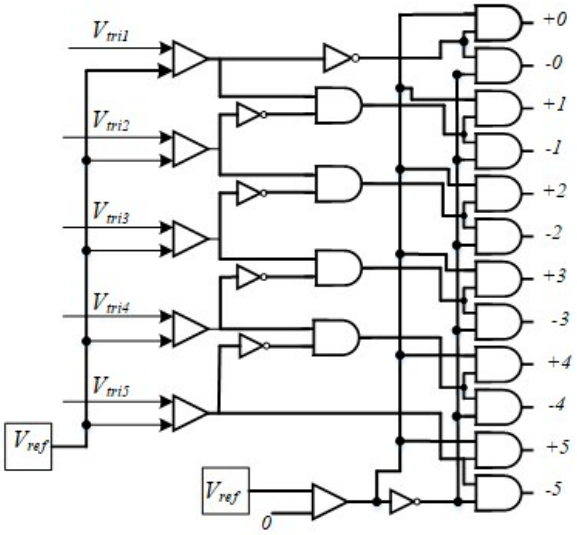

Figure 14. Modulation scheme of the 11L Boost ANPC RC-TMLI.

2.2.3. Three-Phase RC-TMLIs

Three-Phase Three-Level Two-Leg RC TMLI

Figure 15 shows a three-phase three-level two-leg NPC inverter [111]. This is a combination of a conventional four-switch inverter [112] and a three-phase three-level inverter topology. The number of active switches is reduced from 12 to 8 in the traditional three-phase three-level NPC inverter. Similarly, the number of clamping diodes is reduced from six to four [111–113].

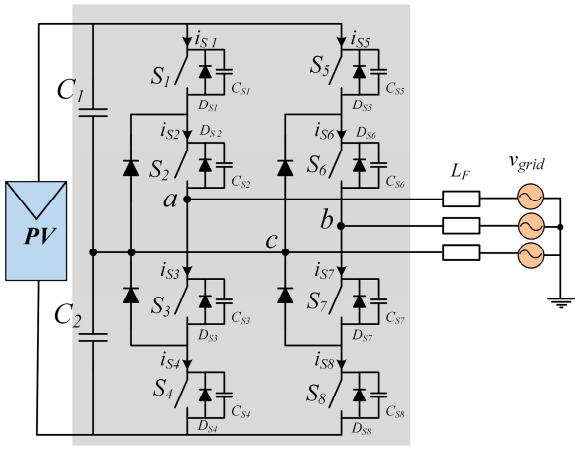

Figure 15. Three-phase 2-leg RC-TMLI.

Compared with traditional CHB and FC topologies, it requires a smaller number of components for multilevel operations. CHB requires separate DC sources for each half-bridge [29,30], whereas FC requires large capacitors that increase the size and volume [42,82,83]. Therefore, the number of components for a three-phase three-level inverter is drastically reduced in [111], and a detailed comparison of this topology in terms of component count with traditional inverters is presented in Table 4. However, the limitation of this topology lies in its practical restriction, as it operates with a lower output voltage range, which is only half that of conventional three-leg three-level structures [114,115]. Space vector diagrams for three-leg three-level and two-leg three-level configurations are presented in [63] and [115], respectively. These diagrams clearly show the restricted voltage range in a two-leg three-level inverter. The optimum features provided by this topology thus include a significant reduction in cost and volume since the conventional three-level NPC infrastructure is employed, which does not require the use of bidirectional switches,

capacitors and clamping diodes. With a limitation in its practical implementation, as previously described, this topology also generates a balanced voltage of optimum quality.

Hybrid 9-Level RC-TMLI

A symmetrical hybrid nine-level inverter was presented in [116] to increase the output voltage levels while decreasing the number of DC/PV sources, as shown in Figure 16.

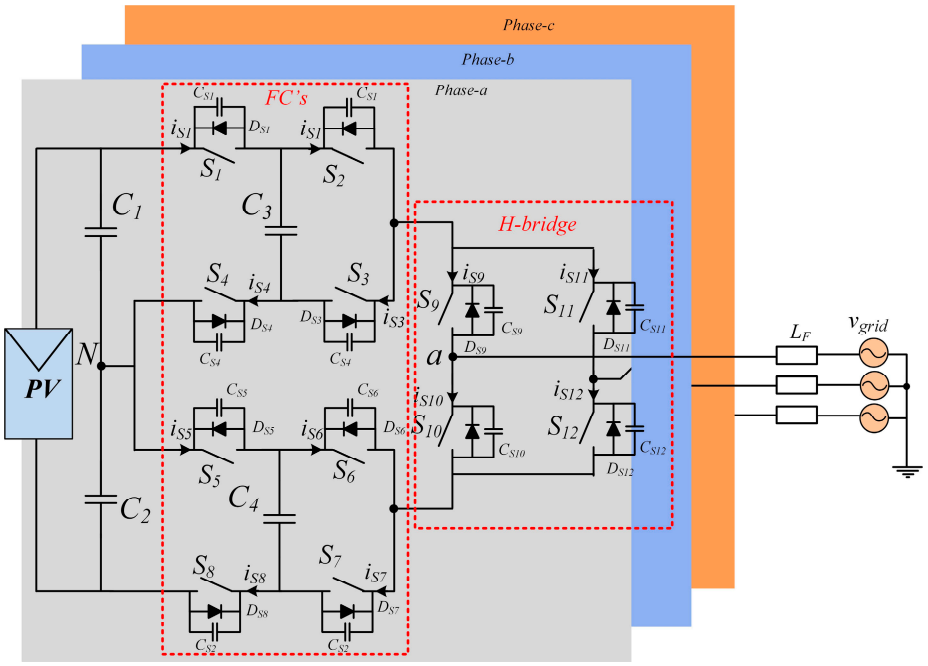

Figure 16. Hybrid 9-level RC-TMLI.

The symmetrical hybrid nine-level inverter is composed of two three-level FC converters and a half-bridge. Each three-level FC consists of four switches and an FC, whereas the H-bridge consists of four switches. The output voltage of two three-level FCs has five levels, which can be named a five-level DC/DC converter. Each phase of this inverter comprises a five-level DC/DC converter cell and an H-bridge cell. The pulse-width-modulation technique implemented is the voltage balancing methodology for capacitors based on the phase-shifting technique. The following operating rules are to be followed to create nine output voltage levels. (1) Switches S_1, S_2, S_8, S_7, S_9, S_{11}, and S_4, S_3, S_5, S_6, S_{10}, S_{12} should be operated in a complementary way, respectively. (2) The H-bridge should be operated using bipolar modulation. Based on the aforementioned operating rules, each phase can generate nine output voltage levels. Compared to the conventional hybrid cascaded nine-level converter [117], the number of isolated DC sources is significantly reduced. A detailed comparison of the component count with traditional topologies is presented in Table 4. Analysis of the performance parameters for the topology is presented in Table 5.

Hybrid 13-Level RC-TMLI

The multilevel configuration is built by sequentially connecting a T-type inverter with three levels to a H-bridge module and a three-level FC unit [118]. At the pole voltage, this configuration produces a 13-level output. Each phase in the circuit comprises two stages, as shown in Figure 17. There are 10 switches (S_1 to S_{10}) and 2 FCs (C_3 and C_4). The inverter's first stage is a T-type NPC structure that produces a three-level output, which is then linked in series with the second stage, which is composed of a half-bridge module followed by a three-level FC unit to produce a 13-level output. The DC bus voltage is created by two capacitors, C_1 and C_2, which are maintained at half of the DC-link voltage to balance the neutral-point voltage. V_C is the total DC-link voltage, i.e., $V_C = V_{C1} + V_{C2}$.

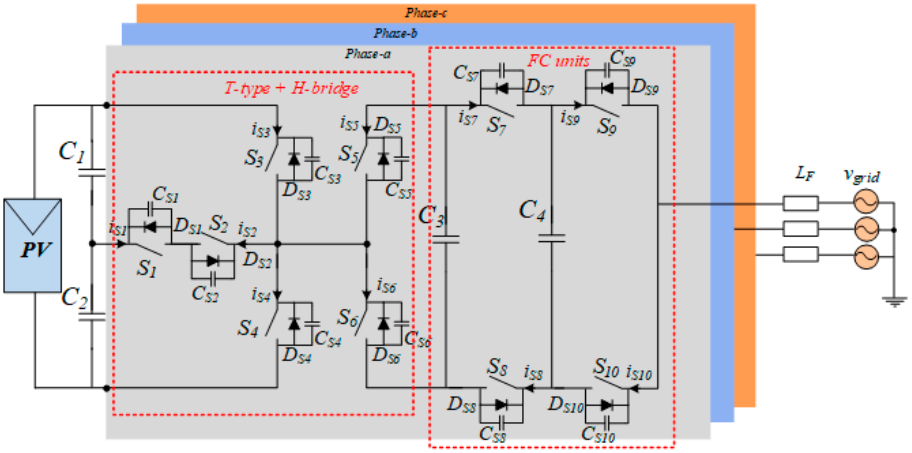

Figure 17. Hybrid 13-level RC-TMLI.

The use of five complementary switch pairs simplifies control while also reducing the need for gate driver circuits and reducing volume. S_1–S_2, for example, are connected in an anti-series configuration to provide a bidirectional current flow to/from the neutral-point of the DC bus. S_3–S_5 handle most of the DC bus voltage stress, S_4–S_6 block $V_{C/4}$, and the remaining four switches in S_7–S_8 and S_9–S_{10} pairs only block $V_{C/8}$. In conclusion, [118] it provides significant benefits, such as a single DC source for 13-level generation, reduced switch requirements, reduced need for FCs, efficient DC-link utilization without lower-order harmonics, and grid suitability. A detailed comparison with other traditional topologies in terms of components is presented in Tables 4 and 5.

Modular TMLI

Modular topology of the TMLI constitutes of one of the most promising applications to be employed in medium- to high-voltage applications. This is due to the many advantages that they present, which include optimum output characteristics, reduction in voltage stress for each component as well as high scalability. Capacitor balancing is the prevalent issue associated with this topology as it leads to unnecessary switching of the power devices involved. In the configuration proposed in [119] and shown in Figure 18, the disturbances and imbalances associated with capacitor voltages have been focused on and assessed. A balancing methodology is thus developed along with an emulator to verify the calculations. Based on this quantitative analysis, a decrease in switching action is acquired, thereby improving efficiency, control and reliability.

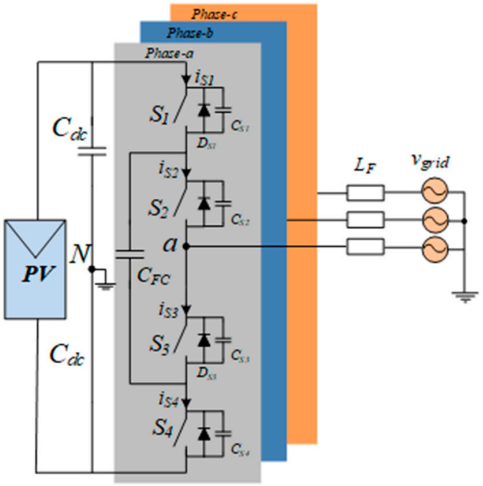

Figure 18. Modular TMLI.

Switched Capacitor TMLI

The transformerless operation of multilevel converters employing switched capacitor units is another configuration of significance owing to features that include boosting of voltage as well as self-voltage balancing of the capacitors involved. Based on the comprehensive review presented in [120], focused on all existing SC TMLI topologies, a quantitative analysis was formulated, assessing the different operational parameters. The topologies assessed include single-source, multiport, midpoint-clamped and hybrid SC TMLIs. Firstly, considering the cost metric, it is concluded in [120] that the hybrid configuration involves fewer power switches for charging capacitors and is the optimum selection from an economic viewpoint, whereas the highest cost is associated with the multiport configuration, as it involves multiple DC sources. A suitable choice when considering the leakage current concern is the midpoint clamped configuration. Considering the output, multiport configuration is the efficient choice in order to acquire high number of voltage levels.

Another switched capacitor nine-level TMLI configuration is proposed in [121], with a focus on reducing switch components, voltage stress as well as leakage current. The topology is shown in Figure 19. The topology involves 12 switches in order to generate nine different voltage levels. The scheme employed for modulation is high-frequency switching. For the prevention of leakage current, the connection scheme regarding common ground is presented. With the decrease in switching component for each level, a reduction in overall cost is obtained.

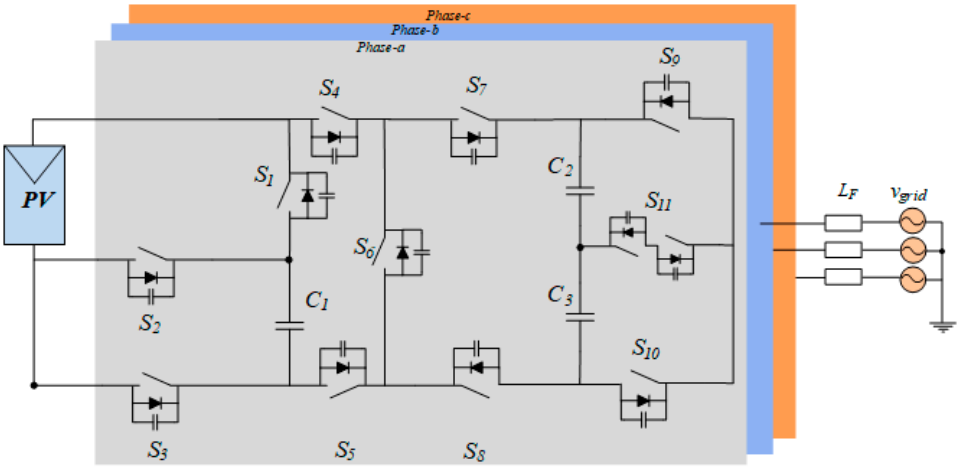

Figure 19. Switched capacitor 9-level TMLI.

Three-Phase TMLI

Another single-source hybrid asymmetrical configuration of the TMLI is presented in [122]. This hybrid structure comprises the combination of the conventional neutral-point clamped converter and cascaded H-bridge with the level-doubling network configuration. The main focus in [122] is to bring about a decrease in the leakage current through the reduction in the requirement for the DC capacitor bus. This is achieved through the merging of the DC buses by utilizing the NPC arrangement. This merge also then leads to the requirement of only one DC source. In order to acquire the balancing of the capacitor, a buck boost converter of low rating is employed, which eliminates the need for a transformer and brings about a significant reduction in overall cost. Along with a reduction in leakage current, the proposed topology provides the features of high efficiency as well as reliability.

A 1:5 asymmetry is incorporated as shown in Figure 20, which indicates the division of voltage within the structure of the inverter. This comprises the division of the DC voltage into two parts with a ratio of 1:5. This asymmetric topology leads to the inverter generating more output levels as compared to the symmetric infrastructure. Another important feature worth considering is the fact that the NPC, which operates at a high level of switching

frequency, leading to switching losses, is operated at a fundamental level frequency in the proposed topology, which makes the losses almost negligible.

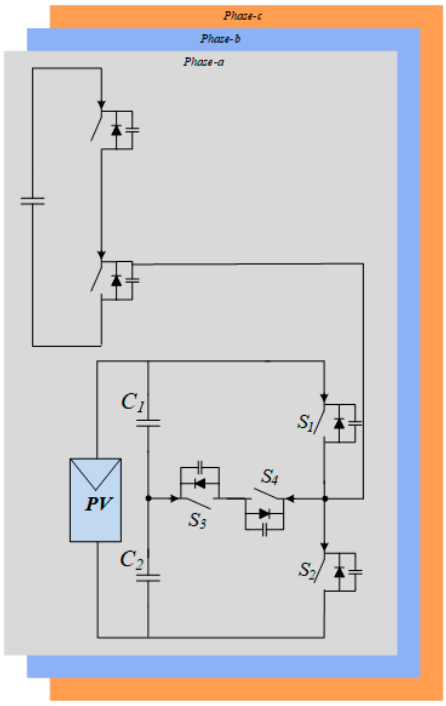

Figure 20. Three-phase TMLI with 1:5 asymmetry.

Self-Balanced Switched Capacitor TMLI

A switched capacitor configuration of the TMLI employing 13 levels is presented in [123] and shown in Figure 21. The main focus is the voltage-boosting feature, which was acquired without the need for any additional circuit arrangement. The circuit employs a single source with the combination of the conventional H-bridge and switched-capacitor circuits, employing a total of three capacitors, two diodes, and 11 switches. While the H-bridge functions to change the polarity of the output voltage, the switched capacitor arrangement provides the requisite for charging and discharging the capacitors. This charging and discharging process takes place along with the rise and fall of the voltage waveform, thus providing the automatic self-balance operation. While the proposed topology operates at a high efficiency, providing a significant boost in the output voltage, the involved switches and diodes lead to the generation of overall losses in the system.

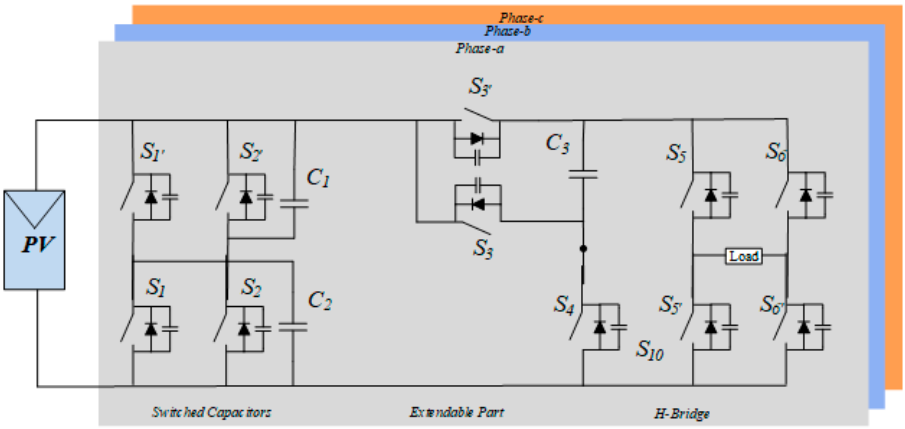

Figure 21. Thirteen-level self-balanced switched capacitor TMLI.

2.2.4. Control Approaches of Hybrid Three-Phase RC-TMLI Topologies

Three-Phase Three-Level Two-Leg RC TMLI

Conventional modulation strategies cannot be implemented on the topology proposed in [111], since one output phase of the inverter is connected to the neutral present between the capacitors. The application of a conventional modulation technique to the four-switch inverter would then lead to one voltage phase not being modulated. So, for the generation of the requisite gate signals for the inverter with a small number of components, the carrier-based PWM strategy is proposed. The modulation scheme for the implemented strategy employs a PI controller and is shown in Figure 22.

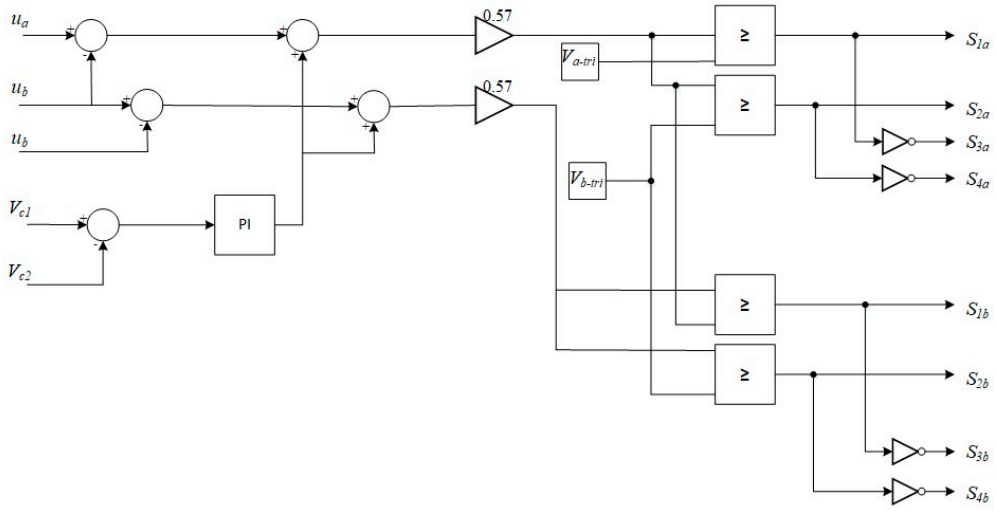

Figure 22. Modulation scheme of three-phase three-level two-leg RC TMLI.

Hybrid Nine-Level RC-TMLI

The modulation strategy of the proposed nine-level hybrid topology [116] comprises two stages in high and low frequencies. For this purpose, the symmetrical inverter is divided into two cells. The first cell is the high-frequency cell that consists of two 3-L converters, the output voltage of which has five levels. This output can be seen as a five-level DC/DC converter for which the switches function at high frequency and the voltage rating is $V_{dc}/4$. The second cell is the low-frequency cell, consisting of an H-bride with a voltage rating of V_{dc} for the four switches that operate at fundamental frequency. Switches S_1, S_2, S_8, S_7, S_9, and S_{11}, and S_4, S_3, S_5, S_6, S_{10}, and S_{12} should be operated in a complementary way, respectively. The H-bridge should be operated using bipolar modulation. Based on the aforementioned operating rules, each phase can generate nine output voltage levels.

Hybrid 13-Level RC-TMLI

In order to generate gate signals for the 10 switches for each phase in the proposed topology [118], a level-shifted sinusoidal PWM strategy is implemented. The voltage output containing 13 levels is obtained; 12 carrier signals with an amplitude of $V_{dc}/8$ are phase-shifted and then compared with the sinusoidal reference voltage waveform. Redundant states are selected on the basis of polarity of current. A square wave offset is included in the reference voltage, which assists in the balancing of voltage for the flying capacitor.

Modular TMLI

The modular technique employed in this topology [119] is the nearest level modulation NLM in which discrete voltage levels are used for the approximation of the sinusoidal waveform. This modulation strategy, shown in Figure 23, comprises of the comparison of the reference waveform with the voltage levels available in converter. The demand voltage

value is rounded off to the nearest level of voltage. The switches are operated on the basis of this value in order to generate the output voltage that is required. These steps are then repeated to generate as well as maintain the output voltage level. The modulation scheme is provided below.

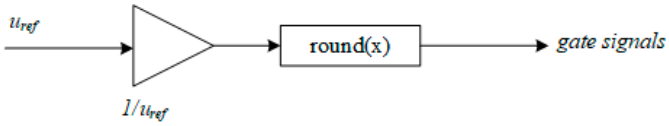

Figure 23. Modulation scheme of modular TMLI.

Switched Capacitor TMLI

The switching operation of the topology [121] is carried out in nine stages, of which five stages are for the positive half cycle, which confirms the working of the topology in asymmetric function. The modulation scheme is shown in Figure 24.

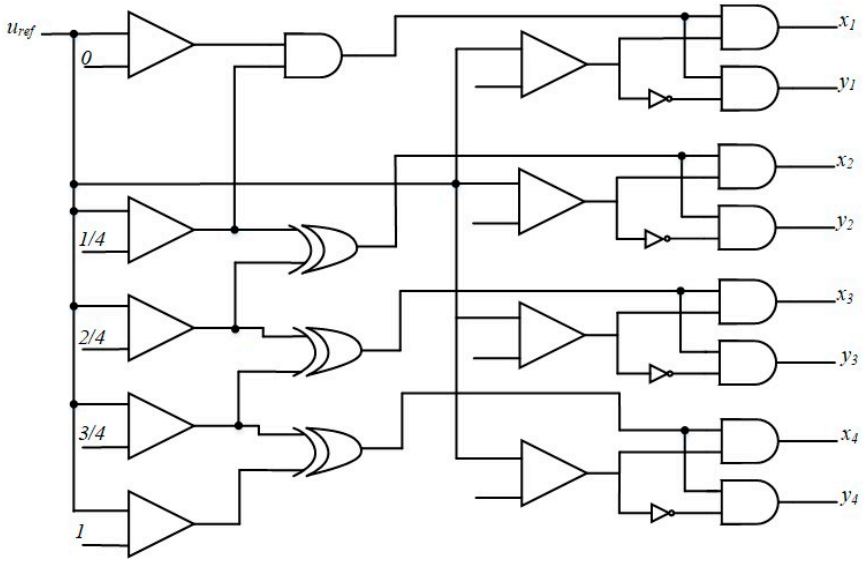

Figure 24. Modulation scheme for switched capacitor TMLI.

1. An output voltage of magnitude 0 is obtained through the simultaneous activation of the switches S_1, S_3, S_4, S_5, S_7, S_8, and S_{10}.
2. A magnitude of $0.5V_{DC}$ at the output is obtained through the activation of switches S_1, S_3, S_4, S_5, S_7, S_8, S_{11}, and S_{12}.
3. Switches S_1, S_3, S_4, S_5, S_7, S_8, and S_9 are activated to attain an output voltage of $1V_{DC}$.
4. Through the activation of switches S_1, S_3, S_4, S_6, S_8, and S_{11}, a magnitude of $1.5V_{DC}$ is obtained at the output.
5. Finally, a $2V_{DC}$ output is obtained through the activation of switches S_1, S_3, S_4, S_6, and S_8.

Three-Phase TMLI

Closed-loop control is implemented as the modulation strategy and for balancing the capacitor voltages in this proposed topology [122]. The modulation strategy is shown in Figure 25. In order to attain a complete balance of the capacitor voltages, two control loops are used. These include the outer voltage and inner current control loops. The difference value between the measured voltage value from the capacitor and voltage that is required (reference value) is calculated and then provided to the PI controller. An inner current control loop is implemented to reduce the amount of ripples and startup in the current. The PWM signal is then generated through the comparison of the carrier signal and output of the controller.

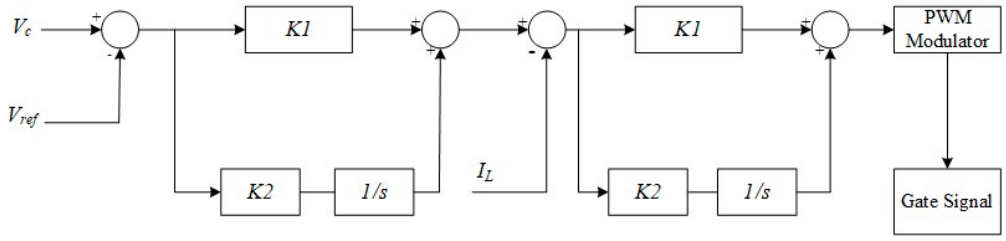

Figure 25. Modulation scheme for three-phase TMLI.

Self Balanced Switched Capacitor TMLI

In this proposed topology [123], the switches are connected in pairs, due to which each pair shares the same gate signals. This reduces the complexity of the control and leads to the requirement of generating fewer gate signals. Moreover, the control circuit is also not required to balance voltages, as the DC capacitors used carry out self-balancing and do not require any additional external circuit. The switching process is mentioned below:

1. The first stage involved a value of 0 for the output voltage, during which switches S_1, S_2, S_3, S_4, S_5, and S_6 are in the active state.
2. The switches S_1, S_2, S_3, S_5, and S_6 are in the active state, leading to the output voltage being equivalent to the DC voltage source.
3. In order to obtain $+2V_{dc}$ at the output, two paths are considered, which both involve switches S_3, S_5, and S_6 to be in the active state and with capacitor C_1 discharging in first path and C_2 discharging in the end.
4. In the next stage, the output voltage is the sum of voltage of both capacitors and the DC source ($+3V_{dc}$). During this stage, all six switches are in the active state.
5. For $+4V_{dc}$ at the output, S_1, S_2, S_3, S_5, and S_6 remain in the active state.

In a similar manner, $+5V_{dc}$, $+6V_{dc}$, and negative voltage levels are obtained. During the generation of these voltage levels, the capacitors are connected in parallel, charge and discharge accordingly. This leads to an automatic self-balancing of the capacitor voltages without the need for an external circuit.

Table 2 provides a summary of the different control approaches implemented for the hybrid three-phase RC-TMLI topologies.

Table 2. Control approaches of hybrid three-phase RC-TMLI topologies.

Control Approaches						
2-leg RC-TMLI	**9-Level RC-TMLI**	**13-Level RC-TMLI**	**Modular RC-TMLI**	**SC RC-TMLI**	**3-Phase TMLI**	**Self-Balanced SC RC-TMLI**
[111]	[116]	[118]	[119]	[121]	[122]	[123]
Carrier PWMPI controller	Bipolar PWM	Level-shifted sinusoidal PWM	Nearest level PWM	Phase disposition PWM	Sinusoidal PWM using voltage, current control	Selective harmonic elimination PWM

2.3. Dual Input RC-TMLI Topologies

Modular RC-TMLI

In comparison to the conventional modular MLI types discussed in [124–127], the inverter described in [117] provides numerous advantages, including a reduced number of components and lower voltage stresses on the switches, regardless of the output voltage level. It consists of only 2 DC sources/PVs and 12 switches, as shown in Figure 26.

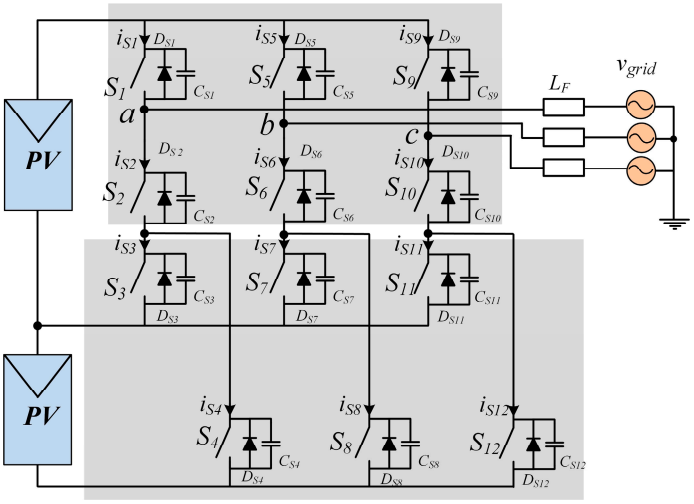

Figure 26. Modular RC-TMLI.

The modulation techniques employed include the sinusoidal pulse-width-modulation SPWM technique. In order to increase the number of levels, multiple sets of three additional switches must be cascaded. By omitting the use of FCs and clamping diodes, this unique configuration distinguishes itself from the established norms of the NPC and FC inverter designs [43,44,126]. This change from tradition provides a slew of compelling benefits and notable distinctions that have a significant impact on the system's performance and characteristics. This configuration simplifies the control strategies, reduces the overall component count, improves the design compactness, extends system lifetime, and ultimately reduces manufacturing costs by eliminating FCs and clamping diodes. These characteristics make it an appealing choice for a wide range of applications, owing to its increased efficiency, dependability, and cost-effectiveness. A detailed comparison of these topologies is presented in Tables 4 and 5.

RCC TMLI

The reduced component count (RCC) five-level configuration is derived from a conventional five-level stacked inverter, which includes two three-level FC inverters (cells) and a selection stage, as described in [127–129]. This inverter variant stands out for its superior reliability in comparison to the traditional FC inverter [83], on the basis of its reduced number of FC components. Nonetheless, it is critical to recognize that this approach results in a greater number of switches, necessitating an equal number of gate drivers and protection modules. Consequently, the overall cost of the inverter system could increase.

Therefore, the RCC five-level topology (shown in Figure 27 and discussed in [125]) effectively addresses the aforementioned challenge by integrating FC cells from all three-phase legs of the stacked inverter into a single set of upper (S_1–S_4) and lower (S_5–S_8) cells. This novel design includes additional three-level NPC sections within each phase circuit, allowing FC cells to be connected to any of the three outputs as desired. For the complete inverter, this setup requires only 20 switches, 6 diodes, and 2 FCs.

The reduced number of components in the inverter not only improves its reliability but also reduces the stored energy, resulting in a smaller size and weight, as well as lower overall costs. In addition, the simplified structure simplifies wiring and maintenance and improves electromagnetic interference (EMI) performance. This reduces the number of voltage sensors and gate drivers, contributing to a reduction in cost, complexity, and device stress.

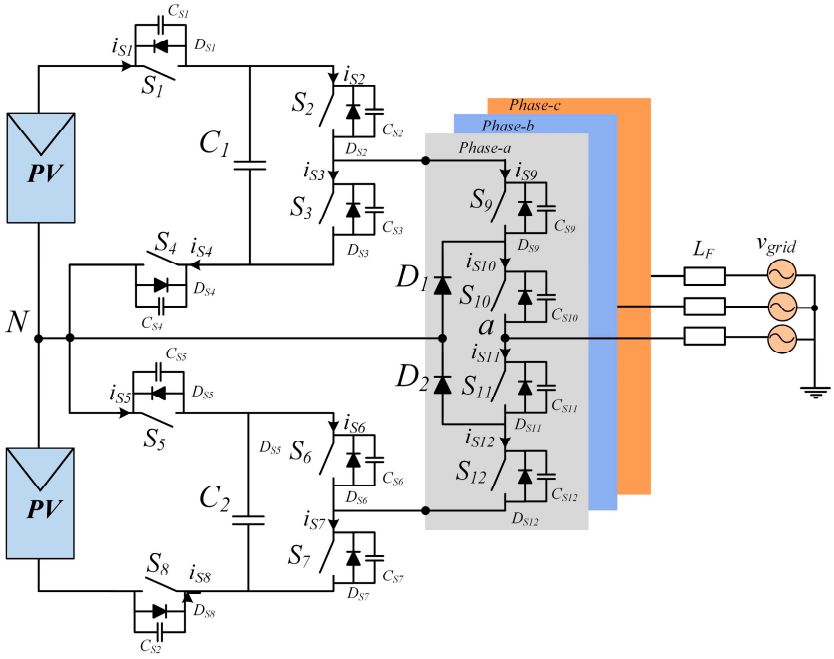

Figure 27. RCC TMLI.

Control Approaches of Dual-Input RC-TMLI Topologies

Modular RC-TMLI

The control method for the proposed dual-input topology [117] comprises two switching states for the cascade configuration of the half-bridge converter. The first stage involves the lower switch being in OFF state, during which the upper switch conducts, and the second stage involves the activation of the lower switch with the upper switch OFF. For this cascaded configuration, the carrier-cascaded pulse-width modulation scheme is implemented in order to ensure the control of the terminal voltage. In the deployment of the carrier cascaded PWM strategy, one half-bridge section is operational during the switching state, while the other state remains unchanged. This is performed in order to keep the power losses to a minimum. For this topology, a modified version of the cascaded PWM is used for effective converter control and equalization of voltage. The balance of the terminal voltage is realized through the carrier signal. To maintain continuity in the reference voltage, only one half-bridge at a time is made to change the switching state. Following this pattern, in a cascaded cell configuration, multiple half-bridges can be operated in either the switch's ON or OFF state to generate a staircase voltage waveform at the output. This scheme is also optimal in terms of fault control, where a half-bridge can just be bypassed without influencing the other cells, in case of cell damage.

RCC TMLI

Though the modulation of a three-phase inverter is usually carried out in a per-phase manner, with a reference for each phase, for the proposed topology [125], the minimum, maximum and middle reference values are considered, since this configuration incorporates a combination of FC cells. The modulation of upper and lower FC cells is performed by the maximum and minimum reference values V_{max} and V_{min}. This provided the maximum and minimum inverter voltages at the output. The time average for the middle phase in the NPC section is determined between the midpoint as well as maximum and minimum values, which in turn leads to a complete three-phase waveform.

Table 3 provides a summary of the control approaches implemented for the dual-input RC-TMLI topologies.

Table 3. Control approaches of dual-input RC-TMLI topologies.

Control Approaches	
Modular RC-TMLI	**RCC TMLI**
[117] Level-shift PWM	[125] Multilevel PWM with voltage control

3. Comparative Analysis

An extensive comparative analysis of both the physical as well as performance parameters was conducted for the conventional and hybrid transformerless topologies of the multilevel inverters.

3.1. Analysis of Physical Parameters

The NPC, FC, CHB, and ANPC topologies are among the most common single- and three-phase multilevel inverter topologies. High step-up TMLI, FCHT-type inverter, DSCC HBC type, hybrid ANPC-LVS inverter, and Boost ANPC inverter are examples of single-phase hybrid inverter topologies with reduced component counts, as mentioned in Table 4. Three-phase two-Leg TMLI, modular TMLI, RCC TMLI, hybrid nine-Level, and hybrid 13-Level inverters are hybrid topologies with smaller numbers of components in three-phase systems, as illustrated in Table 4.

Here, 'n' denotes the total number of voltage levels in the inverter. A single DC source is used in the NPC, ANPC, and FC for both single- and three-phase systems. The number of DC sources in the CHB is calculated as $(n-1)/2$ for single-phase systems and $3(n-1)/2$ for three-phase systems, as shown in Table 4 respectively.

The total number of switches in the NPC, FC, and CHB inverters for single-phase operation is $2(n-1)$, whereas for three-phase operation, it is $6(n-1)$. Similarly, the number of switches for a single-phase ANPC inverter is $2[2(n-1)+2(n-1)]$ and $3[2(n-1)+2(n-1)+2(n-1)]$ for three-phase configurations.

The number of clamping diodes in the NPC inverters is computed as $(n-1)(n-2)$ for single-phase configurations and $3(n-1)(n-2)$ for three-phase configurations. For single-phase FC inverters, the number of flying capacitors is $(n-1)(n-2)/2$, whereas for three-phase configurations, it is $(3/2)(n-1)(n-2)$.

The number of DC bus capacitors in the NPC, FC, and ANPC inverters for single- and three-phase systems can be determined as $(n-1)$.

These calculations are carried out for both 5-level and 11-level single-phase inverters, and the results are compared to hybrid topologies, as shown in Table 1. Similarly, three-phase topologies are calculated using 3-level and 13-level configurations, and their component counts are compared to hybrid topologies, as shown in Table 4. Each type of TMLI has distinct benefits and drawbacks. NPC has high voltage capabilities, no FCs, a simple design, and is compact in a three-level structure but it requires complex control and reduced reliability as the number of levels increase due to a dramatic increase in the number of diodes. Cascaded inverters offer high reliability owing to their modular structure and fewer harmonics; however, they require separate isolated DC sources and additional components. FC inverters feature fewer active components and lower losses than NPC inverters; however, they require a large number of FCs and have capacitor voltage balancing issues, restricted voltage handling, and low reliability. The ANPC also does not require FCs for a three-level structure, but the number of FCs increases with an increase in several voltage levels and potentially greater expenses for additional switches. In comparison to the hybrid topologies listed in Table 4, these traditional inverters require a significant number of components for a higher number of voltage levels. Table 4 illustrates that hybrid topologies have a significantly smaller number of components than traditional topologies.

Table 4. Comparison of physical parameters of single-phase multilevel inverter topologies. **NPC**: neutral point clamped, **FC**: flying capacitor, **CHB**: cascaded H -bridge, **ANPC**: active neutral point clamped, **RC-TMLI**: reduced component transformerless multilevel inverter.

Comparison of Physical Parameters of Single-Phase Multilevel Inverter Topologies													
	Traditional Topologies								**Hybrid Topologies**				
	NPC		**FC**		**CHB**		**ANPC**		**Three-Phase 2-Leg RC-TMLI**	**Modular RC-TMLI**	**RCC**	**Hybrid 9-Level**	**Hybrid 13-Level**
	[101,130–133]		[38,39,133]		[49,133–136]		[137–139]		[140]	[141]	[142]	[143]	[144]
Number of levels	3	13	3	13	3	13	3	13	3	3	5	9	13
Number of DC sources	1	1	1	1	3	18	1	1	1	2	2	3	1
Number of switches	12	72	12	72	12	72	18	468	8	12	20	36	30
Number of gate drivers	12	72	12	72	12	72	18	468	8	12	20	36	27
Number of diodes	6	396	-	-	-	-	-	-	4	-	6	-	-
Number of capacitors	-	-	3	198	-	-	-	-	-	-	2	6	6
Dc bus capacitors	2	12	2	12	-	-	2	12	2	-	-	6	2
Comparison of physical parameters of three-phase multilevel inverter topologies													
	Traditional Topologies								**Hybrid Topologies**				
	NPC		**FC**		**CHB**		**ANPC**		**Three-Phase 2-Leg RC-TMLI**	**Modular RC-TMLI**	**RCC**	**Hybrid 9-Level**	**Hybrid 13-Level**
	[101,130–133]		[38,39,133]		[49,133–136]		[137–139]		[140]	[141]	[142]	[143]	[144]
Number of levels	3	13	3	13	3	13	3	13	3	3	5	9	13
Number of DC sources	1	1	1	1	3	18	1	1	1	2	2	3	1
Number of switches	12	72	12	72	12	72	18	468	8	12	20	36	30
Number of gate drivers	12	72	12	72	12	72	18	468	8	12	20	36	27
Number of diodes	6	396	-	-	-	-	-	-	4	-	6	-	-
Number of capacitors	-	-	3	198	-	-	-	-	-	-	2	6	6
Dc bus capacitors	2	12	2	12	-	-	2	12	2	-	-	6	2

3.2. Analysis of Performance Parameters

Considering the hybrid topologies presented and reviewed in this paper, an analysis is presented on the performance factors. The factors that can be assessed include overall efficiency, hardware cost, modulation complexity, voltage stress and leakage current. These factors hold significant importance as they determine the operational outcome of each topology. Table 5 illustrates the comparative analysis of all the topologies based on these performance factors.

Considering the review of single-phase hybrid configuration of the TMLIs presented, with six switching states in each half cycle and a total of 12 modes, the high-step-up RC TMLI topology does present a complexity in modulation despite its operation through a single DC source and being efficient in terms of voltage stress as it incorporates comparatively few diodes as compared to other five-level inverters. In comparison, with the FCHB type RC TMLI topology, the overall efficiency is improved due to a reduction in voltage stress due to it having fewer diodes. Moreover, with the incorporation of fewer switches, as well as the deployment of only one FC bridge, the cost is reduced as well. The modulation algorithm is also simplified for the case of the ANPC-LVS TMLI topology along with using fewer power devices, thus bringing about a reduction in voltage stress. A high rating level for voltage can be achieved with the Boost ANPC TMLI.

Analyzing the three-phase hybrid topologies for the TMLI on the same factors previously mentioned, it can be concluded that for the three-phase three-level two-leg RC TMLI, a significant reduction in volume and cost is obtained, as it makes use of the conventional NPC infrastructure. For the case of modular as well as RCC TMLI configurations, although the infrastructure employ dual-PV sources, they also provide the benefits of increased

efficiency, cost effectiveness, and low size and weight. The 13-level hybrid TMLI provides features of increased output through single DC source, low-order harmonics, and grid suitability. Modular and switched capacitor TMLIs both provide a significant reduction in cost due to a reduction in power devices. For the self-balanced configuration of the switched capacitor TMLI, despite an overall boost in the output voltage, the increased number of switches and diodes leads to losses in the system. The recently proposed three-phase TMLI topology employs a conventional NPC operating at fundamental frequency, making overall losses negligible. Moreover, the elimination of the transformer and DC capacitor bus gives a reduction in leakage current and overall cost.

Table 5. Comparison of performance parameters of multilevel inverter topologies.

Comparison of Performance Parameters of Single-Phase Multilevel Inverter Topologies								
	Traditional Topologies			**Hybrid Topologies**				
	NPC	**FC**	**CHB**	**High Step-Up RC-TMLI**	**FCHB-Type RC-TMLI**	**DSCC HBC RC-TMLI**	**Hybrid ANPC**	**Boost ANPC**
	[101,130–133]	[38,39,133]	[49,133–136]	[137–139]	[140]	[141]	[142]	[143]
Voltage Stress	50%	50%	25–33%	Low	Low	Low	Low	Low
Leakage Current	100 mA	150 mA	50 mA	Low	Low	Low	Low	Low
Efficiency	97%	96%	98%	96%	98.9%	94.18%	97.33%	96%
Hardware cost	1.2–1.5x	1.6x	1.5–2x	Low	Low	Low	Low	High
THD	2–4%	2–4%	1–3%	40.48%	6%	3.13%	13.16%	2–5%
Modulation complexity	High	Low	Lowest	High	Low	Low	Low	Low
Comparison of Performance Parameters of Three-Phase Multilevel Inverter Topologies								
	Traditional Topologies			**Hybrid Topologies**				
	NPC	**FC**	**CHB**	**3-Phase 2-Leg RC-TMLI**	**9 Level RC-TMLI**	**13 Level RC-TMLI**	**Modular RC-TMLI**	**SC RC-TMLI**
	[101,130–133]	[38,39,133]	[49,133–136,138–142]	[90,137–139,143,144]	[111,140]	[141,145]	[125,142]	[116,143]
Voltage Stress	50%	50%	33%	Low	Low	Low	Low	Low
Leakage Current	600 mA	750 mA	450 mA	Low	Low	Low	Low	Low
Efficiency	98%	97%	99%	95–97%	96–98%	97–99%	98–99%	96–98%
Hardware cost	1.5x	1.7x	1.6–2x	Low	Low	Low	Low	Low
THD	1.5–3%	1.5–3%	1–2.5%	1%	5.06%	7.15%	7.13%	1%
Modulation complexity	High	Low	Lowest	Low	Low	Low	Low	High

4. Conclusions

This study highlights the increasing importance of transformerless multilevel inverters for solar power integration in medium- and high-power applications. These inverters have gained popularity due to their ability to produce high-quality waveforms while maintaining low voltage stress across active components and minimizing the THD in the output voltage. However, achieving these benefits requires the use of a large number of active and passive components, which results in increased size and weight. This study focuses on two main goals. First, a detailed overview of traditional transformerless multilevel inverters (TMLIs) with single- and three-phase topologies is given, providing a foundational understanding of these systems. This is followed by the investigation of hybrid TMLI topologies designed for photovoltaic applications with a small number of components.

Based on the physical parameters of traditional inverters, while NPC provides simplicity in design, it requires complex control. Cascaded inverters with their high reliability also involve a certain level of complexity in design owing to additional components and isolated DC sources. For the ANPC, the number of FCs need to be increased for each increase in voltage level, thereby increasing component count. As compared to these traditional inverters, the hybrid topologies provide a considerable reduction in components, with

the three-phase two-leg RC TMLI making use of the fewest components and only one DC source.

Considering the performance factors, the single-phase FCHB-type RC TMLI using fewer diodes and switches along with one FC bridge leads to a significant reduction in overall cost and voltage stress. When assessing the three-phase hybrid TMLI topologies, the hybrid 9-level and 13-level RC TMLI topologies, as well as the modular RC TMLI, stand out as being high in efficiency while also providing a reduction in modulation complexity, hardware cost owing to the reduced number of components, leakage current, and voltage stress, respectively, making them a good choice for photovoltaic installations. The SC RC TMLI, on the other hand, while providing a reduction in voltage stress and leakage current, also involves a complex modulation scheme.

This study provides researchers with valuable insights into the field of multilevel inverters by comparing traditional and hybrid single-/three-phase topologies in terms of physical as well as performance parameters. The most relevant features of all the photovoltaic inverter topologies reviewed in this state of the art have been extracted and organized into tables to facilitate researchers and engineers in selecting the most suitable one for specific applications.

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