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A New TDU-Based Hierarchical Beamforming Framework to Suppress Grating Lobes and Save Space

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ABSTRACT: This paper introduces a new hierarchical beamforming network (HBFN) design methodology that introduces a new degree of freedom in the time delay unit (TDU) allocation across beamforming layers. By varying the TDU delay range within a single layer instead of using a uniform delay profile, this method reduces quantization error magnitudes, significantly suppresses grating lobes and optimizes physical space utilization. This approach alters the statistical structure of quantization errors, leading to an 11.2 dB reduction in grating lobes for a 16×16 planar array in full-wave EM simulation. Additionally, a large-scale 256×256 array model demonstrates an 18.0 dB grating lobe suppression and a space saving of up to 29.9%, confirming the scalability of the approach. The reduced space requirement of TDUs enables improved mobility, supporting the transition to flat panel arrays and making it well-suited for radar, satellite and mmWave communication systems. This paper presents a rigorous analytical framework, full-wave electromagnetic validation and a discussion of the practical impact of these findings in phased array design.

INDEX TERMS. Broadband antennas, grating lobes, hierarchical beamforming, phased arrays, quantization effects, time delay units.

I. INTRODUCTION

Phased array antennas have become a cornerstone of modern radar, satellite communication and 5G cellular networks due to their ability to electronically steer beams, enable adaptive nulling and support multiple simultaneous beams [1]. However widespread adoption of large aperture phased arrays is limited by the cost, size, weight and complexity of fully populated arrays with independently controlled elements.

These challenges have driven extensive research into architectures that reduce the burden of independent element control while maintaining system performance; methods such as tile vs slat designs [2], and modularization with subarrays [3], [4], [5].

Other methods of reducing the size and complexity of phased arrays include irregular architectures such as thinned arrays, sparse and time-modulated arrays [6], [7], [8].

The use of parasitic elements instead of active elements has also been proposed to reduce complexity and cost [9] along with randomly feeding multiple antenna elements from a single phase shifter [10].

This paper focuses on the beamforming network (BFN) within wideband phased arrays and proposes a novel design method that significantly reduces BFN size without compromising performance.

To operate over a truly wide frequency band, phased antenna arrays require time delay units (TDUs) to prevent beam squint and signal dispersion. Such arrays are sometimes called timed arrays [11]. TDUs can be more expensive than phase shifters and take up more space as they are required to provide significant delay values. The maximum delay is determined by the size of the array, the bandwidth, and the maximum scan angle [12]. For example, a square array 50-wavelength wide requires a TDU of approximately 60 wavelengths to achieve a 60° scan in all directions.

TDUs are often implemented by switching transmission lines of varying length in and out of the transmission path. The number of delay values is controlled by the choice of the number of control bits per TDU, as illustrated in Fig. 1.

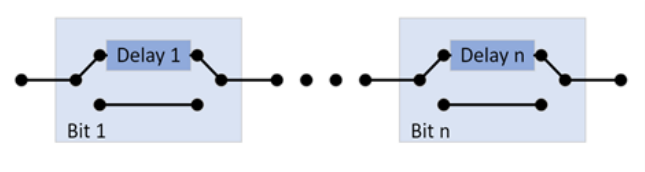

FIGURE 1. Layout of typical TDU with n-bit control.

Large delay values can become a physical challenge requiring significant real estate to implement. Hence researchers have proposed hierarchical structures to enhance design efficiencies and to reduce the number and size of TDUs required for a beamforming network [13], [14]. A typical hierarchical TDU-based BFN is illustrated in Fig. 2.

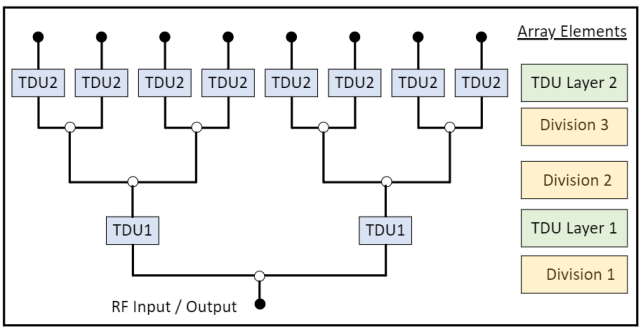

FIGURE 2. Hierarchical beamforming network showing divisions and layers.

Prior studies have considered the optimum design configuration for the number and location of the TDUs and the associated number of the control bits, based on a set of selection criteria [15], such as the number of TDUs and the tolerable phase error. The researchers used integer linear programming (ILP) to run all possible combinations and weighted the results to determine an optimum configuration.

This paper builds upon those approaches by introducing a new degree of freedom: the ability to vary the TDU delay range within a single BFN layer. As far as the authors know, the open literature to date has only considered uniform TDU values in a single layer.

This variation offers two key benefits. First, it can save the size required to build the BFN as some TDUs reduce in value and hence size. Secondly, the phase errors can reduce and become less structured with less of a regular pattern thus reducing pointing errors and sidelobe levels.

We quantify these benefits by applying the proposed method to the ILP-derived uniform baseline configurations from [15]. The proposed shaping, or profiling, of TDU values is applicable for linear and rectangular planar arrays and is scalable in size.

A design methodology is presented to generate tailored TDU profiles that minimize delay range per element and promote smaller, more concentrated quantization errors. This approach contributes to the state of the art in three key ways:

- **Physical space reduction** – Varying the delay values of TDUs reduces the physical footprint of the beamforming network, an aspect not addressed in prior work.
- **Phase error reduction** – The approach lowers array phase errors, improving sidelobe and grating lobe performance.
- **Scalability** – The method applies to both linear and planar arrays and scales effectively across different sizes and configurations.

To validate the proposed approach, numerical simulations and full-wave electromagnetic (EM) modelling are conducted on planar arrays. A 16 × 16 planar array simulation at 30 GHz demonstrates a grating lobe reduction of up to 11.2 dB with a size reduction of 10.1%, while a numerical model of a 256 × 256 array exhibits an 18.0 dB sidelobe reduction and a 11.2% space saving. Additionally, the methodology is applied to a 128-element linear array, where the RMS phase error is reduced from 3.83° to 3.3°. More significantly, the proposed method enables alternative, more compact solutions that maintain equivalent performance while achieving space savings of 21% for the 128-element linear array and 29.9% for the 256x256 planar array.

These architectural improvements translate into practical deployment advantages. By reducing the physical size of the TDUs, it enables more compact and mobile phased arrays, reducing weight, lowering manufacturing costs and supporting the next generation of flat panel arrays. These benefits make it particularly well-suited for applications in aerospace, satellite communications and mobile radar platforms where physical volume and weight are critical constraints.

The remainder of this paper is organized as follows: Section II develops the theoretical framework for hierarchical TDUs with variable delay ranges and presents numerical simulations and quantifies performance improvements.

Section III validates the approach using full-wave EM simulations.

Section IV discusses practical implementation considerations and outlines directions for future work.

Section V concludes with key takeaways.

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II. THEORY

A significant benefit of using a hierarchical BFN design is the saving in real estate and the number of control bits required. For example, considering a 256 x 256 antenna array, the optimum BFN design across 3 layers saves 96% of the real estate and requires only half the number of control lines compared to a flat BFN design using a single layer of TDUs with uniform values per element.

However, the lower layer TDUs of a hierarchical BFN are feeding widely spaced subarrays which introduces the risk of grating lobes.

In existing hierarchical TDU-based BFN designs, TDU values in each layer are generally the same, i.e. they are uniform in value. This, however, fails to capture the fact that the TDUs in the center of an array do not need the full delay range of those TDUs at the edges. We propose leveraging this practical insight by tailoring the TDU delay range within each layer to further enhance BFN performance. For a uniform linear or planar array, it is the TDUs at the edges that must swing from maximum to minimum delay whereas those in the middle need only swing around half the delay range. In this paper, we consider reducing the least significant bit (LSB) of center TDUs, while maintaining constant bit depth across the layer, to lower the quantization resolution where full range is unnecessary. There is also the option to reduce the number of control bits for the central TDUs, which can be readily extended based on the design here.

This profile-based approach reduces the number of large quantization errors and increases the number of small ones, thereby reshaping the distribution of errors across the array in a beneficial way**.** This logic is consistent with our observations in Section I and will be quantitatively developed throughout the following analysis.

Notation Consistency

Variables that vary across the antenna elements are expressed as functions of p, x and y (e.g., $r_n(p)$, $LSB_n(x,y)$), while layer indices n are treated as fixed parameters and indicated by subscripts. This convention distinguishes element-specific quantities from layer-specific parameters and is used consistently in both linear and planar array formulations.

A. Linear Array.

We begin by considering every possible design variant of a hierarchical BFN for a linear array.

Given a linear array with M elements, where M is a power of 2, the number of division levels D is:

$$D = \log_2 M \tag{1}$$

Note that division level 1 is at the lowest level, furthest from the antenna radiating elements.

Let L denote the number of layers of TDUs. Each TDU layer may be placed on any division level from 1 to D and multiple layers may reside on different or the same levels, depending on the design requirements.

We denote the actual division level where there is a layer of TDUs as d_n where n is the number of the TDU layer and d_n is equal to the division level that incorporates the TDU layer of number n. (For example, $d_2 = 4$ means that the second layer of TDUs in on the 4th division level.)

Next, we calculate the scanning details for each layer of TDUs by calculating the size of each corresponding subarray, M_n. This is the number of array elements fed from the group of TDUs on layer n, fed from a single TDU on the layer n-1.

$$\begin{aligned} M_1 &= M \\ M_n &= \frac{M}{2^{d_{n-1}}}, \qquad \forall n \in \{2,....,L\} \end{aligned} \tag{2}$$

The size of each subarray, in wavelengths is given by h_n;

$$\begin{aligned} h_1 &= M_1 e_p \left(1 - \frac{1}{2^{d_1}}\right) \\ h_n &= M_n e_p \left(1 - \frac{1}{2^{(d_n - d_{n-1})}}\right), \qquad \forall n \in \{2,....,L\} \end{aligned} \tag{3}$$

where e_p denotes the separation, or pitch, of antenna elements in wavelengths.

Considering the maximum scan angle $\theta_{\max}$, the scan distance for each subarray is given by,

$$h_n^{scan} = h_n \sin\theta_{\max} \tag{4}$$

From this, we calculate the maximum delay $T^{\max}$ required at each TDU layer as the sum of any error from the TDU layer below, due to quantization, plus the value necessary to achieve the scan required of the subarrays fed from that layer of TDUs.

$$\begin{aligned} T_1^{\max} &= \frac{h_1^{scan}}{c} \\ T_n^{\max} &= \frac{h_n^{scan}}{c} + T_{n-1}^{qe}, \qquad \forall n \in \{2,....,L\} \end{aligned} \tag{5}$$

where T^{qe} is the quantization error.

The maximum LSB value of each TDU is simply the maximum delay divided by the number of bits controlling that TDU, i.e.

$$LSB_n^{\max} = \frac{T_n^{\max}}{2^{b_n} - 1}, \qquad \forall n \in \{1,....,L\} \tag{6}$$

Let b_n be the number of control bits for layer n.

The delay error from the TDU below can be calculated as half the value of the LSB of that layer.

The quantization error values are:

$$T_n^{qe} = \frac{LSB_n}{2}, \qquad \forall n \in \{1,....,L\} \tag{7}$$

This quantization error accumulates through the hierarchy and plays a direct role in the final phase accuracy at the antenna elements.

B. TDU range profile across a layer

The calculation of the TDU delay values for each layer depends on the number of subarray elements formed by the TDUs at that layer and the number of array elements fed from a single TDU. Symmetry exists both within each subarray and across the complete array, since the array must steer symmetrically in both directions.

If each antenna element is indexed by p, a modified index p' is introduced to account for the subarray structure and to enforce symmetry about the center of the array.

For each layer $\forall n \in \{1,....,L\}$, the delay profile is defined over subarrays of size M_n. The value of p'_n is computed as follows.

Let the local index r_n of antenna element p within its layer n subarray be:

$$r_n(p) = (p-1) \bmod M_n, \quad \forall p \in \{1,....,M\} \tag{8}$$

where $(.) \bmod$ is modular arithmetic.

The subarray resolution factor f_n is defined as:

$$f_n(p) = \lfloor r_n \cdot 2^{d_n - D} \rfloor, \quad \forall p \in \{1,....,M\} \tag{9}$$

The floor function $\lfloor . \rfloor$ rounds a number to the nearest integer towards negative infinity.

Then the center-reflected subarray index p'_n is:

$$p'_n(p) = \max\left(f_n, 2^{d_n - d_{n-1}} - 1 - f_n\right), \quad \forall p \in \{1,....,M\} \tag{10}$$

Note that $d_0 = 0$. For implementation or visualization purposes, these expressions can alternatively be simplified by calculating the top half of the array and applying mirror symmetry.

Within each subarray, the TDU delay values decrease toward the center. The step size, Δ, for each layer is calculated as:

$$\begin{aligned} \Delta_1 &= \frac{h_1^{scan}}{c \cdot \left(2^{d_1} - 1\right)} \\ \Delta_n &= \frac{\Delta_{n-1}}{2^{d_n - d_{n-1}}} \quad , \; n \in \{2,....,L\} \end{aligned} \tag{11}$$

Combining the step size with p', the LSB value at each element $\forall p \in \{1,....,M\}$ for each layer $\forall n \in \{1,....,L\}$ are given recursively:

$$\begin{aligned} LSB_1(p) &= \frac{\Delta_1 \cdot p'_1}{2^{b_1} - 1}, \qquad for \; n = 1 \\ LSB_n(p) &= \frac{\frac{1}{2} \cdot LSB_{n-1}(p) + \Delta_n \cdot p'_n}{2^{b_n} - 1}, \; \forall n \in \{2,....,L\} \end{aligned} \tag{12}$$

Introducing a delay profile within a layer reduces the maximum quantization error at each TDU by lowering the LSB value toward the center. Consequently, the next layer up in the BFN requires a smaller delay range, as it must only compensate for the reduced residual error passed up from the previous layer. This compression effect accumulates through the hierarchy, enabling space and error reductions.

It should be noted that this profiling opportunity exists only if the subarray contains at least four TDUs. When only two TDUs are present in a subarray, there is no scope for variation in the center delay values. Therefore, a minimum of two division levels is required between adjacent TDU layers to enable profiling.

The value of the most significant bit (MSB) for each TDU is calculated as:

$$\begin{aligned} &MSB_n^p = \frac{2^{b_n}}{2} LSB_n^p, \\ &\forall p \in \{1,....,M\} \quad and \quad \forall n \in \{1,....,L\} \end{aligned} \tag{13}$$

And the total TDU delay value for every TDU is

$$\begin{aligned} &TDU_n^p = LSB_n^p \left(2^{b_n} - 1\right), \\ &\forall p \in \{1,....,M\} \quad and \quad \forall n \in \{1,....,L\} \end{aligned} \tag{14}$$

Using the established formulae for the LSB delay values at each array element p in layer n, we can determine both the number of TDUs required in the layer and their corresponding delay values.

There are 2^{d_n} TDUs in layer n.

Inspection of the LSB values reveals the delay range required across the layer.

As an example of the methodology, we consider the design shown in Fig. 3, which corresponds to variant 7390 from [15], identified as the optimal solution for a 128-element linear array at 30 GHz. The caption of Fig. 3 shows the TDU delay values and control bits for the linear array with an element pitch of $\lambda / 2$ for a maximum scan angle of +/- 60° from boresight.

A ±60° scan angle is commonly used in array antenna studies as it represents a challenging yet realistic test of array performance.

Fig. 4 is a graph of the total delay value for each TDU on each of the 3 layers. On layer 1, there are 2 TDUs (i.e. 2^{d_1}) and because of the small count, there is no opportunity to apply profiling, each must provide the full required delay range. The graph for layer 2 (red) shows the step down in maximum delay value from 1020 ps to a minimum of 673.6 ps for the 32 TDUs on layer 2, division 5. Each TDU on layer 1 feeds 16 (i.e. $2^{d_2 - d_1}$) TDUs on layer 2 and 64 (i.e. $2^{D - d_1}$) array elements.

The step down in value for each layer 2 TDU is calculated to achieve the maximum delay value required for the subarray of 64 array elements to be able to achieve the delay for the maximum scan angle.

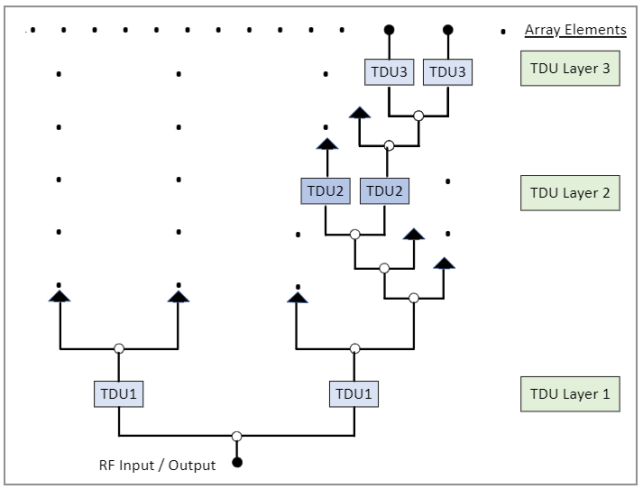

FIGURE 3. 128-linear array design, TDU1 has 2 bits and LSB = 307.9 ps, TDU2 has 4 bits and LSB = 68 ps and TDU3 has 6 bits and LSB = 1.2 ps.

At each higher layer this same profiling approach is extended to calculate the maximum TDU delay value required across the subarray.

In this example there are 8 unique values on layer 2 and 16 unique values on layer 3. Since most of the performance benefit arises from the lower layers, a full set of unique values at the highest layer may not always be necessary in practical implementations.

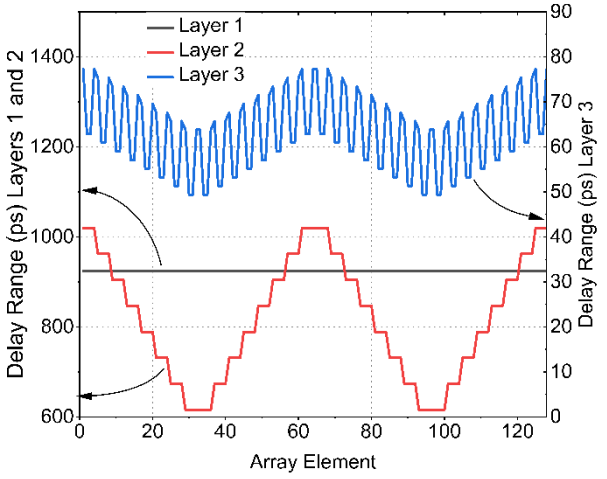

FIGURE 4. Graph of the TDU values on each of layers 1, 2 and 3 along the full length of the 128-element linear array with the design shown in Fig. 3.

Varying the LSB delay values, as described here, reduces both the RMS phase error along the array and the physical area required to implement the TDUs.

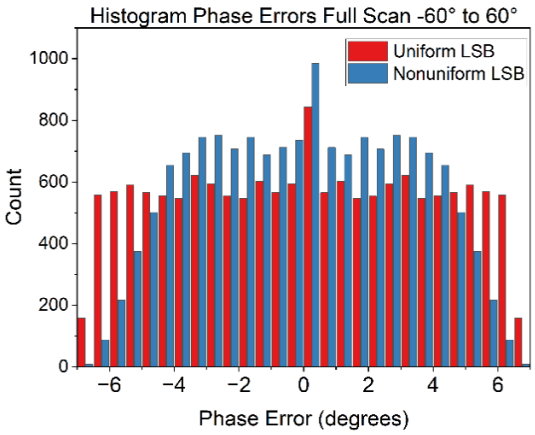

FIGURE 5. Combined histograms for the element phase errors for the 128-element linear array with the nonuniform TDUs and uniform TDUs for a full scan from -60° to 60°, showing many more smaller errors and fewer large errors for the nonuniform TDUs as compared with uniform TDUs.

This effect is illustrated in Fig. 5, which shows the phase error occurrences for a full scan of the linear array from -60° to 60°. The uniform TDU case exhibits an even spread of phase error values, while the nonuniform case produces a distribution with many small errors and fewer large deviations. This shift improves RMS phase error and results in better beamforming performance.

To calculate the resulting array phase error, we note that it is governed entirely by the final layer of TDUs that provides the final correction after cumulative delays from earlier layers. The accuracy of this adjustment determines the deviation from the ideal delay at each antenna element and thus the resulting phase error. Assuming each element's delay error is uniformly distributed within ±½ LSB, the RMS error is equal to the standard deviation (σ) of the error, as the mean is zero and has been given by Mailloux [1] as,

$$\sigma = \frac{LSB}{2\sqrt{3}} \tag{15}$$

Now that we have varied the LSB values of the TDUs, there is a range of LSB value errors. In principle, the overall variance could be calculated by a weighted sum of individual TDU variances, but this is unnecessarily complex. Because the LSB profile across the array is nearly linear, the square of the delay errors also varies slowly and approximately linearly.

This justifies using the arithmetic mean of LSB values as a direct estimate for RMS phase error, with negligible loss in accuracy (<0.0003%).

Hence, we calculate the average TDU delay value by taking the midpoint between the delay at the edge and the delay at the minimum of the LSB range. This average value is then used in (15) to estimate the resulting phase error.

To estimate a TDU footprint, we adopt the method proposed in [12], which compares the area required for uniform versus varying delays. The method assumes TDUs

are implemented on a PCB and occupy square unit cells of area a x a. The researchers proposed a scheme of a single length of line, equal to the delay required by the MSB which occupies no more than half the unit area, leaving space for shorter delay lines.

If we assume a PCB relative permittivity of 2, then 10 mm of line equals about 47 ps of delay. Working at 30 GHz, this equates to a unit cell of 3.5 mm x 3.5 mm, being half a wavelength, allowing for an MSB line length of 10.5mm, equal to approximately 50 ps delay, such that the whole cell delivers a maximum delay of twice the MSB delay, giving a TDU of 100 ps delay in an area of 12.25 mm^2. This ratio is used consistently for all real estate calculations.

Since the schematic structure is unchanged, space savings arise solely from the reduced delay range requirements per TDU, particularly in lower layers.

Putting this all together, the application of the proposed method to the baseline 128-element linear array design (variant 7390, as per Fig. 3.) results in a 13.3% reduction in TDU footprint and a 13.7% improvement in RMS phase error, decreasing from 3.84° to 3.31°. This phase error reduction incurs no performance penalty and demonstrates a measurable gain in sidelobe suppression alongside significant space savings. Fig. 6 shows the beam pattern for a –60° scan, comparing the case with and without the TDU delay profile. The overall array pattern remains largely unchanged, with no detrimental effects introduced, and the proposed method improves the response by a few decibels in certain regions. In particular, it suppresses a grating lobe near 30°, which corresponds to one of the grating lobes introduced by the periodic subarray structure formed by the first TDU layer. In this case, the array is divided into four 32-element subarrays spaced 16λ apart, resulting in the formation of 32 grating lobes. In a perfect array, these grating lobes would be perfectly cancelled due to the nulls in the array and subarray array factors. However, the partial visibility of the grating lobe at 30° arises from the degradation of these ideal nulls by quantization errors. Although reduced in amplitude, the angular position and frequency-aligned behavior support its classification as a suppressed grating lobe rather than a conventional sidelobe.

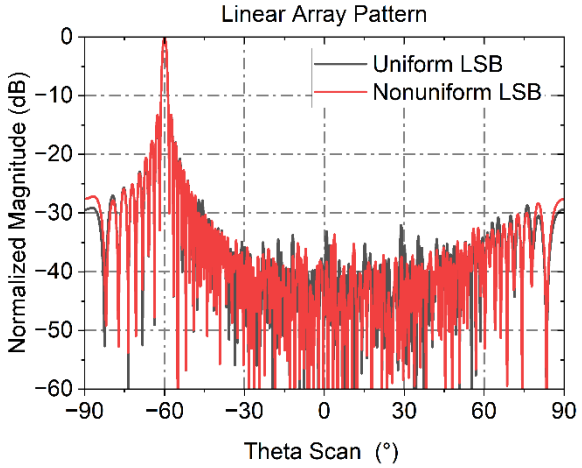

FIGURE 6. Array pattern for a 128-element linear array with constant TDU LSB values in a layer and varying TDU LSB values.

More importantly, introducing nonuniform TDU values changes the ILP-optimal solution itself. A revised configuration using 2, 6 and 5 bits on layers 1, 5 and 7, respectively meets the same phase error target with a 21% footprint reduction. This result shows that the proposed methodology both improves existing designs and enables new, more compact solutions that meet the same performance objectives.

All performance comparisons in this work use unity input amplitudes at each element, with no amplitude tapering or transmission line loss included. The observed improvements in sidelobe and grating lobe suppression are entirely attributable to the phase structure introduced by nonuniform TDU delays.

C. Planar Array

The core principles applied to linear arrays extend naturally to two-dimensional planar arrays. In such arrays, TDUs near the center require less delay than those at the periphery and this now holds in both the horizontal and vertical directions. As a result, the maximum delay values occur along all four edges of the array, decreasing progressively toward the center. This creates a bowl-shaped TDU delay distribution, sometimes multiple adjoining bowls, depending on the number and placement of TDU layers across division levels.

In a 2D planar array, each division level subdivides the array by a factor of 4, unlike the binary division applied in linear arrays. If the total number of M is a power of 4, the number of division levels is given by:

$$D = \log_4 M \tag{16}$$

The size of each subarray in wavelengths is derived from the linear array case but scaled appropriately to account for the maximum distance occurring along the diagonal of the square array elements;

$$\begin{aligned} h_1 &= M_1 e_p \sqrt{2}\left(1 - \frac{1}{d_1}\right) \\ h_n &= M_n e_p \sqrt{2}\left(1 - \frac{1}{2^{(d_n - d_{n-1})}}\right), \qquad \forall n \in \{2, \ldots, L\} \end{aligned} \tag{17}$$

To compute the maximum delay required on each TDU layer, each array element is indexed by its position (x, y) in a Cartesian coordinate system, where x and y are integer values representing the column and row numbers, respectively. Here both x and y are in the range $\forall x, y \in \{1, \ldots, 2^D\}$.

The TDU delay profiles for each element on each layer are computed by treating each array element as the intersection of a row and a column linear array. For an element at (x, y) the

required delay is calculated from its position in both the row and the column and assigned the maximum of the two as the TDU delay for that position.

Using (8) - (12), the LSB values for the row and column linear arrays are calculated separately, substituting x and y for p and the planar TDU LSB value is given by:

$$LSB_n(x,y) = \max\left(LSB_n(x), LSB_n(y)\right) \quad \forall x, y \in \{1,....,2^D\}, \quad \forall n \in \{1,....,L\} \tag{18}$$

The MSB values and total TDU delay values for the planar array elements are determined using the same method described in (13) and (14).

As an example, consider a 256 x 256 array, with L=3, $\theta_{\max} = 60^o$ scanned across all azimuth directions. The array operates at 30 GHz with $\lambda/2$ element pitch.

Applying the integer linear programming method from [15] yields an optimal baseline configuration with TDUs on division levels 2, 6 and 8, and control bit depths of 2, 5 and 6, respectively. Applying the proposed nonuniform TDU profile to this baseline yields an 11.2% reduction in TDU footprint and a 6.5% improvement in RMS phase error.

More significantly, introducing nonuniform TDU values expands the design space, yielding 24 new candidate configurations that meet all design constraints. One such configuration, with TDUs on levels 4, 6 and 8 and bit depths of 3, 3 and 6, achieves a 29.9% reduction in space, a slight improvement in average sidelobe level (from –47.36 dB to –47.72 dB) and a 1.8% reduction in control lines, with only a 0.25% increase in the number of TDUs.

These results highlight that nonuniform TDU profiles not only reduce spatial and phase error overhead in existing designs, but also enable new, more compact solutions with improved sidelobe performance.

Because the top layer's LSB profile depends on both the profiles and control bit allocations of all underlying layers, it is not trivial to express the final phase error with a simple analytical formula. Instead, we calculate it exactly for each design variant of interest, of which only a small number are relevant.

To illustrate the complexity of a typical TDU delay profile in a large array, Fig. 7 shows the maximum delay values of the TDUs on layer 2 for row 145 in the 256×256 planar array. The profile is neither linear nor uniformly stepped; rather, it varies nontrivially along the row due to the hierarchical structure, the influence of underlying TDU layers and the specific spatial location of each TDU. This nonuniform shaping of delay values is a deliberate feature of the proposed method and plays a key role in disrupting regular phase error patterns that would otherwise reinforce grating lobes.

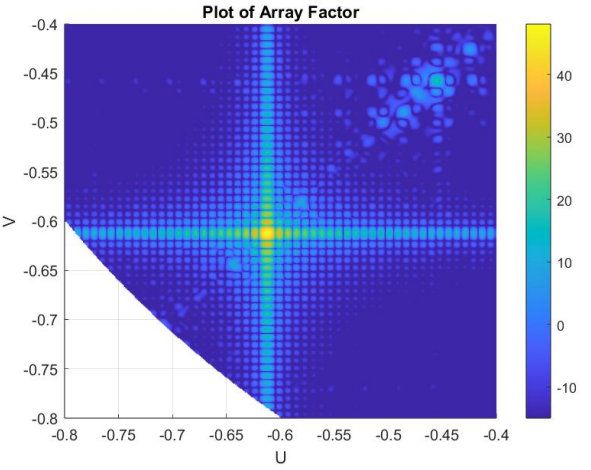

FIGURE 8. Array pattern plot for 256x256 array with constant TDU values in each layer highlighting the grating lobes.

While the reduction in RMS phase error from varying LSB values is modest, the corresponding redistribution of quantization errors, with more small errors and fewer large ones, results in meaningful suppression of grating lobes. This improvement is not a product of randomness, but rather of

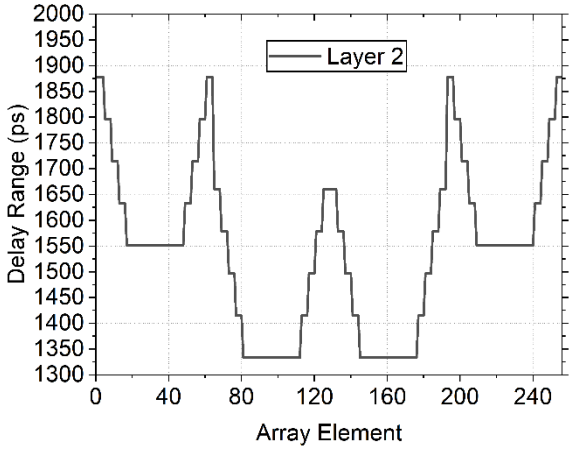

FIGURE 7. The TDU values for row 145 of a 256x256 planar array with varying TDU LSB values on layer 2.

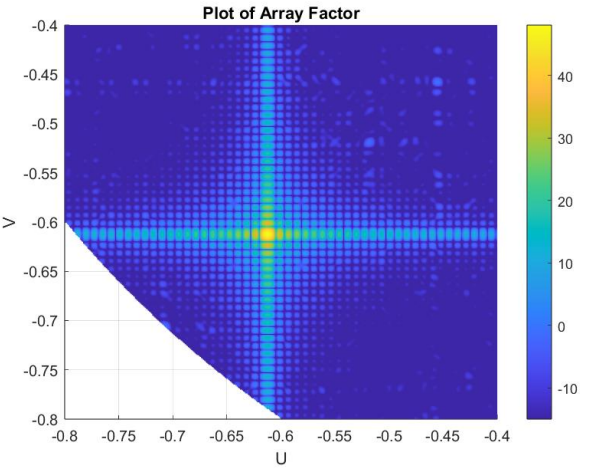

FIGURE 9. Array factor plot for 256x256 array with varying TDU values on each layer and lower grating lobes.

breaking structured and repeating error patterns that promote sidelobe formation.

Fig. 8 presents the close-in array factor in UV space for the baseline design from [15] which uses uniform TDU values in each layer. The main beam is steered to the scan direction $U = V = -0.61$. The prominent lobe near U = V = –0.456 closely matches the theoretical position of a grating lobe arising from the large subarray separation (32λ) introduced by the first TDU layer in both X and Y directions. This periodic spacing gives rise to 46 grating lobes along the diagonal (U = V) for a 60° scan. These lobes are distributed across the visible region, but several are particularly apparent in the range between –0.4 and –0.5 due to quantization-induced degradation of ideal array-level and subarray level nulls. Their spatial alignment with predicted grating lobe locations confirms their origin, distinguishing them from conventional sidelobes.

After applying the proposed LSB variations across all layers, the grating lobe and adjacent sidelobes are suppressed. This is visually shown in Fig. 9 and further quantified in Fig. 10, which compares the diagonal array factor cut for uniform and nonuniform TDU configurations.

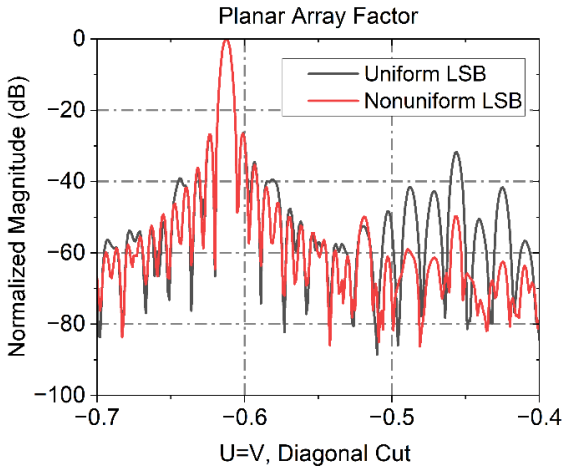

FIGURE 10. Array pattern plot for 256x256 planar array with comparison of uniform and nonuniform TDU values for a diagonal cut of U=V showing improvement to close-in grating lobes.

The primary grating lobe is reduced by 18.0 dB with some surrounding sidelobes suppressed over 20 dB.

This example illustrates that even modest improvements in phase accuracy, when distributed in a less structured manner, can significantly improve grating lobe and sidelobe performance in large arrays. A more detailed analysis of this effect, including the underlying phase error distribution, is presented in the following section using full-wave simulation of a 16×16 array.

III. VERIFICATION THROUGH FULL WAVE SIMULATION

To verify the performance of the proposed method in the presence of mutual coupling and practical antenna effects, a full-wave electromagnetic simulation was conducted using Ansys HFSS R2023 R2.1. A broadband 16×16 planar array was modelled with each element excited at constant amplitude and phase-shifted according to the proposed TDU configurations.

The array employs Vivaldi antennas as elements, designed using established techniques such as in [16]. As shown in Fig. 11, each element is modeled as a perfect electric conductor on

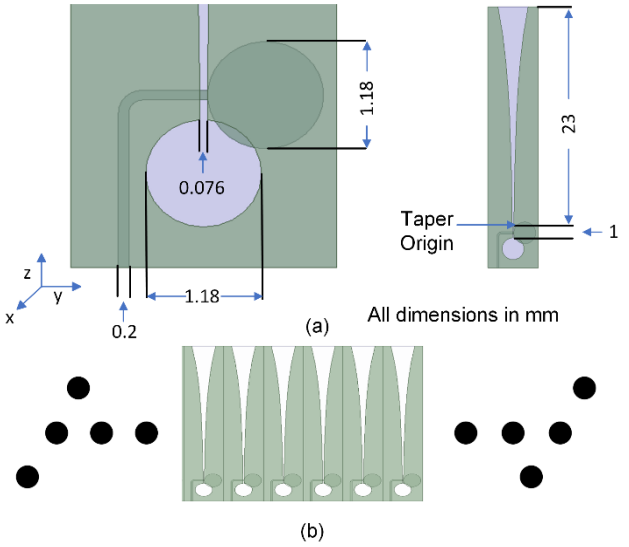

FIGURE 11. (a) Vivaldi element details and (b) section of 16x16 element planar array.

either side of a 16 mil Rogers 4003 laminate. Elements are fed via a central stripline within the substrate, with the taper defined by the exponential profile $y = 0.05e^{0.135z}$. The array pitch is 5 mm, corresponding to half a wavelength at 30 GHz.

The beamforming network comprises two TDU layers, placed at division levels 2 and 4, with 2 and 6 control bits respectively. The maximum LSB time delays are 81.6 ps and 1.62 ps for layers 1 and 2.

Full-wave simulation confirms that both uniform and nonuniform TDU configurations support complete beam steering across the intended scan range. At 30 GHz and a 60° scan angle, both configurations achieve a gain of 29.4 dBi, with a VSWR of 2.2 measured at the corner element. This confirms that the aperture efficiency remains unchanged despite the modifications to the BFN.

A notable improvement is observed in sidelobe levels, with reductions of up to 11.3 dB when using nonuniform TDU values, as illustrated in Fig. 12. In the uniform case, three prominent sidelobes appear, which are substantially suppressed under the nonuniform configuration.

These results confirm that applying a tailored TDU LSB profile can improve both phase accuracy and sidelobe performance in practical antenna arrays.

Since the Vivaldi antenna is a broadband element, a further comparison was performed at 10 GHz using the same 16×16 array configuration with both uniform and nonuniform TDU values. See Fig. 13. At this frequency, the array achieves a gain

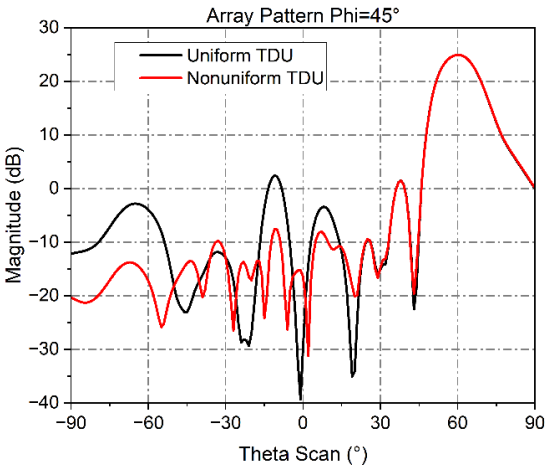

FIGURE 12. Full-wave simulation array pattern plot for 16x16 planar array with uniform and nonuniform TDU values at 30 GHz.

of 17.7 dBi, with a corner-element VSWR of 3.9 for both configurations.

At 10 GHz, however, there is little observable suppression of grating lobes when using nonuniform TDU values. This is due to the shorter electrical element spacing, the elements are spaced at $\lambda/6$ and the subarrays are separated by $2\lambda/3$. Under these conditions, no grating lobes fall within the visible region and thus the benefits of quantization error reduction do not manifest as sidelobe suppression in this case. Nonetheless, the space-saving advantages of the proposed TDU profile remain fully applicable across frequency.

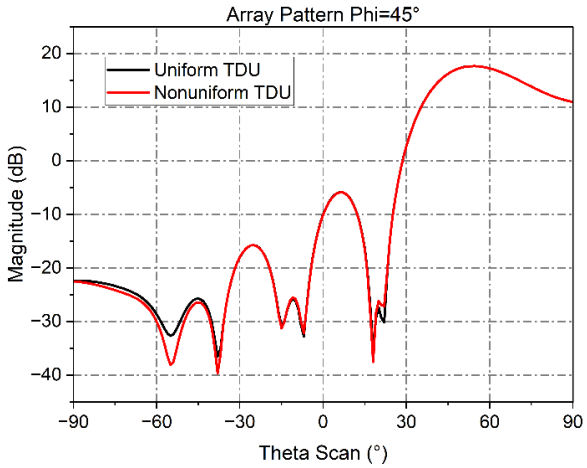

FIGURE 13. Full-wave simulation array pattern plot for 16x16 planar array with uniform and nonuniform TDU values at 10 GHz.

IV. DISCUSSION

a) **Profiling Depth Benefit vs. Benefit Trade-Off**

To satisfy typical phase error specifications, it is essential to include a layer of TDUs at the highest division level (closest to the antenna elements). Without this, multiple elements may share the same delay value, causing phase errors to grow unbounded with increasing scan angle.

A TDU layer at the first division level does not offer any scope for delay range variation. In contrast, delay profiling becomes increasingly effective in higher-level TDU layers where more elements are grouped. However, a minimum spacing of two division levels is required for meaningful profile variation.

b) **Dominant Impact of Lower TDU Layers**

The majority of the space-saving benefit arises from the lower TDU layers. In the 256x256 planar array example, layers 1 and 2 (division levels 2 and 6) account for 63% of the total space saving, while the remaining reduction is achieved by applying nonuniform TDU values to the top layer. Similarly, 16.7 dB of the total 18 dB grating lobe suppression results from applying nonuniform TDU values in just these two layers. This suggests that even partial profiling, limited to lower TDU layers, captures most of the benefit and offers a practical trade-off between complexity and performance. Designers of large-scale arrays may find this balance attractive, especially when facing constraints in fabrication, layout, or computational optimization.

c) **Applicability to Irregular Array Topologies**

The proposed method extends to irregular arrays, including clustered, thinned, or sparse layouts, since the core principle still holds: elements near the array center require less delay range than those at the edges. Thus, the method is robust and adaptable across practical array architectures.

d) **Implementation Overhead and Design**

In the 256×256 array example, the number of distinct delays is 2 in layer 1, 16 in layer 2 and 32 in layer 3. With modern CAD tools and PCB manufacturing workflows, this level of variation presents little difficulty in layout or fabrication. Nonetheless, design teams must account for the added complexity during integration, particularly in large-scale or cost-sensitive systems.

V. CONCLUSION

This paper presents a new methodology for optimizing hierarchical beamforming networks by applying nonuniform delay profiles within TDU layers. A systematic approach is proposed for designing these delay profiles, tailored to the array structure, enabling meaningful reductions in both physical footprint and phase quantization errors.

Beyond space and error savings, a central contribution of this work is the demonstrated suppression of grating lobes, achieved by reshaping the distribution of phase errors.

Numerical evaluation and full-wave electromagnetic simulations confirm that the proposed approach yields substantial improvements, including an 18.0 dB grating lobe reduction in a 256x256 planar array and a 29.9% space saving compared to the baseline configuration.

These results establish the effectiveness and practicality of the proposed method and position it as a scalable solution for advanced BFN design across a range of array sizes and configurations.

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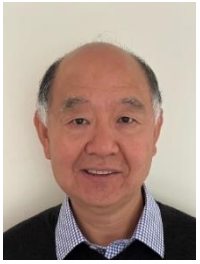

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FIGURE 1. Layout of typical TDU with n-bit control.

FIGURE 2. Hierarchical beamforming network showing divisions and layers.

FIGURE 3. 128-linear array design, TDU1 has 2 bits and LSB = 307.9 ps, TDU2 has 4 bits and LSB = 68 ps and TDU3 has 6 bits and LSB = 1.2 ps.

FIGURE 4. Graph of the TDU values on each of layers 1, 2 and 3 along the full length of the 128-element linear array with the design shown in Fig. 3.

FIGURE 5. Combined histograms for the element phase errors for the 128-element linear array with the nonuniform TDUs and uniform TDUs for a full scan from -60° to 60°, showing many more smaller errors and fewer large errors for the nonuniform TDUs as compared with uniform TDUs.

FIGURE 6. Array pattern for a 128-element linear array with constant TDU LSB values in a layer and varying TDU LSB values.

FIGURE 7. The TDU values for row 145 of a 256x256 planar array with varying TDU LSB values on layer 2.

FIGURE 8. Array pattern plot for 256x256 array with constant TDU values in each layer highlighting the grating lobes.

FIGURE 9. Array factor plot for 256x256 array with varying TDU values on each layer and lower grating lobes.

FIGURE 10. Array pattern plot for 256x256 planar array with comparison of uniform and nonuniform TDU values for a diagonal cut of U=V showing improvement to close-in grating lobes.

FIGURE 11. (a) Vivaldi element details and (b) section of 16x16 element planar array.

FIGURE 12. Full-wave simulation array pattern plot for 16x16 planar array with uniform and nonuniform TDU values at 30 GHz.

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