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ABSTRACT

Epitaxial graphene on cubic silicon carbide on silicon could enable unique optical metasurface devices seamlessly integrated with CMOS technologies. However, one of the most promising methods to obtain large-scale epitaxial graphene on this challenging system typically leads to a highly p-type-doped graphene with a Fermi level pinned at ∼0.55 eV below the Dirac point. Hence, the use of conventional gate dielectric materials such as SiO_2 and Si_3N_4 precludes the tuning of the graphene carrier concentration. We demonstrate that this limitation can be overcome with the use of polyethyleneimine (PEI) as a gate dielectric material for graphene field-effect transistors. We achieve significant tuning of the graphene's Fermi level, enabling ambipolar operation exceeding a 3 eV window. In addition, we demonstrate that excellent stability of the PEI-based devices can be achieved, thanks to the addition of a thin protective oxide film. These findings highlight the potential of ionic polymers for advancing reconfigurable graphene-based devices for photonic applications.

I. INTRODUCTION

Epitaxial graphene (EG) synthesized on cubic silicon carbide (3C-SiC) on silicon substrates provides a unique platform for wafer-scale integration of graphene with the existing silicon semiconductor technologies and infrastructures. Such an integration allows the harnessing of tunable optical and electronic properties of graphene together with the favorable optical properties of 3C-SiC for nanophotonics applications on an easily scalable silicon platform.[1] In particular, it enables the coupling of tunable graphene surface plasmon polaritons with the low-loss surface phonon polaritons in SiC offering great promise for tunable nanophotonic devices operating at mid-infrared wavelengths.[1,2]

Controlling the carrier concentration and the Fermi level of graphene is a key to the dynamic tunability of graphene's electronic and optical properties. This characteristic property of graphene can tune the photonic response of EG/3C-SiC based optical devices, including thermal emitters,[3] filters,[2] and detectors[4–9] that are uniquely achievable with the graphene/3C-SiC combination.

Despite this potential, the development of tunable electronic and photonic applications based on graphene on 3C-SiC/Si substrates has been hindered by multiple challenges. Among those, the difficulty in obtaining consistent epitaxial graphene coverage on the very defective template, compounded with electrical leakage issues into the substrate.[10–12]

Electrostatic gate control in a graphene field-effect transistor (GFET) configuration is a traditional way to control the carrier concentration in graphene. Attempts have been made toward functioning GFETs on 3C-SiC/Si substrates, where graphene was synthesized via the thermal decomposition of 3C-SiC/Si.[13,14] Those devices suffered from significant gate leakage current, hindering an efficient electrostatic gate control.[15]

In our previous work, we have successfully addressed the aforementioned issues by adopting a Ni/Cu alloy-mediated growth method to synthesize graphene on a 3C-SiC heteroepitaxial layer formed on a highly resistive Si substrate.[12] The liquid-phase nature of the epitaxial growth enables uniform graphene coverage, and the highly resistive nature of silicon allows graphene to be electrically insulated from its underlying pseudo-substrate.[12,16,17] Using a bilayer top-gate-dielectric stack of SiO_2 and Si_3N_4 and the liquid phase alloy-mediated graphene growth technique, we demonstrated room temperature transfer characteristics,[12,15] at a gate leakage current six orders of magnitude lower than the drain current.

However, field-effect measurements of graphene[15] exhibited a unipolar type of conduction due to the high p-type doping (in the order of 10^{13} cm^{-2}) with a Fermi level of ~0.55 eV below the Dirac point. The drain current showed only minimal variation under the gate modulation, suggesting a pinned Fermi level in graphene. Due to dielectric breakdown, the ambipolar conduction in graphene could not be demonstrated[13,15] as the Dirac point occurs at large positive values of gate voltage (V_{GS}).[18] To probe the ambipolar conduction, a large gate voltage operation is required, which depends on the dielectric capacitance value. A larger capacitance is necessary for achieving a wider gate modulation range, however, with conventional ceramic dielectrics, including high-k dielectrics, such as HfO_2, Al_2O_3, and ZrO_2, the challenge of dielectric breakdown persists due to the necessity of using relatively thin dielectric layers.[19]

Here, we show how to overcome this issue by replacing the traditional gate dielectric materials with a polymer electrolyte such as polyethyleneimine (PEI). PEI is widely known as an n-type dopant in GFETs and carbon nanotubes.[20–29] The amine groups in PEI contain lone pairs of electrons each, allowing them to be electron donors[20–22,28] when modulated by an external gate voltage. When voltage is applied between the PEI and graphene, the electrons move to the graphene–PEI interface to form a thin layer with a thickness in the range of 1–5 nm called the Debye layer.[30] Due to the few-nanometer range of the Debye length, the dielectric capacitance of the GFETs with PEI is ~5.17×10^{-6} F cm^{-2}, at least two orders of magnitude larger than that of the typically top or back-gated dielectrics with capacitance in the range of 10^{-8} F cm^{-2} (Ref. 31) and varies the charge concentration in graphene. Due to the higher specific capacitance of the PEI, its use as a gate dielectric material has shown lower gate voltage operation in top-gated graphene FETs.[22,32] In addition, the use of PEI is reported to be beneficial for applications such as biosensing, as they are capable of abruptly increasing the sensing range of graphene-based FETs.[33]

PEI has been used in the literature to obtain n-type doping of graphene. For example, Farmer *et al.* have used PEI to obtain graphene FETs.[20] In this case, graphene was mechanically exfoliated from highly oriented pyrolytic graphite (HOPG) and only lightly doped. Yan *et al.* have used PEI in FETs based on graphene synthesized by chemical vapor deposition (CVD) on a copper foil and reported that using PEI on graphene results in delamination upon drying due to poor interfacial adhesion between the PEI and graphene.[22] A proposed solution was the addition of polyethylene glycol (PEG) to PEI to obtain better adhesion. However, it was found that the FET transfer characteristics changed substantially with exposure to air, attributed to a degradation of the polymer–graphene interface.[22]

In this work, we use PEI to successfully unpin the highly p-type-doped epitaxial graphene under gate bias and also address the instability issue of PEI in air. In addition, we explore the use of graphene-based devices for fast (radio frequency) dynamic switching using simulations, particularly to obtain an estimate of cut-off frequencies.

II. GFET FABRICATION AND CHARACTERIZATION

Figure 1 depicts the preparation flow of the GFET devices. We used unintentionally doped, 500 nm thick NOVASiC 3C-SiC films epitaxially grown on 235 μm thick, highly resistive (resistivity > 10 kΩ cm) Si (100) substrates. 3C-SiC/Si substrate wafers are diced into 1×1 cm^2 coupons and cleaned in acetone and isopropanol before fabrication. The GFETs were fabricated using the process flow indicated in Fig. 1. At first, the photoresist AZ1512 is spin-coated on the sample, and the EG channel is defined via photolithography using the maskless aligner (MLA 150, Heidelberg Instruments). This is followed by the deposition of nickel and copper via sputtering (NanoPVD, Moorfield Nanotechnology). The graphene channel is formed after the lift-off of the photoresist in acetone, followed by annealing in a Carbolite HT furnace at 1100 °C, 5×10^{-4} mbar for 1 h. After annealing, the samples undergo a wet freckle etch for ~16 h to get rid of the metal residues and silicides, resulting in few-layer graphene (~3–7 layers) as measured by x-ray photoelectron spectroscopy (XPS), reported in our previous work,[12] see Figs. 1(a)–1(e). Note that, with the help of *in situ* neutron reflectometry measurements, we have presented the details of the unique liquid-phase alloy-mediated graphene synthesis approach in Ref. 17. After the graphene channel is formed, a second round of photoresist AZ1512 is spin-coated on the sample. This is followed by patterning the photoresist for the Source (S), Drain (D), and Gate (G) contacts, as shown in Figs. 1(f) and 1(g). The contacts were deposited via sputtering 100 nm of nickel using the nanoPVD, followed by photoresist lift-off in acetone, see Figs. 1(h) and 1(i). After the GFETs fabrication, the PEI (average molecular weight ~800, density ~1.050 g/ml, Sigma-Aldrich, viscosity ~2000–10 000 cP) was spin-coated onto the FET devices at 4000 RPM for 60 s, as given in Fig. 1(j). Finally, some of the devices were capped by 50 nm of SiO_2 deposited by e-beam evaporation at room temperature as a protection layer for the PEI, see Fig. 1(k).

Confocal Raman spectroscopy was performed at room temperature using a Witec Raman spectrometer operating at 532 nm laser using a 50× objective at a spot size of ~1 μm and incident power of 17 mW. We used a reference silicon sample (~520 cm^{-1}) for calibration. Raman mapping was performed on a 30×30 μm^2 area in the center of the FET channel using a 0.20 μm step size and 0.1 s integration time. The resulting averaged Raman spectra are examined here.

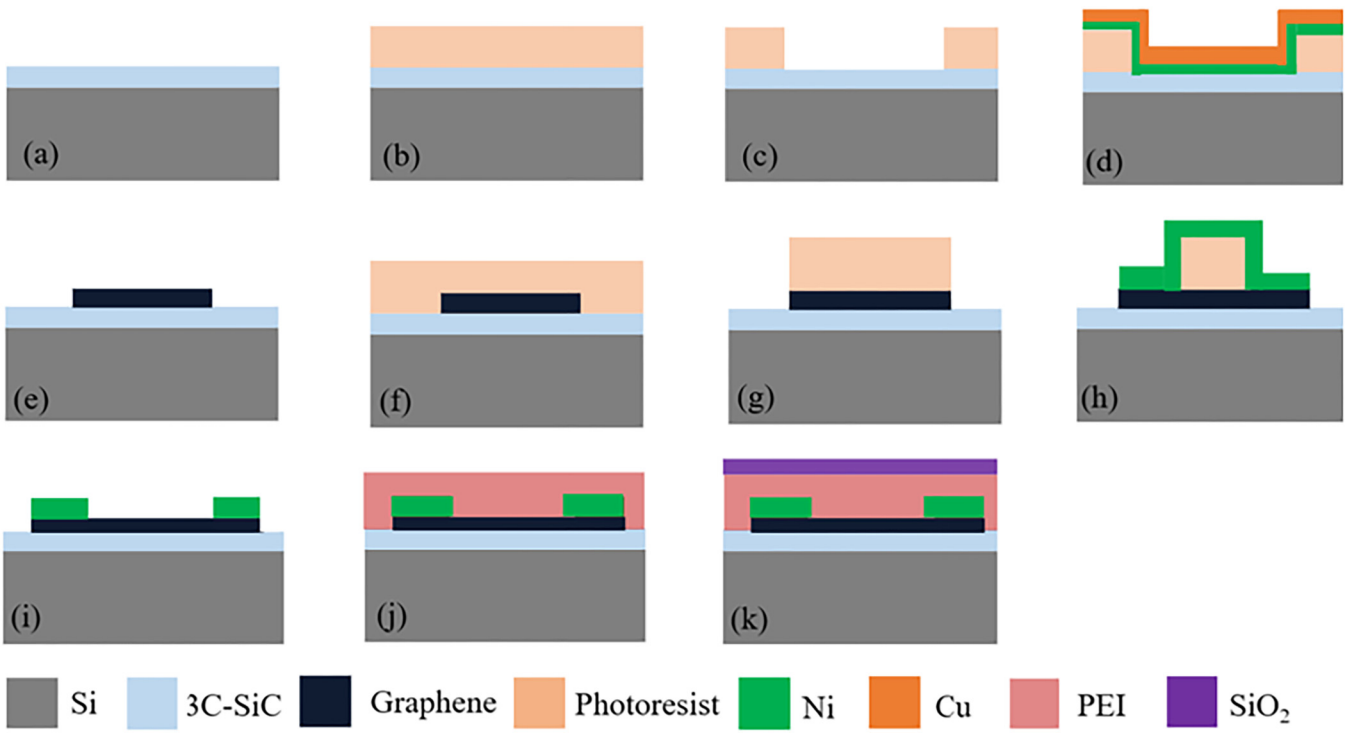

FIG. 1. Fabrication process flow of GFETs on cubic SiC on silicon using PEI. (a) and (b) Spin coating of 1.2 μm of AZ1512 photoresist and photolithography, (c) and (d) sputtering of 10 nm of nickel and 30 nm of copper, followed by liftoff and graphene channel formation (e) and (f) spin coating of the AZ1512 photoresist and photolithography, (g)–(i) sputtering of 100 nm of nickel and liftoff for source, drain, and gate contacts (j) spin coating the PEI and (k) e-beam evaporation of SiO_2.

The Scanning Kelvin Probe (SKP) measurements to estimate the work function of graphene were performed at room temperature and aeration with an M470 Biologic scanning electrochemical workstation, using a vibrating capacitance tungsten probe of 150 μm diameter positioned vertically to the sample close to 100 μm. Additionally, the probe vibration was 80 Hz with an amplitude of 30 μm. The dimension of the potential maps was $1000 \times 1000\,\mu m^2$ at a scan rate of $100\,\mu m\,s^{-1}$.

The transfer characteristics were measured at room temperature using a Keithley 4200A-SCS parameter analyzer and C-2 mini probe station from Everbeing International Corporation.

The radio frequency (RF) performance of the top-gated epitaxial graphene field-effect transistors with PEI is characterized through simulations, where the cut-off frequency is determined from scattering (S) parameter assessment across frequencies. Figure 2 shows the designed graphene field-effect transistor for the radio frequency characterization. The simulation was implemented using CST Microwave Studio with the frequency-domain solver to analyze the transistor's behavior. Discrete ports, each configured with a 50 Ω characteristic impedance, were assigned between the gate and source terminals, as well as the drain and source terminals, to facilitate impedance matching. Boundary conditions were set as open (free space added) to enhance simulation precision. An adaptive frequency sweep was employed to compute S-Parameters. The two-port configuration allowed for the evaluation of forward (S_{21}) and reverse (S_{12}) transmission. To ensure accuracy, adaptive meshing was utilized in areas with high field intensity, particularly around the interfaces. The simulation setup incorporated both material properties and structural configurations, enabling a comprehensive assessment of the transistor's RF performance. The results were analyzed using CST's post-processing tools to extract key performance metrics relevant to the transistor's application.

III. RESULTS AND DISCUSSION

Figure 2(a) shows an optical microscope view of the fabricated GFET with a channel length of 200 μm and a width of 400 μm. Figure 2(b) indicates the averaged Raman Spectrum across a $30 \times 30\,\mu m^2$ area on the graphene channel, clearly showing the D, G, and 2D intensity peaks of graphene. Figure 3 shows the Kelvin potential map of epitaxial graphene on SiC/Si(100) measured with the SKP, with a mean potential of 0.2 ± 0.01 V. The work function of the sample (WF_{sample}) can be estimated according to the equation Kelvin potential = $WF_{sample} - WF_{tip}$.[34] Using a value for the work function of the tungsten tip (WF_{tip}) of 4.5 eV, the work function for the graphene is estimated to be 4.70 eV.

This value of work function for graphene on the silicon substrate is ~0.55 eV larger than the value of 4.15 eV reported for

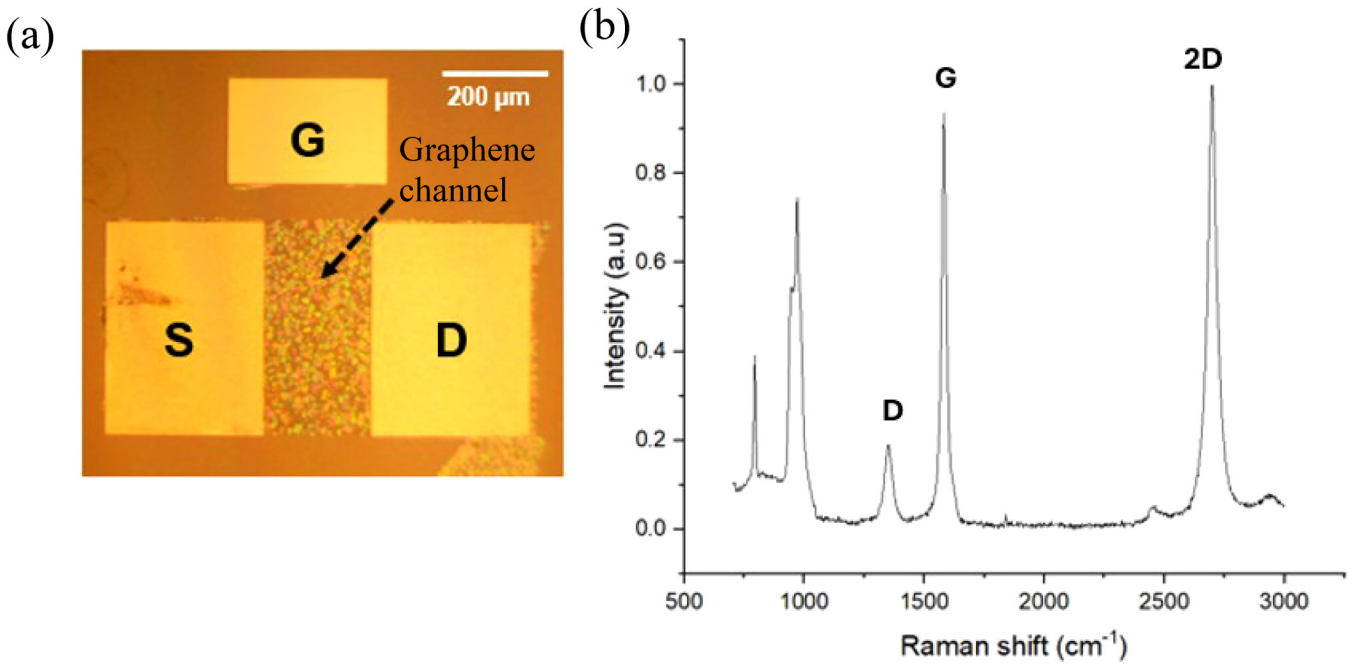

FIG. 2. (a) Optical microscopy image of a fabricated GFET with a 200 μm long and 400 μm wide graphene channel. (b) Raman averaged spectrum across a 30 × 30 μm^2 area on the graphene channel after the GFET fabrication shows the graphene characteristics peaks D, G, and 2D Raman fingerprints.

monolayer graphene on SiC(0001) by Mammadov *et al.*[35] This increment reflects the high-doping and larger Fermi level difference for graphene on Si substrates.[36]

Figure 4 shows the drain current (I_D) vs gate voltage (V_{GS}) transfer characteristics of the oxide-capped GFET at room temperature. As shown in Fig. 4, I_D first decreases from 8.2×10^{-5} A and reaches a minimum value of 5.2×10^{-5} A as V_{GS} is swept from −3.0 to −1.45 V, indicating p-type conduction in the channel. The value of V_{GS} of −1.45 V at the minimum point of I_{DS} corresponds to the Dirac voltage, V_{Dirac}.[37] This is the voltage bias

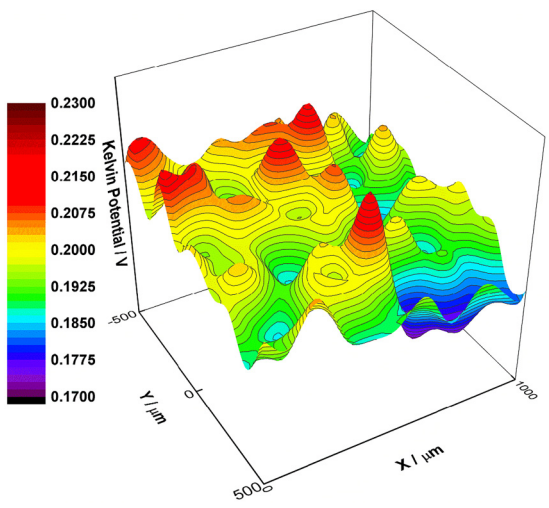

FIG. 3. Kelvin potential measured across a 1000 μm^2 area of epitaxial graphene grown on SiC/Si(100), showing a mean potential of 0.2 ± 0.01 V.

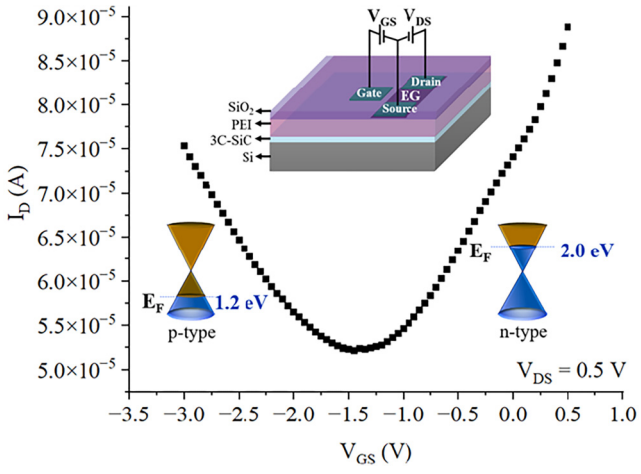

FIG. 4. Transfer characteristics of a GFET with PEI as a gate dielectric showing ambipolar conduction under the forward V_{GS} sweep (V_{GS} from negative to positive values). The Fermi level of the epitaxial graphene is tuned from a maximum of 2.0 eV above the Dirac point (n-type) to 1.2 eV below the Dirac point (p-type).

that sets charge neutrality in the FET channel, and a negative V_{Dirac} indicates an n-type doping of the graphene channel, as opposed to the highly p-type doping of the as-grown graphene.[38] Beyond V_{Dirac}, as we move toward more positive values of V_{GS}, I_{DS} increases up to 8.8×10^{-5} A at V_{GS} of 0.5 V, indicating n-type conduction.

The transfer characteristics in Fig. 4 indicate the ambipolar conduction of the GFET when PEI is used as the gate dielectric. The negative V_{Dirac} indicates that graphene is effectively n-type doped, despite the high p-type doping in the order of 10^{13} cm^{-2} (Ref. 12) of the as-grown EG on SiC(100). This can be explained by extensive n-type doping provided by the PEI, thanks to its electron-donating amine groups.[20,21]

A. Estimating the maximum carrier concentrations

The field-effect mobility μ of the GFET is given by $\mu = (L/W) \times (1/C_G) \times (1/V_{DS}) \times (dI_D)/(dV_{GS})$.[39] The maximum change in the value of $(dI_{DS})/(dV_{GS})$ is 15 μA V^{-1} in the p-type conduction regime. C_g is the gate capacitance per unit area is $\varepsilon_o \times \varepsilon_{PEI}/t_{ox}$, where ε_o and ε_{ox} are the permittivity of the free space and that of the PEI layer, respectively.

When PEI is used as a dielectric, t_{ox} is the thickness of its Debye layer. In principle, the Debye length d_{TG} for electrolyte dielectrics can be calculated if the electrolyte concentration is known, as given by $d_{TG} = (2ce^2/\varepsilon\varepsilon_0 kT)^{-\frac{1}{2}}$,[31] where c is the electrolyte concentration, e is the electric charge, and kT is the thermal energy. However, in the presence of a polymer, the electrolyte ions form complexes with the polymer chains and the exact concentration of ions is not amenable to measurement.[40] The dielectric Debye layer made of polymer molecules generally has a thickness of a few nanometers (~1–5 nm).[31,40] If we assume a Debye length for PEI of 2 nm as in Das *et al.*[40] and a dielectric constant of 9,[41]

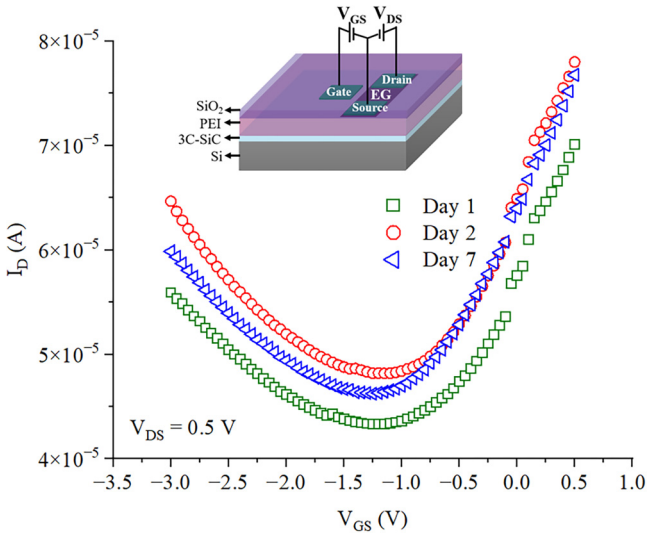

FIG. 5. Transfer characteristics of the GFET over time with a SiO_2 capping layer protecting the PEI, monitored over 7 days.

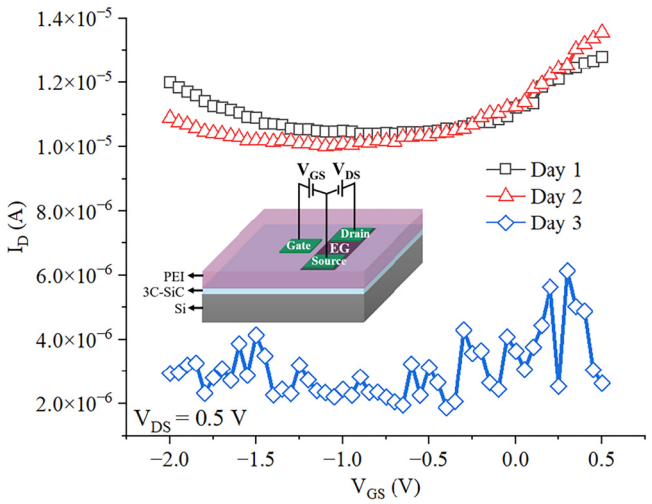

FIG. 6. Transfer characteristics of a GFET without the protective oxide capping layer, monitored over 3 days starting from the deposition of the PEI coating.

we estimate $C_G \sim 4 \times 10^{-6}$ F cm^{-2}. Furthermore, Yan *et al.*[22] have reported that the use of PEI of ~2 nm thickness resulted in ambipolar behavior, which further justifies that the assumption of 2 nm thickness for the Debye layer is reasonable. Hence, the mobility in the p-type conduction regime is ~3.8 cm^2 V^{-1} s^{-1}. The sheet resistance of graphene can be estimated from the channel resistance, $R_{channel}$, as $R_s = R_{channel} \times (W/L)$. $R_{channel}$ can be obtained from $(dV_{DS})/(dI_{DS})$ in the linear region, resulting in a value of R_{sheet} of 14 kΩ/sq. Based on the estimated mobility and sheet resistance, the sheet carrier concentration in the p-type conduction region is about 1×10^{14} cm^{-2}. The corresponding Fermi level, E_F is estimated to be 1.2 eV below the Dirac point, as indicated in the inset in Fig. 4, where $E_F = \hbar v_F \sqrt{\Pi n}$ with Fermi velocity, $v_F = 1.1 \times 10^6$ ms^{-1}.[42,43]

Similarly, the mobility for the n-type conduction region at the maximum change in the value of $(dI_{DS})/(dV_{GS})$ is 18 μAV^{-1} is estimated to be ~4.5 cm^2 V^{-1} s^{-1} with R_{sheet} of ~5 k ohm/sq, leading to a sheet carrier concentration of ~3×10^{14} cm^{-2}. The corresponding Fermi level is 2.0 eV above the Dirac point, as shown in Fig. 4.

The use of PEI has led thus to ambipolar transfer characteristics and a wide ~3 eV window tunability of the Fermi level of the epitaxial graphene, from 1.2 eV below up to 2.0 eV above the Dirac point, which is repeatable and stable with time. This is a

TABLE I. Material properties used for the simulation of RF characteristics of GFETs.

	Si	3C-SiC	PEI
Thickness (μm)	235	0.5	2.2
Dielectric constant	11.70	6.52	2.28
Electrical conductivity (S/m)	0.01	100	10^{-11}

remarkable change from the pinned E_F at 0.55 eV using conventional ceramic dielectrics.[15] Note that the smaller value of mobility compared to the as-grown EG on SiC(100) on the p-type and n-type conduction regimes can be attributed to the charge impurity scattering from the PEI.[20,40] To further validate the results, we have also presented results from a second GFET with PEI as a gate dielectric and analyzed the transfer characteristics. The transfer characteristics indicated ambipolar conduction with mobility, sheet carrier concentration, sheet resistance, and Fermi level to be 0.3 $cm^2 V^{-1}s^{-1}$, 10^{14} cm^{-2}, 160 kΩ/sq, and 1.3 eV below the Dirac

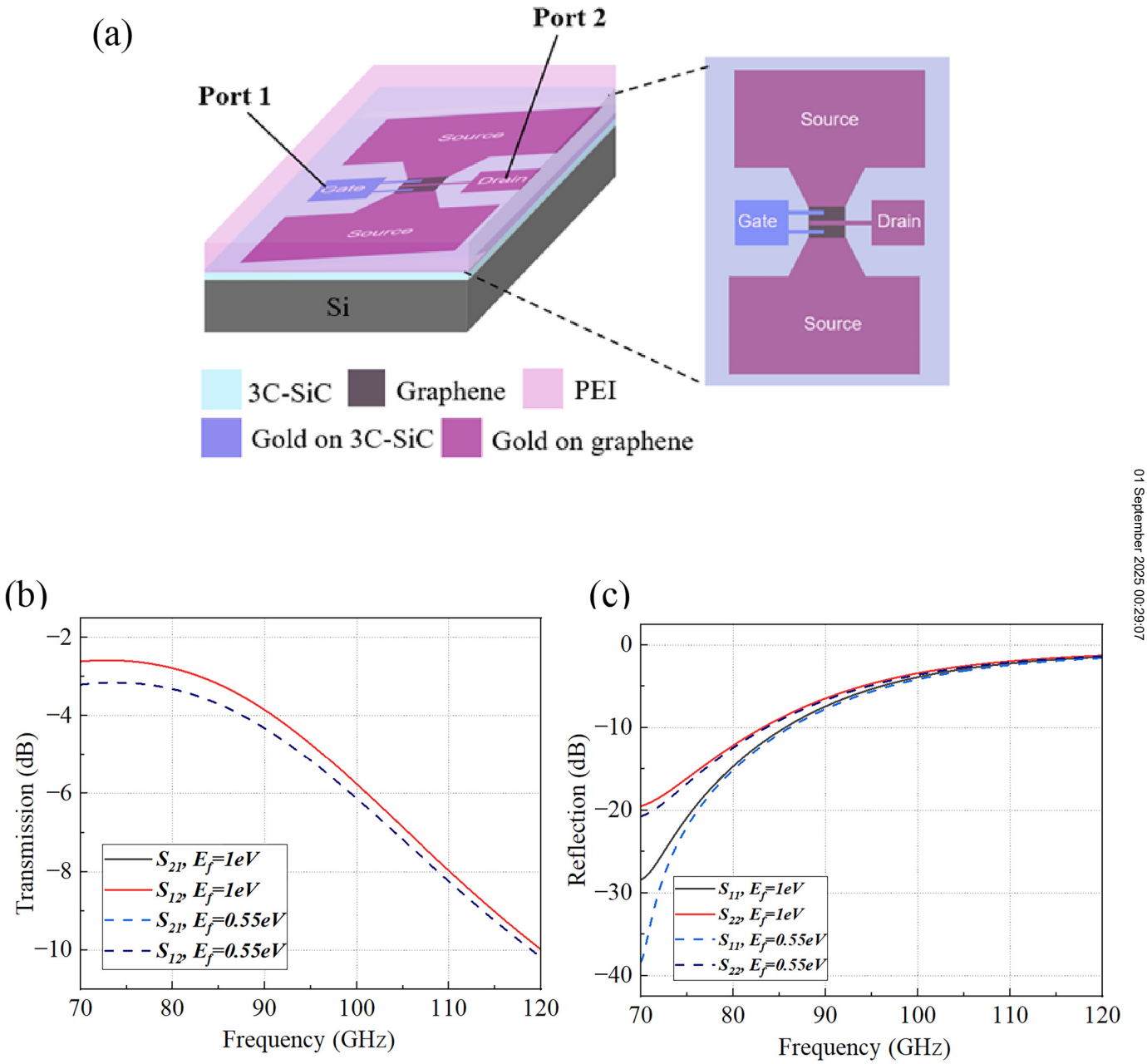

FIG. 7. (a) Schematic of an RF top-gated graphene field-effect transistor with PEI as a gate dielectric layer. (b) RF transmission coefficient of epitaxial graphene field-effect transistors, S_{21} (S_{12}) as a function of frequency, indicating an operating frequency of 70 GHz. (c) Reflection coefficient S_{11} (S_{22}) of epitaxial graphene field-effect transistors, as a function of frequency.

point, in the p-type conduction regime and a mobility, sheet carrier concentration, sheet resistance, and Fermi level of $1.25\,cm^2\,V^{-1}\,s^{-1}$, $8\times10^{13}\,cm^{-2}$, 64 kΩ/sq and 1.1 eV above the Dirac point, in the n-type conduction regime.

B. Stability of transfer characteristics with PEI over time

Figures 5 and 6 investigate and compare the repeatability and stability of the transfer characteristics of graphene/PEI GFETs measured over 3 days. Data corresponding to Day 1 in Fig. 5 were acquired on the same day after the deposition of PEI and SiO_2 capping layer.

While Fig. 5 demonstrates that the transfer characteristics remain stable for at least up to 7 days when the devices are capped by the 50 nm oxide, Fig. 6 shows that the I_D-V_{GS} trend shows a dramatic change starting on day 3. This instability confirms the previous report by Yan *et al.*[22] where the uncapped PEI exposed to air ultimately results in the degradation of the PEI/graphene interface. If the degradation in transfer characteristics shown in Fig. 6 were due to moisture ingression into the PEI, making it protonated, this would have likely resulted in a reduced electron transfer from PEI to graphene, rather than the drop in drain current observed between day 2 and day 3. This degradation could point toward a progressive drying of the PEI layer with consequent loss of adhesion to graphene. We demonstrate here that when a capping or protective layer is used on the devices, this phenomenon is halted or at least greatly suppressed. On the other hand, we believe that it is a key that the capping layer is deposited on the device at room temperature using a relatively low-energy process like evaporation to minimize damage to the PEI during the capping deposition. We acknowledge the importance of long-term performance stability under ambient and stress conditions for the successful integration of PEI-based GFETs for realistic applications. While we cannot guarantee that this simple capping approach will work long-term, this work indicates that if the system can be effectively sealed with adequate packaging and protected from external conditions, long-term stability could be achieved.

C. Extrapolation to high-frequency switching

GFET on 3C-SiC on silicon with a large tunable window paves the way for tunable electronic and optic/photonic devices. Here, we estimate its high-frequency switching capabilities using simulations in CST Microwave Studio. The simulations assess the potential operating range of GFETs. The material properties considered are given in Table I. In the case of graphene, the material parameters such as the Fermi level and relaxation time (the latter estimated from the mobility) were considered. To find out the effect of tunability, the Fermi level values of 0.55 and 1 eV were considered. The relaxation times were estimated as 0.82 Fs at the Fermi level of 0.55 eV and 0.15 Fs at the Fermi level of 1 eV.

Figure 7(a) shows the schematic of the transistor RF top-gated graphene field-effect transistor with PEI as a gate dielectric layer used for simulations. Figure 7(b) shows the transmission coefficient S_{21} (S_{12}) of the GFETs across the frequency range of 70–120 GHz. The reflection coefficients S_{11} and S_{22} are shown in Fig. 7(c). The cut-off frequency determines how fast the graphene channel current can be modulated via the gate. Figure 7 shows that the GFET has an operating frequency of ∼70 GHz. The cut-off frequency estimated is ∼103 GHz at a Fermi level of 0.55 eV and ∼100 GHz at 1 eV. These estimated values are substantially larger than the experimental value of 4.2 GHz reported for epitaxial graphene RF transistors with a 2 μm channel and 20 nm thick Al_2O_3 gate dielectric by Moon *et al.*[39] Note that this work involves only the RF simulations and does not consider the effect of parasitic capacitance arising between the gold contacts and graphene channel, as well as between the source and drain electrodes through fringing fields, which degrades the RF characteristics in real-world. In addition, graphene-gold contact resistance could further influence the RF response, increased by possible surface contamination or diffusion of adhesion layers such as titanium or chromium, whose oxides could introduce further resistance and parasitic effects in the real-world. This underscores the need for experimental validation. Liu *et al.* and Lu *et al.*[25] reported that the experimental measurements of cut-off frequencies of a GFET using PEI as a gate dielectric are likely to be limited by the low ionic mobility of the gel.[44]

IV. CONCLUSIONS

Using top-gated field-effect transistors with a polyethyleneimine gate dielectric, we have successfully unpinned the Fermi level and controlled the carrier concentration in highly p-doped graphene on a 3C-SiC/Si substrate. We also show the achievement of ambipolar conduction in graphene with a wide range of tunability of the Fermi level across a ∼3 eV window. In addition, we show that the use of a thin SiO_2 protective layer on top of the PEI prevents progressive degradation upon air exposure at least up to 7 days, suggesting that the use of adequate sealing could ensure long-term stability of the PEI. This progress underpins the realization of dynamically tunable metasurface devices based on graphene on SiC.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

A. Pradeepkumar: Conceptualization (supporting); Data curation (lead); Formal analysis (equal); Investigation (lead); Methodology

(equal); Visualization (lead); Writing – original draft (lead). **Y. Yang:** Investigation (equal); Methodology (equal); Supervision (supporting); Validation (equal); Writing – review & editing (supporting). **E. Castañeda:** Investigation (supporting); Validation (supporting); Visualization (supporting). **F. A. Angel:** Formal analysis (equal); Methodology (equal); Supervision (supporting); Visualization (supporting); Writing – review & editing (supporting). **F. Iacopi:** Conceptualization (lead); Formal analysis (equal); Funding acquisition (lead); Methodology (equal); Resources (lead); Supervision (lead); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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