A Comparative Study on Characteristics of Major Topologies of Voltage Source Multilevel Inverters

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***Abstract*—This paper provides a brief review on characteristics of main topologies of voltage source multilevel inverters. The selected topologies included conventional two levels, flying capacitor, neutral point clamped, three levels and seven levels cascaded H-bridge inverters. Several performances of topologies including quality of waveforms of output voltage, cost, complexity and reliability are selected as indicators for comparative study. The proposed topologies are simulated under the same load conditions in P-SIM environment.**

***Keywords*—Multilevel inverter, cascaded H-bridge, flying capacitor, neutral point clamped, pulse width modulation (PWM)**

I. INTRODUCTION

The main feature of dc-ac converters which are called inverter is the ability to produce sinusoidal ac output waveforms with controllable frequency, magnitude and phase from an input dc voltage. Inverters usually are used in speed control of dc motors, high voltage dc converters for power transmission systems, electrochemical processes, magnet dc supplies, dc supplies for ac drive inverters and battery chargers [1]–[5]. The insulated gate bipolar transistor (IGBT), metal oxide field effect transistor (MOSFET) or bipolar junction transistor (BJT) switches of the inverter are turned on and off according to a sequence specified by a pulse width modulation (PWM) modulation strategy to generate ac output waveforms from input dc supply. The usual methods of modulation are carrier-based PWM, space vector modulation or selective- harmonic elimination modulation [1]. Multilevel power converters are another group of inverters that have been attractive recently due to their characteristics. They have been selected as the power converter of choice in several high voltage and high power applications [6], [7]. Developments of this group of converters help researchers to overcome the deficiencies of two-level VSI in medium and high voltage applications. The main advantages of multilevel inverters compared with conventional two-level inverters are their ability to provide higher output voltage levels using power devices of lower voltage ratings, increasing the number of output voltage levels which provides a better voltage waveforms with reduced total harmonic distortion (THD), Lower stress on switching device which reduce the electromagnetic interference problem [5], [8]. Contrary to these advantages of these topologies they may have some drawbacks which need more analysis and comparisons. On the other hand some of other features like cost, reliability, complexity and control methods can be subject of research due to recent growing tendency for these topologies. This paper provides an overview of simple two level inverter and three types of multilevel inverters, as shown in Fig. 1 including their topologies and modulation strategies [9]–[11].

The reminder of paper is organized as follows. In Section II structure of simple conventional two level inverter and its characteristics is discussed. Multilevel inverter topologies including neutral point clamped, flying capacitor and cascaded H-bridge topologies are analyzed in Sect. III. A conclusion is provided in Sect. IV as the last part.

II. SIMPLE TWO LEVEL INVERTER

In this section conventional two level inverter is discussed and some features are analyzed using the P-SIM simulation model. The simulated circuit, phase and line output voltages and output current along with the frequency spectrum of output voltage are shown in Fig. 2. As illustrated in the Fig. 2a, the circuit included three pairs of switching device and each pair handling one phase of output voltage. As can be seen in this figure, a simple PWM technique is used to change the duty cycle of output voltage of each phase according to the amplitude of reference sine wave. The phase and line voltages have two and three levels in this inverter. The voltage waveforms are sinusoidal PWM signals which provide an almost in sinusoidal current on the load side. Although there are some high frequency harmonics in ranges more than 1 kHz which are clear in Fig.2d.

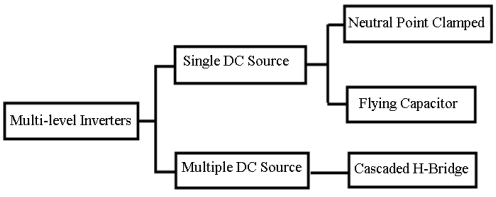

Fig. 1. Multilevel converter topologies.

To compare the quality of output voltage with other inverters, the THD factor of phase (A) of output voltage for conventional two levels inverter can be calculated from

$$THD = \left[\sum_{i=2}^{n} \left(\frac{V_i^2}{V_1^2} \right) \right]^{0.5} \quad (1)$$

As this factor is selected as one of performance indicators, it will be calculated for multilevel inverter topologies under the same load condition. An ac three phase motor is used as load for all topologies and its characteristics provided in the appendix at the end of paper. The next sections of paper focused on structure and characteristics of three types of multilevel inverters.

III. Neutral Point Clamped Multilevel Inverter

The second topology is neutral point clamped (NPC) multilevel inverter as shown in Fig. 3a. The circuit included twelve switching device for a three phase output voltage. As can be seen, a NPC inverter basically is composed of two traditional two-level voltage source converters stacked one over the other with some minor modifications.

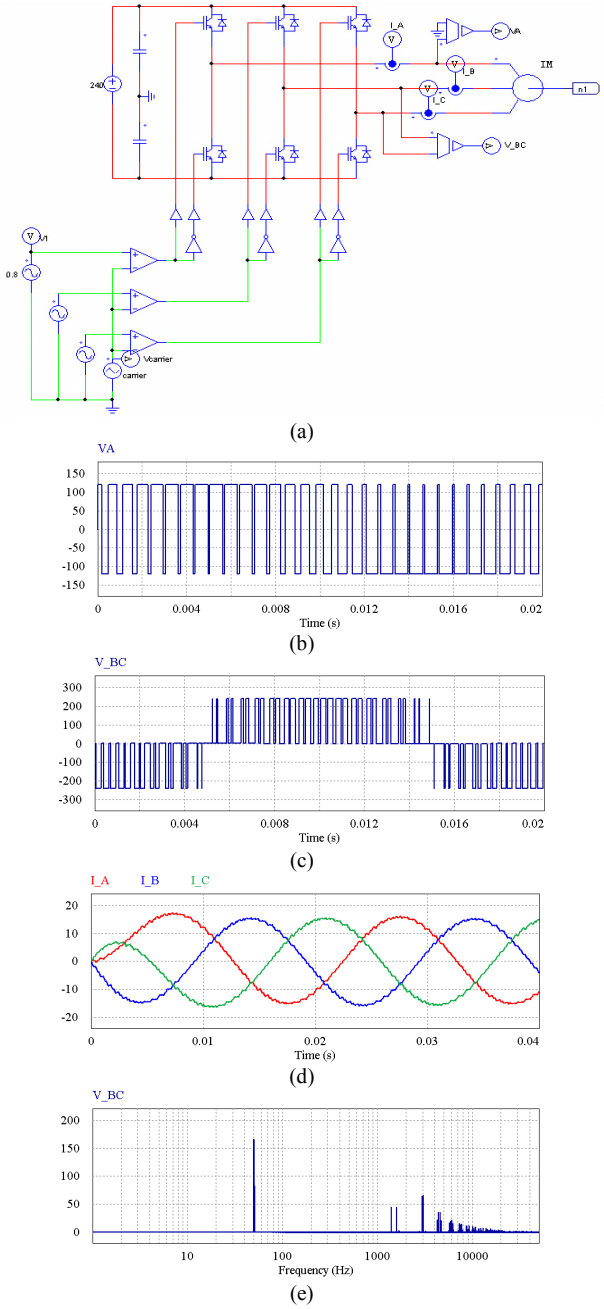

Fig. 2. . Simulation circuit diagram of conventional two-level inverter (a) simulated circuit schematic, (b) Wave form of phase voltage, (c) Waveform of line voltage, (d) line currents waveforms, and (e) frequency spectrum of line voltage.

In this topology with the same switching device, the power rating of the converter can be doubled [12]. A level shifted PWM (LS-PWM) technique is used as modulation method [13]. In this method, the carriers are arranged in vertical shifts and each carrier is set between two voltage levels. Based on the simulation circuit model, the wave forms of output phase and line voltage and currents are shown in Fig. 3b-d. The high frequency harmonics of output line voltage are shown in Fig. 3e. The value of THD for line voltage can be calculated from (1). In case of request for higher power ratings and more voltage levels, the inverter rating can be extended by increasing the number of switching devices and clamping diodes. Practically, this inverter is limited on three levels because of the number of clamping diodes needed to share the voltage in higher ratings and difficulty of controlling the dc-link capacitors.

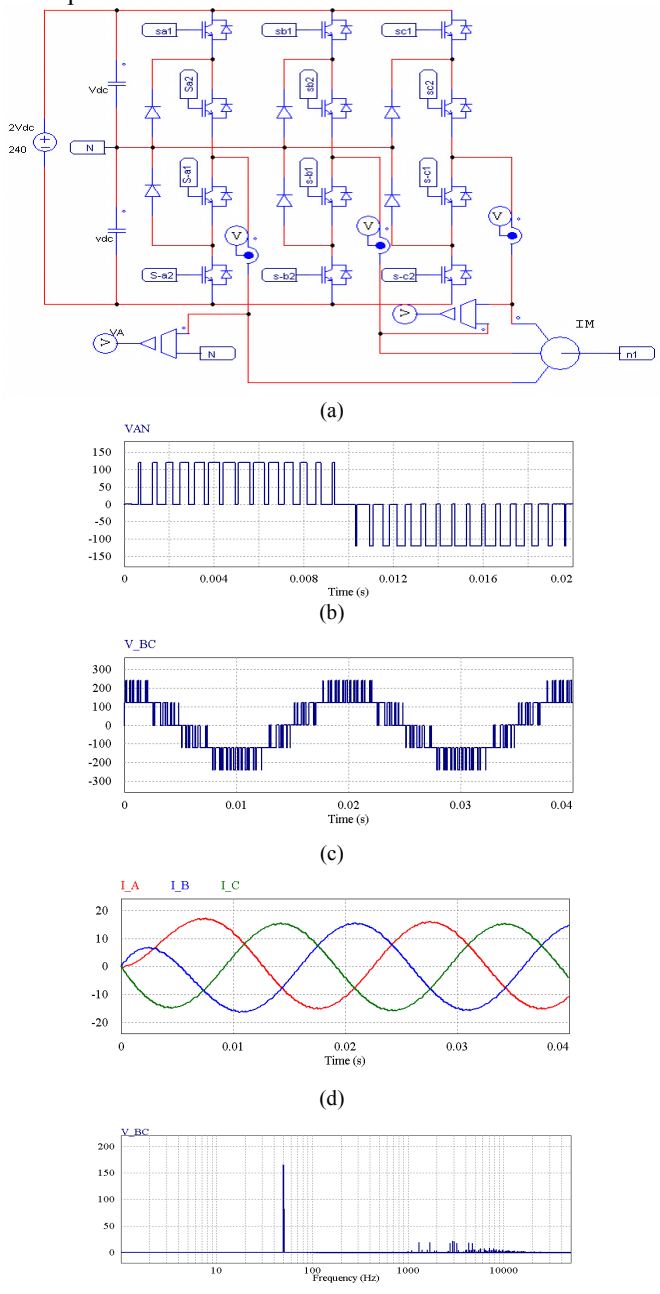

Fig. 3. Simulation circuit model of 3-level neutral point clamped inverter ,(a) simulated circuit schematic, (b) Wave form of phase voltage, (c) Waveform of line voltage, (d) line currents waveforms, and (e) frequency spectrum of line voltage.

IV. Flying Capacitor Multilevel Inverter

The flying capacitor (FC) topology is almost same as NPC topology [14]. As can be seen in Fig. 4a, the clamping diodes are replaced by flying capacitors in this topology. Based on this, the flying capacitor will have a modular structure which is easier to be extended for higher voltage levels and power rates. The output phase and line voltages waveforms, line current waveforms, and frequency spectrum are shown in Fig. 4b-e respectively.

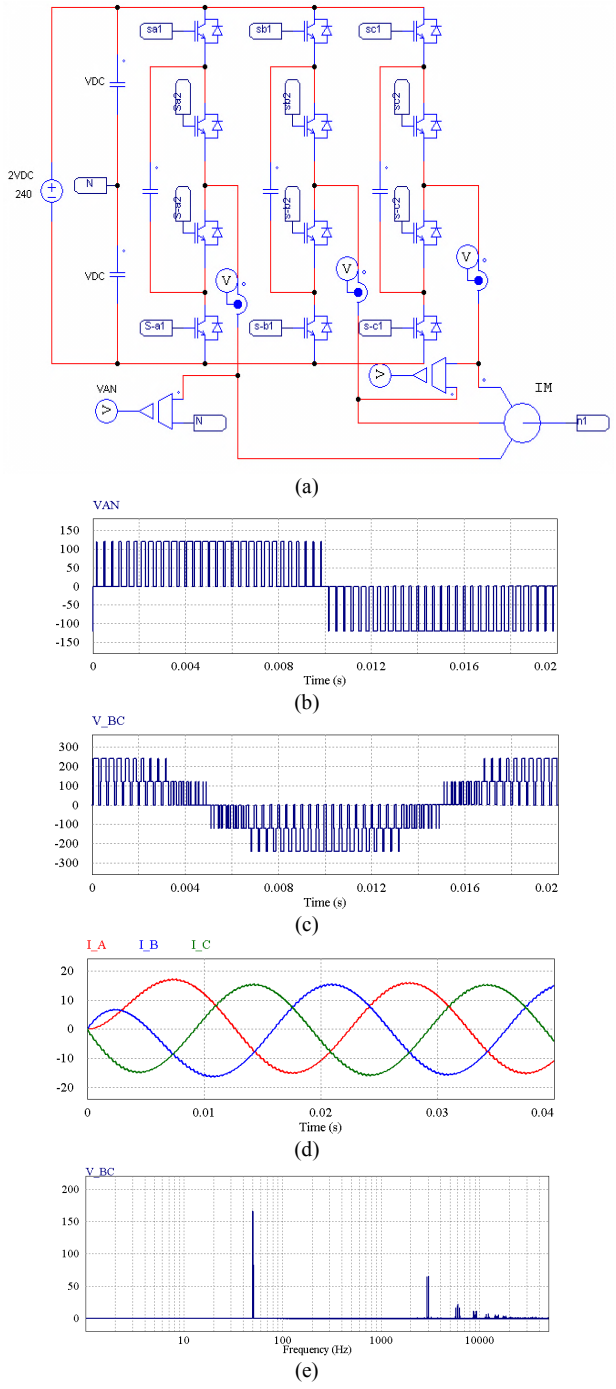

Fig. 4. Flying capacitor multilevel inverter: (a) simulated circuit schematic, (b) Wave form of phase voltage, (c) Waveform of line voltage, (d) line currents waveforms, and (e) frequency spectrum of line voltage.

V. Cascaded H-Bridge Multilevel Inverter

The last type of inverter which is analyzed is cascaded H-bridge (CHB) inverter. The structure of this inverter is based on series connection of two or more single-phase H-bridge inverters [12]. Fig. 5a shows simulation circuit model of phase (A) of three levels H-bridge inverter connected to a three phase motor. In general, a single H-bridge inverter is able to generate three different voltage levels, as shown in Fig. 5b-d. Frequency spectrum of output line voltage of this topology is shown in Fig. 5e.

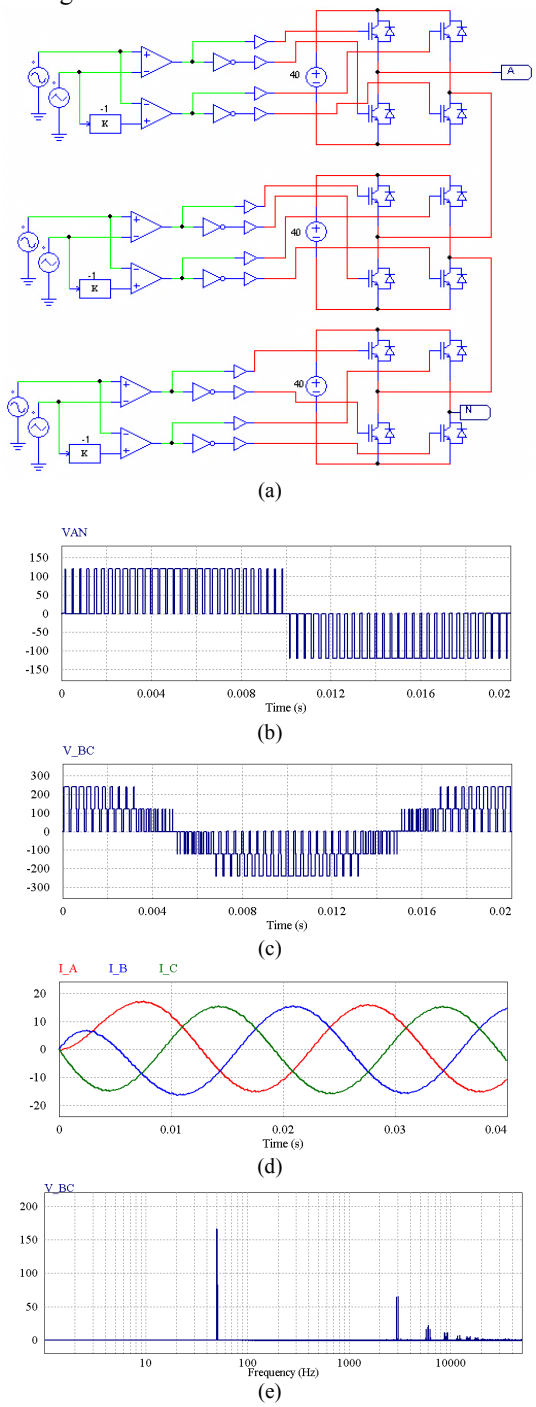

Fig. 5. Three level cascaded H-bridge inverter, phase A, (a) simulated circuit schematic, (b) Wave form of phase voltage, (c) Waveform of line voltage, (d) line currents waveforms, and (e) frequency spectrum of line voltage.

A phase shifted PWM (PS-PWM) method is used for modulation of CHB inverters [15]. Each series connected H-bridge can be modulated separately using the same reference signal. A phase shift of α is introduced between the carrier signals of adjacent modules and can be calculated from

$$\alpha = \frac{180}{n} \tag{2}$$

where n is the number of H-bridges. The output voltage of series connected H-bridges are combined to form the overall output waveform. The number of levels (m) in the output voltage depends on the number of series connected H-bridges (K) and can be calculated from

$$m = 2K + 1 \tag{3}$$

Fig. 6 shows the modulation scheme, waveforms and frequency spectrum of a seven levels CHB topology. Increasing the number of levels will reduce the output voltage and current harmonics. The main drawback of this topology is requirement of an isolated dc source for each H-bridge module [16], [17].This will increase both cost and complexity of this topology.

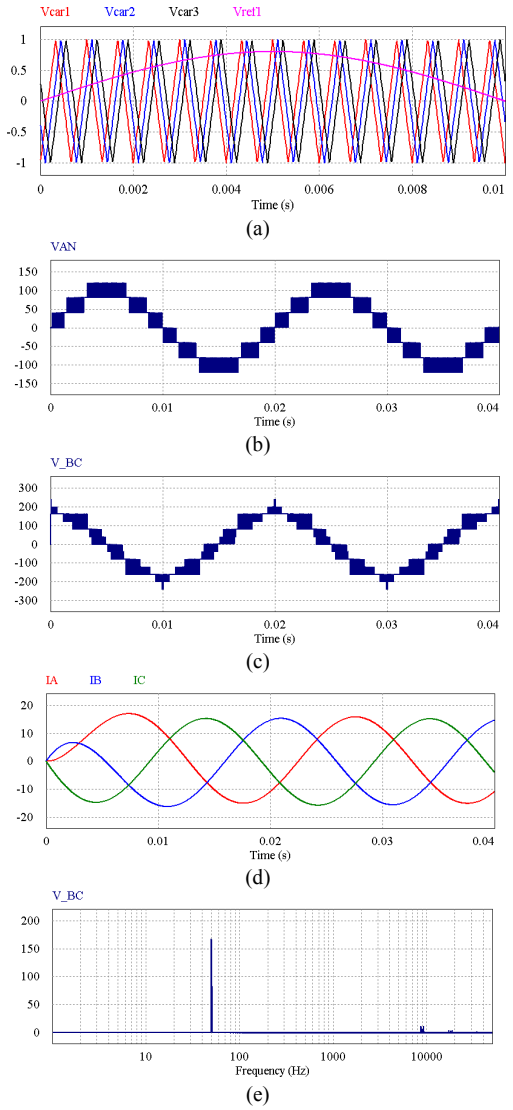

Fig. 6. Seven level CHB: (a) modulation scheme of phase A, (b) output phase voltage, (c) output line voltage, (d) output currents and (e) frequency spectrum of line voltage.

VI. Comparison of Characteristics

In this section cost, reliability, control complexity and total harmonic distortion of output voltage for all topologies are calculated and analyzed and are selected as the main comparison factors.

A. Cost

In general, the overall cost of converter will increase as the number of main components in power circuit increases. To calculate the average price of a converter based on the main components, the first step is to calculate the cost of each block in converter based on the average price of components from (4). More details on this method can be found in our previous publication [18].

$$\alpha_i = \sum_{k=1}^{n} \delta_k . \lambda_k \tag{4}$$

In this equation, λ_k is the average cost of Kth main component and δ_k is the quantity of component in the block. The main components are diodes, switching device, capacitors, inductors and the main blocks are input filter, output filter and switching block. The costs of inverter blocks should be added up to result the overall cost of each topology from

$$C_j = \sum_{i=1}^{n} \alpha_i \tag{5}$$

Based on this method, the cost of each multilevel inverter topology was calculated for the same output voltage and power ratings. The next factor is reliability of inverters which is explained in the next section.

B. Reliability

Reliability is defined as the probability that a device will perform its intended working for a specified period of time under normal operation where the device works within its safe operating area [19]. The reliability of converter topologies depend on reliability of each main block of converters and the reliability of each block depends on failure rate of its included components. The failure rate of components firstly depends on the technological complexity of the devices, voltage and thermal operating conditions. The failure rates of components are defined for a period of one million hours of operation according to the military hand book of MIL-HDBK-217 and can be calculated from

$$\lambda_j = \lambda_b . \prod_{k=1}^{n} \pi_i \tag{6}$$

where λ_b is the base failure rate of component and the factors shown as π_i are the modification factors which modify the base failure rate according to the operational and environmental conditions which affects the reliability of the component. The failure rate of each block (λ_s) can be calculated by summation of failure rates of all included components from

$$\lambda_s = \sum_{j=1}^{m} \lambda_j \tag{7}$$

where λ_j is the failure rate of j-th component per million hours. The failure rate of components or blocks whose failure will lead to complete system failure should be added to find the overall inverter failure rate and as a result the reliability can be calculated from

$$R_i(t) = e^{-\lambda_s . t} \tag{8}$$

Based on this information the failure rate of each inverter switches including IGBT and its anti-paralleled diode and then each inverter legs were calculated. They are considered as converter blocks as explained in more details in [19]–[21] and is shown in Fig. 7.

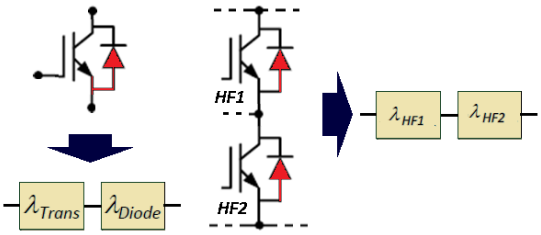

Fig. 7. Calculation of failure rate of inverter switches and legs.

The reliability functions of all topologies are calculated as an indicator for final assessment. There are some other factors effective in reliability assessment such as redundancies and fault-tolerant capabilities which are not considered in our assessment [19]. Our assessment based only the number of main components and their electrical interconnections in inverter circuits. The reliability indexes of all topologies are calculated for 100 thousand hours of systems operation. According to the calculations, it can be seen that the 7-level inverter has the lowest reliability due to the number of switching device. The normalized results are shown in Table. I.

C. Control Complexity

To compare the complexity of topologies, some indicators such as number of switching device, number of driving signals and the voltage balance circuits are considered. This is due to this fact that each switching device requires a separate and isolated gate drive signal and driving circuits increase the complexity of converter. According to this criterion number of isolated driving signals for switching devices and voltage balance circuits are considered as effective complexity factors [19]. To find the complexity index of each topology a number considered for each of above mentioned factors and summation of all numbers of each topology results its complexity index. The normalized complexity factors of all topologies are presented in Table. I for comparative study.

D. Total Harmonic Distortion (THD)

The last factor is THD of output voltage waveform which is measured based on (1). According to the simulated circuits of all topologies and the waveforms shown in Sections II–V, the waveforms of output voltage are almost in sine form although there are some high frequency harmonics.

To compare the characteristics of the three types of inverter topologies, the calculated factors including THD rate, Cost, reliability and complexity are tabulated.The table provides a quick review on main characteristics of the proposed multi-level inverter topologies. To do the final assessment of the topologies, the factors should be normalized from

$$X_i(norm) = \frac{X - X_{\min}}{X_{\max} - X_{\min}} \quad , \quad 0 \le X_i(norm) \le 1 \tag{9}$$

Table I shows the normalized value of selected parameters of the topologies as indicators which help us to compare their performance.

A quick look at the table shows that 7-level CHB topology has the lowest THD factor compared with others for the same input and load conditions. Comparing the cost shows the lowest for two-level topology and the highest for FC and 7-level CHB inverter topologies. The most reliable topology is two-level and 7-level has the lowest reliability. In case of complexity 7-level CHB is the most complex topology because it requires the highest number of switching and control signals.

TABLE I.
NORMALIZED VALUE OF SELECTED PARAMETERS FOR ALL TYPES OF INVERTER TOPOLOGIES

Topology	THD	Cost	Reliability	Complexity
2-level	1	0.80	1	0.55
3-level CHB	0.65	0.90	0.85	0.85
7-level CHB	0.25	1	0.65	1
3-level NPC	0.60	0.95	0.9	0.65
3-level FC	0.65	1	0.7	0.8

VII. CONCLUSION

This paper provides a study on several characteristics of major voltage source PWM inverters including single two levels, five levels, flying capacitor, cascaded H-bridge and neutral point clamped topologies. Cost, control complexity, reliability and total harmonic distortion of output voltage are selected as indicators analyzed via calculation and simulation. Based on the proposed study it can be concluded that the 7-level CHB topology showed the highest cost and complexity and the lowest THD and reliability compared with others. On the other hand 2-level topology is presents the highest THD of output voltage with the least complexity.

APPENDIX

LOAD CONDITION

3 Phase AC motor
V_L=210 V
Rr (rotor resistance) =2.16Ω
Lr (rotor inductance) =7.2 mH
Lm (magnetizing) =155mH
P (No. of poles) =6
Moment of Inertia =0.116
Rs (stator resistance) =2.3Ω
Ls (stator inductance) =7.2mH

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